❑ MN102H730F , MN102H73G , MN102H73K

Type	MN102H730F	MN102H73G (under development)	MN102H73K (under development)
ROM (×8-bit)	External	128 K	256 K
RAM (×8-bit)	10 K	10 K	12 K
Package	TQFP128-P-1414B *Lead-free	TQFP128-P-1414A *Lead-free	
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)	
Interrupts	• $\overline{\text{RST}}$ pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B • ATC ch.0 to 1 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 7 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • A/D conversion finish		

Timer Counter

Timer counter 0 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM0IO pin; system clock (BOSC)
- Interrupt source ····· underflow of timer counter 0

Timer counter 1 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM1IO pin; timer counter 0 output
- Interrupt source ····· underflow of timer counter 1

Timer counter 2 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM2IO pin; timer counter 1 output
- Interrupt source ····· underflow of timer counter 2

Timer counter 3 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM3IO pin; timer counter 2 output
- Interrupt source ····· underflow of timer counter 3

Timer counter 4 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM4IO pin; system clock (BOSC)
- Interrupt source ····· underflow of timer counter 4

Timer counter 5 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM5IO pin; timer counter 4 output
- Interrupt source ····· underflow of timer counter 5

Timer counter 6 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM6IO pin; timer counter 5 output
- Interrupt source ····· underflow of timer counter 6

Timer counter 7 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 9; TM7IO pin; timer counter 6 output
- Interrupt source ····· underflow of timer counter 7

Timer counter 8 : 8-bit × 1
- Clock source ····· 1/2 of system clock (BOSC) frequency; system clock (BOSC); 1/4 of system clock (XI) frequency; TM8IO pin
- Interrupt source ····· underflow of timer counter 8

Timer Counter (Continue)	Timer counter 9 : 8-bit × 1 Clock source ····· 1/2 of system clock (BOSC) frequency; 1/64 of system clock (BOSC) frequency; TM9IO pin; timer counter 8 output Interrupt source ····· underflow of timer counter 9 Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B Timer counter 13 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B Timer counter 14 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture B
Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 6 underflow frequency; 1/8, 1/2 of timer counter 0 underflow frequency; external pin Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 2 underflow frequency; 1/8, 1/2 of timer counter 4 underflow frequency; external pin UART × 4 (common use with serial 0 to 3) I^2C × 2 (common use with serial 1,3; single master)
Multiply-and-Accumulate	16-bit sign × 16-bit sign + 40-bit sign
I/O Pins — **I/O**	104 — • Common use : 59 (use of full address, address data separate 16-bit mode) • Common use : 76 (use of address 16-bit, address data separate 8-bit mode)
A/D Inputs	10-bit × 12-ch. (with S/H)
D/A Outputs	8-bit × 4-ch.
PWM	16-bit × 5-ch. (timer counter 10 to 14)
ICR	16-bit × 5-ch. (timer counter 10 to 14)
OCR	16-bit × 5-ch. (timer counter 10 to 14)
Notes	Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz , VDD = 3.3 V			60+10α*	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open			70	µA
Supply current at HALT	IDDH				30+10α*	mA

(Ta = –40°C to +85°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

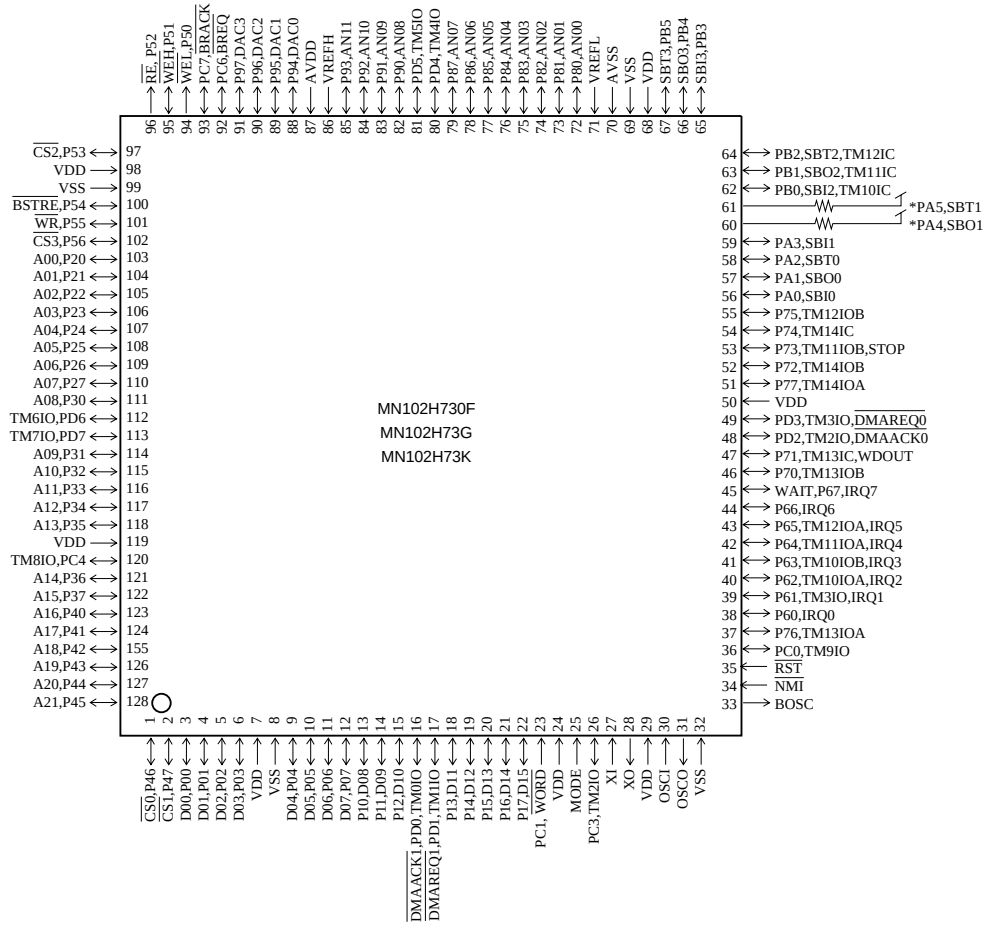
* "α" depends on products .

MN102H73G/73K/730F α = 0

MN102HF73G α = 1

MN102HF73K α = 2

Pin Assignment



TQFP128-P-1414A *Lead-free

TQFP128-P-1414B *Lead-free

* Use 4.7 kΩ to 10 kΩ.

Support Tool

In-circuit Emulator	PX-ICE102H73-128P1414	
Flash Memory Built-in Type	Type	MN102HF73G, MN102HF73K
	ROM (× 8-bit)	128 K / 256 K
	RAM (× 8-bit)	10 K / 12 K
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)
	Package	TQFP128-P-1414B *Lead-free

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