❑ MN102H73 Series

Type	MN102H730FGT	MN102H73G	MN102H73K	MN102HF73G	MN102HF73K
Internal ROM type	External	Mask ROM		FLASH	
ROM (byte)	—	128K	256K	128K	256K
RAM (byte)	10K		12K	10K	12K
Package (Lead-free)	TQFP128-P-1414B	TQFP128-P-1414A		TQFP128-P-1414B	
Minimum Instruction Execution Time	[With main clock operated] 58 ns (at 3.0 V to 3.6 V, 34 MHz)				

■ Interrupts

/RST pin, Watchdog, /NMI pin, Timer counter 0 to 9 underflow, Timer counter 10 to 14 underflow, Timer counter 10 to 14 compare capture A, Timer counter 10 to 14 compare capture B, ATC ch.0 to ch.1 transfer finish, ETC ch.0 to ch.1 transfer finish, External 0 to 7, Serial ch.0 to ch.3 transmission, Serial ch.0 to ch.3 reception, A/D conversion finish

■ Timer Counter

8-bit timer × 10

16-bit timer × 5

Timer 10 to 14 .....timer output, event count, input capture, PWM output, 2-phase encoder input

■ Serial interface

Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)

Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)

UART × 4 (common use with serial 0 to 3)

I^2C × 2 (common use with serial 1,3; single master)

■ Multiply-and-Accumulate

16-bit sign × 16-bit sign + 40-bit sign

■ I/O Pins

I/O 105 : Common use : 59 (use of full address, address data separate 16-bit mode)
Common use : 76 (use of address 16-bit, address data separate 8-bit mode)

■ A/D converter

10-bit × 12-ch. (with S/H)

■ D/A converter

8-bit × 4-ch.

■ PWM

16-bit × 5-ch. (timer counter 10 to 14)

■ ICR

16-bit × 5-ch. (timer counter 10 to 14)

■ OCR

16-bit × 5-ch. (timer counter 10 to 14)

■ Notes

Address / data separate bus interface; 8 / 16-bit bus width selectable; SRAM interface

■ Electrical Charactreistics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz , VDD = 3.3 V			60+10α*	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open			70	μA
Supply current at HALT	IDDH				30+10α*	mA

(Ta = –40°C to +85°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

Note)* "α" depends on products .

MN102H73G/73K/730F α = 0

MN102HF73G α = 1

MN102HF73K α = 2

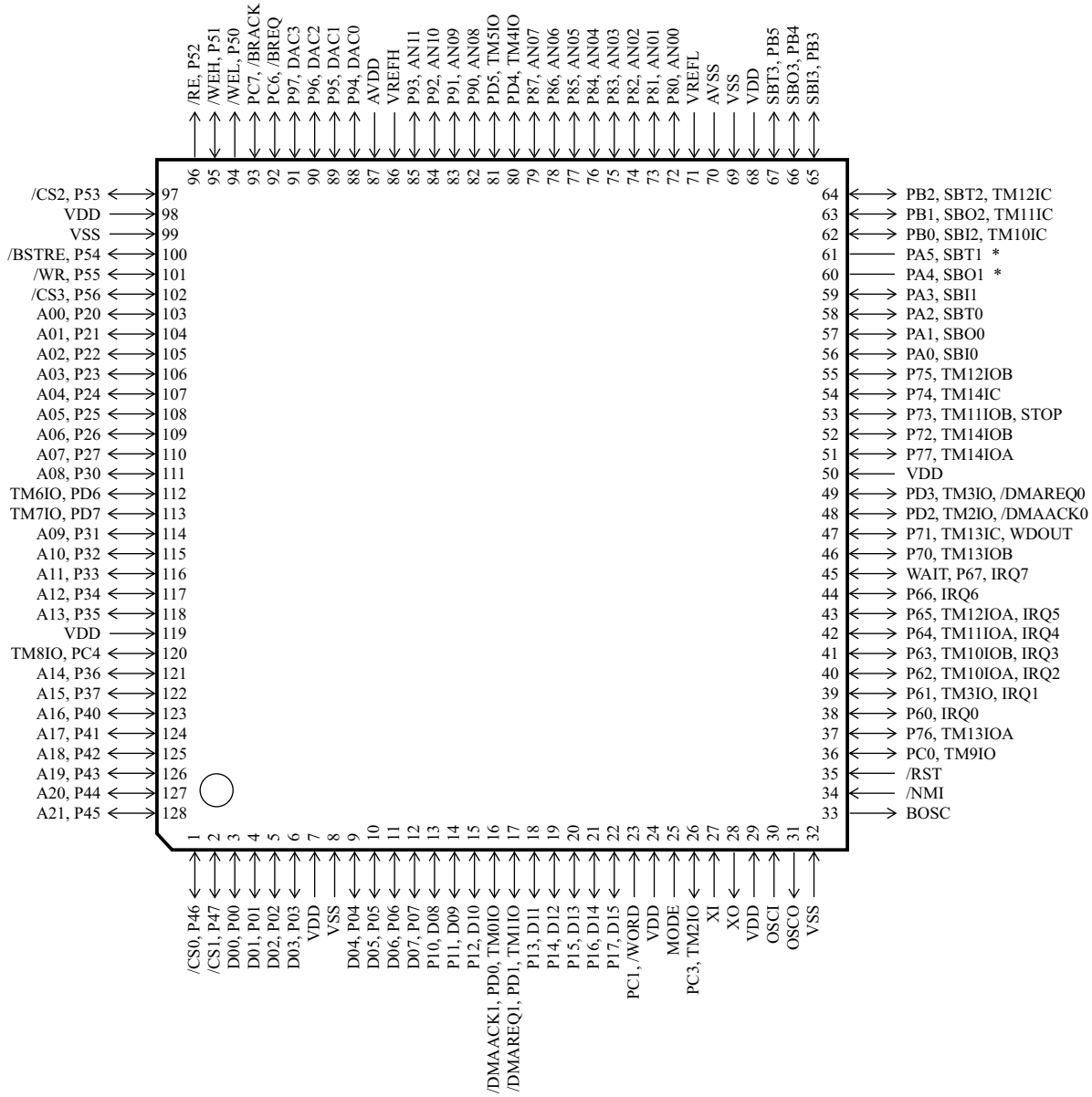
■ Development tools

In-circuit Emulator

PX-ICE102H73-128P1414

■ Pin Assignment

TQFP128-P-1414A, TQFP128-P-1414B



Note) *: Use 4.7 kW to 10 kW