

# MN103000

<b>Type</b>	<b>MN103000</b>
<b>Command ROM (×64-Bit)</b>	16 KB
<b>Data RAM (×32-Bit)</b>	16 KB
<b>Minimum Instruction Execution Time</b>	<b>17 ns (at 3.3 V, 60 MHz)</b>
<b>Interrupts</b>	• RESET • IRQ × 8 • NMI • Timer × 28 • SIF × 4 • DMAC × 4 • WDT • A/D • System error
<b>Timer Counter</b>	<p><b>Timer Counter 0 to 3: 32-Bit × 1</b> (Interval Timer, Event Count, Timer Output, Interrupt, Clock Source for Serial I/F, A/D Conversion Trigger)</p> <p>Clock Source IOCLK, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Underflow of Timer Counter 0, 1, 2, 3</p> <p><b>Timer Counter 4 to 7: 32-Bit × 1</b> (Interval Timer, Event Count, Timer Output, Interrupt, Clock Source for Serial I/F)</p> <p>Clock Source IOCLK, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Underflow of Timer Counter 4, 5, 6, 7</p> <p>* Configuration of Each of Timer Counters 0 to 3 and Timer Counters 4 to 7 can be Changed to 8-, 16- and 24-Bit Timer Counters</p> <p><b>Timer Counter 8: 16-Bit × 1</b> (Interval Timer, Event Count, Toggle Output (2 Lines), PWM Output, One-Shot Output, Input Capture (2 Lines), Interrupt, DMA Start, Generation of Timer Synchronous Output Timing)</p> <p>Clock Source IOCLK, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Overflow of Timer Counter 8, Coincidence with Compare Capture (2 Lines) or at Capture</p> <p><b>Timer Counter 9: 16-Bit × 1</b> (Interval Timer, Event Count, Toggle Output (2 Lines), PWM Output, High-Speed PWM Output, One-Shot Output, Input Capture (2 Lines), Interrupt, DMA Start, Generation of Timer Synchronous Output Timing)</p> <p>Clock Source IOCLK, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Overflow of Timer Counter 9, Coincidence with Compare Capture (2 Lines) or at Capture</p> <p><b>Timer Counter 10: 16-Bit × 1</b> (Interval Timer, Event Count, Toggle Output (3 Lines), PWM Output (2 Lines), One-shot Output, Input Capture (3 Lines), Interrupt, DMA Start, 2-Phase Encode)</p> <p>Clock Source IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter</p> <p>Interrupt Source Overflow of Timer Counter 10, Underflow, Coincidence with Compare Capture (3 Lines) or at Capture</p> <p><b>Timer Counter 11: 16-Bit × 1</b> (Interval Timer, Event Count, Toggle Output (4 Lines), PWM Output, Inter-Offset 3-Phase PWM Output, One-shot Output, Input Capture (4 Lines), Interrupt, DMA Start, 2-Phase Encode)</p> <p>Clock Source IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter</p> <p>Interrupt Source Overflow of Timer Counter 11, Underflow, Coincidence with Compare Capture (4 Lines) or at Capture</p> <p><b>Timer Counter 12: 16-Bit × 1</b> (Interval Timer, Event Count, Toggle Output (4 Lines), PWM Output (3 Lines), One-Shot Output, Input Capture (4 Lines), Interrupt, 2-Phase Encode)</p> <p>Clock Source IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter</p> <p>Interrupt Source Overflow of Timer Counter 12, Underflow, Coincidence with Compare Capture (4 Lines) or at Capture</p> <p><b>Watchdog Timer: 16-Bit to 25-Bit × 1</b></p>

<b>Serial Interface</b>		<b>Serial 0, 1: 7-Bit, 8-Bit × 2</b> (Clock Synchronous mode, Start-Stop Synchronous Mode, I <sup>2</sup> C Mode) Clock Source . (Clock Synchronous Mode, Start-Stop Synchronous Mode) IOCLK, the Underflow of Timer Counter, External Clock (I <sup>2</sup> C Mode) IOCLK, the Underflow of Timer Counter	
<b>I/O Pins</b>	<b>I/O</b>	<b>51</b>	• Common use 51
	<b>Output</b>	<b>25</b>	• Common use 25
	<b>Input</b>	<b>13</b>	• Common use 13
<b>A/D Inputs</b>		10-Bit × 8ch	
<b>PWM</b>		16-Bit × 5ch	
<b>ICR</b>		16-Bit × 15ch (Common with OCR)	
<b>OCR</b>		16-Bit × 15ch (Common with ICR)	
<b>Timer Synchronous Output</b>		4-Bit (Synchronous Output) × 2ch	
<b>DMAC</b>		4ch	
<b>Package</b>		QFP160-P-2828B	

**Electrical Characteristics**

**Supply Current**

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
<b>Operating Supply Current</b>	IDD1	VDD, PVDD, AVDD = 3.3 V VI = VDD or VSS Fosc = 15.0 MHz FRQS pin = Hi level Output released			250	mA
<b>Supply current at SLEEP</b>	IDD2	VDD, PVDD, AVDD = 3.465 V VI = VDD or VSS Fosc = 15.0 MHz FRQS pin = Hi level Output released			50	mA
<b>Supply current at HALT</b>	IDD3	VDD, PVDD, AVDD = 3.465 V VI = VDD or VSS Fosc = 15.0 MHz FRQS pin = Hi level Output released			5	mA
<b>Supply current at stopping</b>	IDD4	VDD, PVDD, AVDD = 3.465 V VI = VDD or VSS Fosc = Oscillation stopped Output released			300	μA

(Ta = -20 °C to +70 °C)

## Electrical Characteristics (Continue)

### A/D Conversion Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3.3 V, VREF- = 0.0 V			±7	LSB
A/D conversion relative Error		A/D conversion clock = 5 MHz			±5	LSB
A/D conversion time			2.8			µs

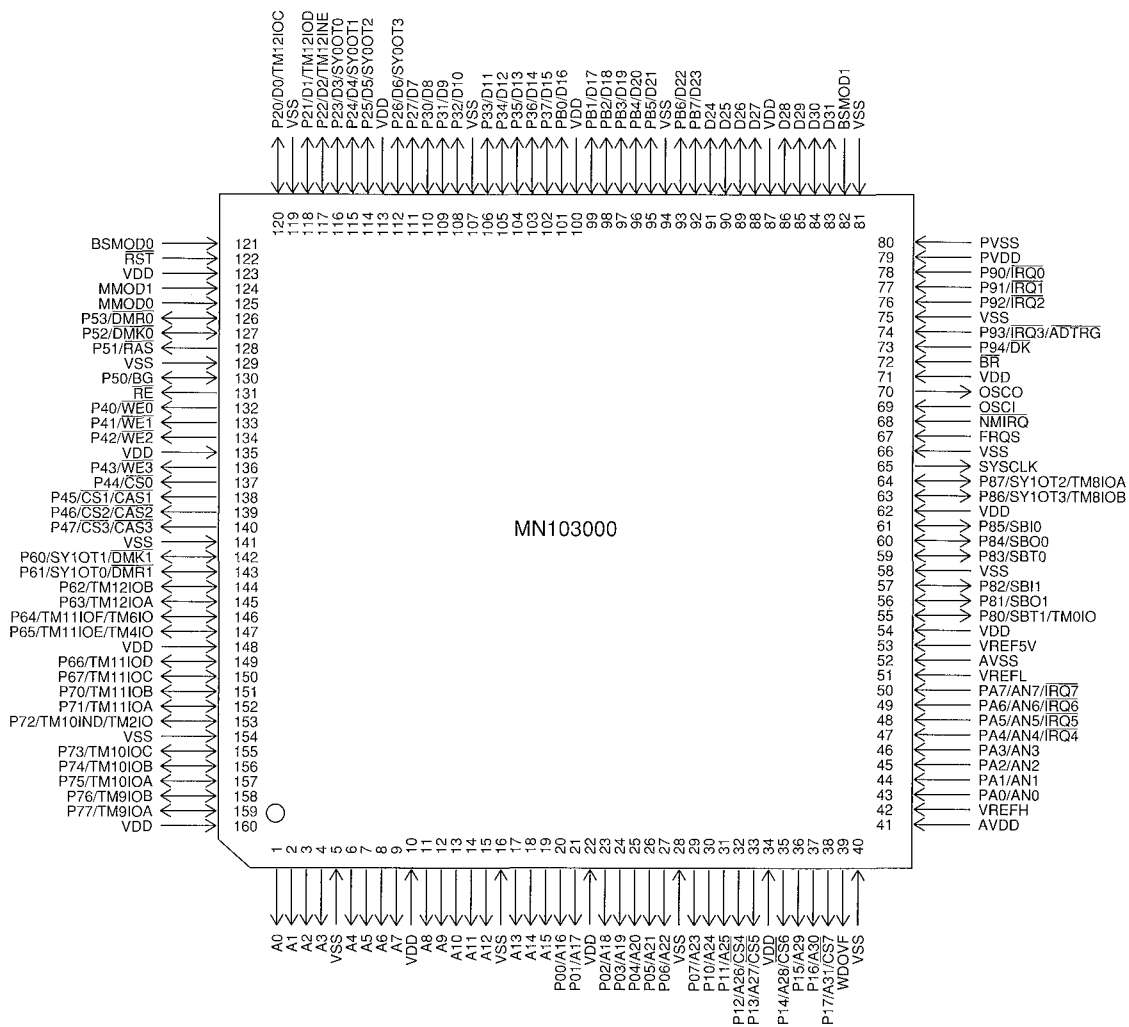
(Ta = -20 °C to +70 °C, AVDD = 3.3 V, AVSS = 0.0 V)

## Support Tool

### In-Circuit Emulator

PX-ICE103000

### Pin Assignment



QFP160-P-2828B