MN103L08 Series

32-bit Single-chip Microcontroller

■ Overview

The MN103LF08K of 32-bit single-chip microcomputers incorporate multiple types of peripheral functions. This chip series is well suited for camera, TV, VCR, AV, printer, telephone, FAX machine, air-conditioner, music instrument and other applications.

This LSI has flexible and optimized hardware configurations and simple efficient instruction set. This LSI incorporates an internal ROM of 256 KB (maximum) and RAM of 20 KB (maximum), 10 external interrupts, 71 internal interrupts including NMI, 23 timer counters, 8 sets of serial interfaces, A/D converter, 2 sets of watchdog timer, DMA, Buzzer, remote control reception and HDMI-CEC.

With 5 oscillation systems (external high frequency: 4 MHz to 20 MHz/ external low frequency: 32.768 kHz/ internal high frequency: 20 MHz/ internal low frequency: 35 kHz/ PLL: frequency multiplier of high or low frequency) contained on the chip, and the internal clock can be switched to four oscillation clock except the internal low oscillation. The internal clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming.

A machine cycle (minimum instruction execution time) is 25 ns (internal operating condition: 1.8 V, 40 MHz).

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN103LF08K	256 KB	20 KB *1	Flash EEPROM version	LQFP100-P-1414 QFP100-P-1818B

Note) *1: use On-Chip-Debugger 19.5 KB

■ Features

- CPU core

MN103L core (The instruction set is compatible MN103S series)
Memory 4 GB (instruct/data common use)
LOAD-STORE architecture(3-stage pipeline)
Machine cycle
High-speed mode 25 ns/ 40 MHz (Max)
Low-speed mode 30.5 μs/ 32.768 kHz (Max)
Operation mode
NORMAL mode (CPU clock operation, Peripheral circuit clock operation mode)
SLOW mode (CPU clock operation, Peripheral circuit clock operation mode)
HALT mode (CPU clock stop, Peripheral circuit clock operation mode)
STOP mode (All clocks stop mode)

- Internal memory

MN103LF08K : ROM 256 KB / RAM 20 KB

- Clock oscillation circuit: 5 circuits

External high-speed oscillation (clkosc) : Crystal oscillator/ Ceramic oscillator
: 4 MHz to 20 MHz
External low-speed oscillation (clkx) : Crystal oscillator/ Ceramic oscillator
: 32.768 kHz
Internal high-speed oscillation (clkrc) : 20 MHz
Internal low-speed oscillation (clkrcx) : 35 kHz
PLL output (clkpll) : 60 MHz to 120 MHz

- Clock multiple circuit (PLL)

Multiplication rate : 4, 6, 8, 10, 12, 16, 20 multiplied clock of clkosc
2440 to 3660 multiplied clock of clkx
Clock dividing : 2, 3 divided of clkpll
Output clock : 20 MHz to 40 MHz (clkplldiv)

- Internal operation clock 5 types

CPU operation clock (clkcpu)
Frequency : 40 MHz (Max)
Clock source : clkplldiv, clkosc, clkrc, clkx
Clock dividing : 1, 2, 4, 8, 16, 32, 64, divided of clock source

Peripheral circuit operation clock (clkbus)
Frequency : 20 MHz (Max)
Clock source : clkplldiv, clkosc, clkrc, clkx
Clock dividing : 2, 4, 8, 16, 32, 64, 128 divided of clock source
(This setting is independent from the dividing clock setting of clkcpu.
Set the frequency of clkbus to less than clkcpu.)

Peripheral circuit operation clock (clksp)
Frequency : 22 MHz (Max)
Clock source : clkrc, clkosc, clkplldiv
Clock dividing : 1, 2, 4, 8, 16 divided of clock source

High-speed oscillation clock (clkoscsel)
Frequency : 22 MHz (Max)
Clock source : clkrc, clkosc

Internal low-speed oscillation clock (clkrcx)
Frequency : 42 kHz (Max)

■ Features (continued)

- Internal operation clock (continued)

Low-speed oscillation clock (clkx)

Frequency : 32.768 kHz (Max)

- Bus interface

Bus area : 2 MB × 2 banks

Data bus : 8/ 16 bits

- DMA Controller

Transfer area : Internal ROM space / Internal RAM space / Internal I/O area / External memory space
↔ Internal ROM space / Internal RAM space / Internal I/O area / External memory space

Channel : 4 ch

Transfer form : 2 bus cycles transfer

Transfer requests : 44 types
External interrupts:4, Timer:19, Serial:15, IIC: 3, A/D converter:1, Remote control:1, Software:1

Transfer modes : 3 modes (One word transfer / Burst transfer / Intermittent transfer)

- Interrupt functions

Internal interrupts : 71 factors
(Timer:29, Serial I/F:10, IIC:6, Watchdog timer:1, DMA:12, A/D converter:1, Real-time clock: 2, Remote control: 4, Power Voltage Detection: 2, HDMI-CEC:1, AC zero cross: 2, System error:1)

External interrupts : 10 factor
(IRQn (n = 0 to 7) : 8, NMIRQ (shares an interrupt factor with IRQ7) : 1, KEY: 1)

- Watchdog Timer

Watchdog Timer

On detection of error, hard reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hard-reset is done by a series of two time-out events)

Time-out cycle : CPU clock cycle × N (N = 2^{16}, 2^{18}, 2^{20}, 2^{27})

Watchdog Timer2

On detection of error, hard reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hard-reset is done by a series of two time-out events)

Time-out cycle : Internal low-speed oscillation clock cycle × N (N = 2^4, 2^5, 2^6, 2^7, 2^8, 2^9, 2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15})

- Timer counter 23 units

General purpose 8-bit timer	× 6 unit
8-bit free-run timer	× 1 unit
General purpose 16-bit timer	× 7 unit
Motor control timer	× 1 unit
Baud rate 8-bit timer	× 8 unit

Timer 0 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), compare register with double buffer
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

Timer 1 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 0), compare register with double buffer
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

■ Features (continued)

- Timer counter (continued)

Timer 2 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), 24-bit cascade connection (to timer 0, timer 1), compare register with double buffer
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

Timer 3 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 2), 32-bit cascade connection (to timer 0, timer 1, timer 2), compare register with double buffer
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

Timer 4 (8-bit timer)

Timer count (Up count), external event count, timer pulse output, PWM output (Cycle is fixed)
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

Timer 5 (8-bit timer)

Timer count (Up count), external event count, timer pulse output, 16-bit cascade connection (to timer 4),
Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clkx, external clock

Timer 6 (8-bit free-running timer)

Clock source : clksp, clkbus, clkx, clksp/2^{12}, clksp/2^{13}, clkx/2^{12}, clkx/2^{13}

Timer 7 (16-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (1 system)
Clock source : clksp, clkbus, external clock, timer 5 output, timer 6 compare match cycle divided by 1, 2, 4, 16

Timer 8 (16-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (1 system)
32-bit cascade connection (to 16-bit timer 7), 32-bit PWM output
Clock source : clksp, clkbus, external clock, timer 5 output, timer 6 compare match cycle divided by 1, 2, 4, 16

Timer 9, 10, 11, 12, 13 (16-bit timer)

Timer count (Up count, Down count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (2 systems)
Clock source : clkbus, clkbus/8, timer 0, 1 compare match cycle, external clock

Timer M (Motor control 16-bit timer)

Timer pulse output, external event count, complementary 3 phases PWM output (triangular wave and saw-tooth wave output,
dead time insertion), 4 phases PWM output (triangular wave and saw-tooth wave output,
dead time insertion), output control by external interrupt (Hi-Z output or output data is fixed)
Clock source : clksp, clkbus, external clock divided by 1, 2, 4, 16

Timer B0, B1, B2, B3, B4 (Baud rate 8-bit timer)

Baud rate timer for serial transfer base clock generation
Clock source : clksp, clksp/2, clksp/4, clksp/8, clksp/16, clksp/32, clksp/64, clksp/128, clksp/256,clkbus, clkbus/2,
clkbus/4, clkbus/8, clkbus/16, clkbus/32, clkbus/64

Timer B5, B6, B7 (Baud rate 8-bit timer)

Baud rate timer for IIC transfer base clock generation
Clock source : clkx, clksp

■ Features (continued)

- Real time clock

  Calendar function (second, minute, hour, month, year)

  Alarm function, Cycle interrupt

  Clock source : clksp, clkx

- Buzzer

  Output frequency : clksp/2^9, clksp/2^{10}, clksp/2^{11}, clksp/2^{12}, clksp/2^{13}, clksp/2^{14}, clkx/2^3, clkx/2^4

- Serial interface 8 channels

  UART/ clock synchronous : 5 channels

  IIC : 3 channels

  Serial 0, 1, 2, 3, 4 (UART/Synchronous serial interface)

  UART

  Parity check, overrun error/framing error detection

  Transfer size can be selected from 7 to 8 bits.

  Clock Synchronous

  The communication type can be selected from 2-ware or 3-wire.

  First tansfer bit can be selected from MSB or LSB

  Arbitrary size of 2 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Synchronous edge selection of transfer clock.

  Maximum transfer rate : 5 MHz

  Clock source : Baud rate timer Bn output (n = 0 to 4), external clock

  Serial 5, 6, 7 (Multi master IIC)

  Multi master IIC

  100 kHz/ 400 kHz communication is supported

  7-bit, 10-bit slave address is settable

  General call communication mode is supported

  Clock source : Baud rate timer Bn output (n = 5 to 7), external clock

- HDMI-CEC

  HDMI-CEC HDMI Specification Compatible with CEC communication option

  Clock source : clkx, clkbus

- Remote control reception circuit: 1 unit

  Association for Electric Home Appliances format

  Clock source : clkx, clkoscsel

- A/D converter Resolution: 10 bit

  Channel : 16 channels

  Clock source : clkbus/2, clkbus/4, clkbus/8, clkbus/16, clkx × 2

- Auto reset

  Auto reset function can be selected ON/OFF

- Power supply voltage detection circuit

  Detection voltage can be set 2.2 V to 4.0 V by software

- Clock monitoring function

  Frequency error detection of external / PLL clock.

  Hardware reset or non-maskable interrupt generation can be selected by program when a frequency error is detected.

- LED driver: 8 sets

■ Features (continued)

- Port function

I/O ports:	87	pins
CMOS I/O	56	pins
Combination CMOS I/O and oscillation pin:	4	pins
Combination CMOS I/O and Analog input:	16	pins
Combination CMOS I/O and LED driver:	8	pins
Nch open drain I/O:	3	pins
Special function pin	6	pins
Reset input pin (NRST):	1	pin (soft reset is available)
A/D converter reference voltage input pin (VREFH):	1	pin
Capacity connect pin (VOUT18):	1	pin
Function contol pins (MMOD, NOCDMOD, ATRST):	3	pins
Power pins	7	pins
power supply pin(VDD50_1,VDD50_2)	3	pins
GND pins (VSS)	4	pins
Power supply separation		
Pins driven by VDD50_1	68	pins (I/O ports: 62 pins)
Pins driven by VDD50_2	25	pins (I/O ports: 25 pins)

- Power supply voltage

VDD50_1 : 2.2 V to 5.5 V
VDD50_2 : VDD50_1 to 5.5 V

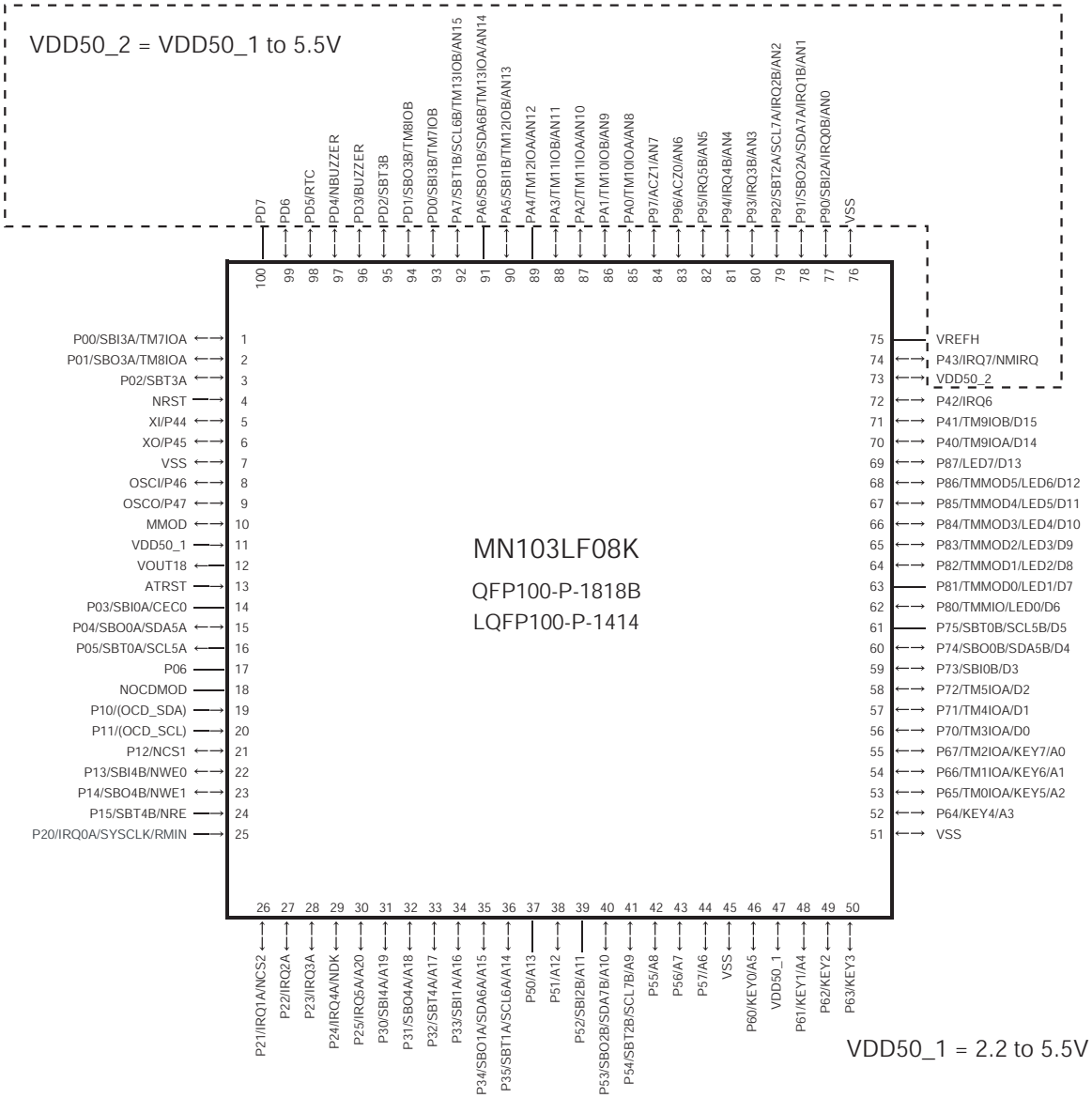
- Operating temperature

–40°C to + 85°C

- Package

QFP100pin (QFP100-P-1818B)
LQFP100pin (LQFP100-P-1414)

■ Pin Description



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