

MN3003

DUAL-64 STAGE BBD FOR LOW VOLTAGE OPERATION

General Description

The MN3003 is a dual 64-stage BBD for low voltage operation ($-9V$) incorporating a clock generator on a single chip. The 64-stage provides a signal delay of up to 3.2msec.

The dual type contains two identical BBD's on a single chip with independent input, output and common clock terminals, as well as common power supply terminals.

The two identical BBD's on the same chip offer uniform characteristics and space saving advantage when they are used in parallel or series connection.

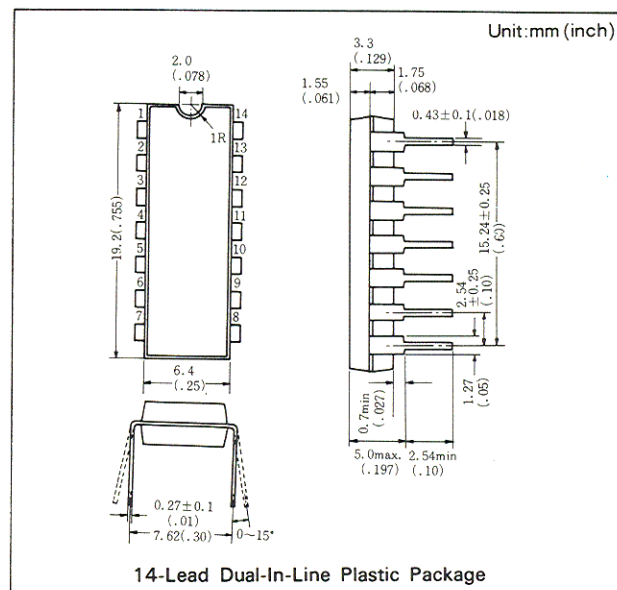
The clock oscillation frequency is controlled by the external resistor and capacitor connected to CG_1 , CG_2 and CG_3 terminals.

Features:

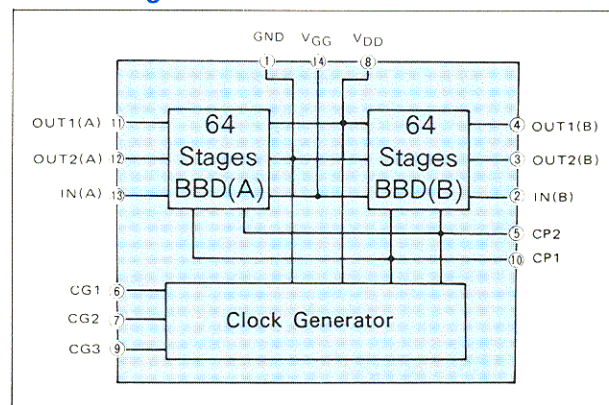
- Variable delay line in audio frequency range:
0.16~3.2msec. (64-stage)
0.32~6.4msec. (64×2-stage)
- Incorporating clock generator circuit.
- Wide frequency response: $f_i \leq 0.3 \times f_{cp}$
- Wide clock frequency range : 10~200kHz
- Wide dynamic range : $S/N=75dB$ typ.
- Low insertion loss : $L_i=3.5dB$ typ.
- Low noise : $V_{no}=0.14mV_{rms}$ max.

Applications:

- Vibrato and/or chorus effects in electronic musical instruments.
- Reverberation effect of electronic musical instruments.
- Variable or fixed delay of analog signals.



Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	$-9, V_{DD} + 1$	V
Signal Delay Time	t_D	0.16 ~ 6.4	msec
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	68min	dB

BBD SERIES MN3003

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Terminal Voltage	$V_{DD}, V_{GG}, V_{CP}, V_i$	$-15 \sim +0.3$	V
Output Voltage	V_o	$-15 \sim +0.3$	V
Operating Temperature	T_{opr}	$-20 \sim +60$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim +125$	$^\circ\text{C}$

Operating Conditions ($T_a=25^\circ\text{C}$)

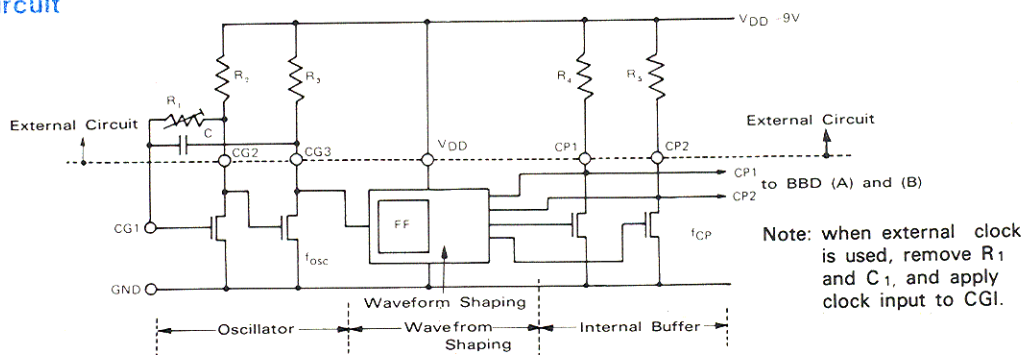
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		-8.5	-9	-9.5	V
Gate Supply Voltage	V_{GG}			$V_{DD} + 1$		V
Clock Voltage "H" Level	V_{CPH}		0		-0.4	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Frequency	f_{CP}		10		200	kHz
Input DC Bias	V_{Bias}		-2.5		-6	V

Electrical Characteristics ($V_{DD}=-9\text{V}$, $V_{GG}=-8\text{V}$, $R_L=100\text{k}\Omega$, $R_2=R_3=22\text{k}\Omega$, $R_4=R_5=2.2\text{k}\Omega$, $C=100\text{pF}$, $f_{CP}=\frac{1}{2}f_{osc}$ (adjustable by R_1), $T_a=25^\circ\text{C}$)

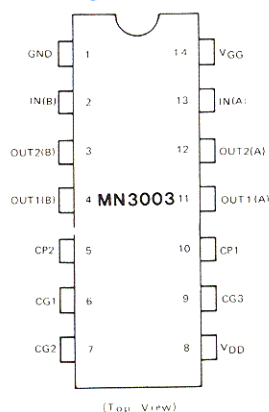
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Signal Frequency	f_i	$f_{CP}=40\text{kHz}$, $V_i=0.8\text{Vrms}$ 3dB down (0dB at $f_i=1\text{kHz}$)			12	kHz
Input Signal Swing	V_i	$f_{CP}=40\text{kHz}$, $f_i=1\text{kHz}$, $\text{THD}=2.5\%$			0.8	Vrms
Insertion Loss	L_i	$f_{CP}=40\text{kHz}$, $f_i=1\text{kHz}$, $V_i=0.8\text{Vrms}$		3.5	7	dB
Total Harmonic Distortion	THD	$f_{CP}=40\text{kHz}$, $f_i=1\text{kHz}$, $V_i=0.5\text{Vrms}$		0.5		%
Noise Voltage	V_{no}	$f_{CP}=90\text{kHz}$, Weighted by "A" curve			0.14	mVrms
Signal to Noise Ratio	S/N		68			dB

Note: Adjust input DC bias to the optimum value between -2.5 and -6 volts.

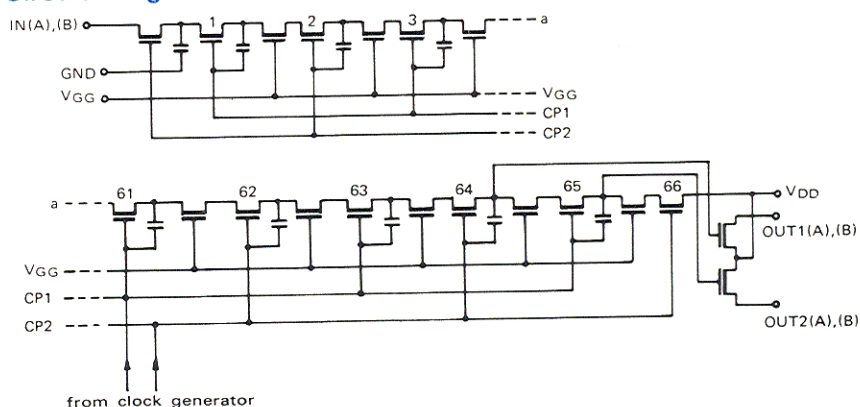
Clock Generator Circuit



Terminal Assignments

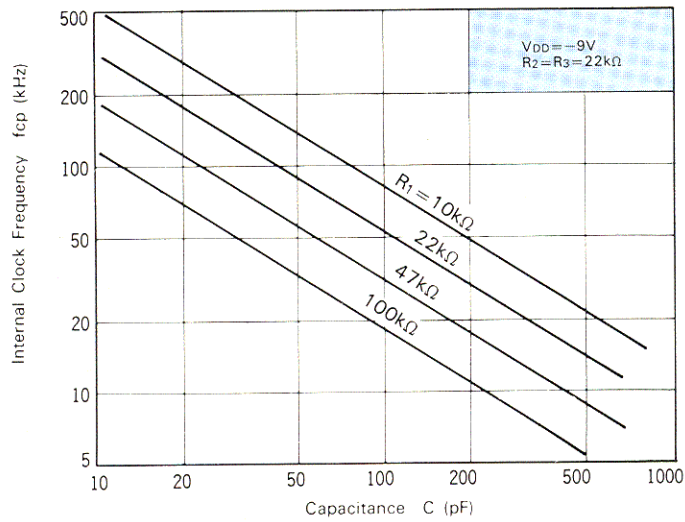
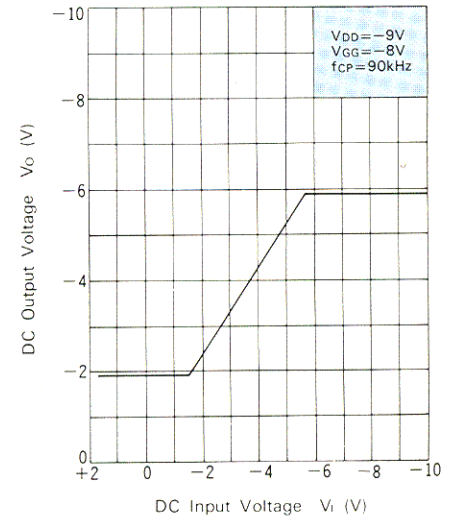
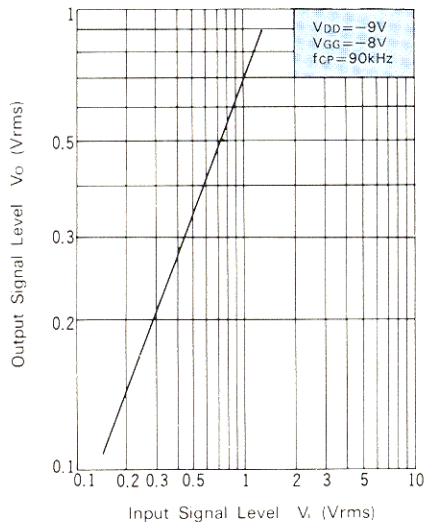
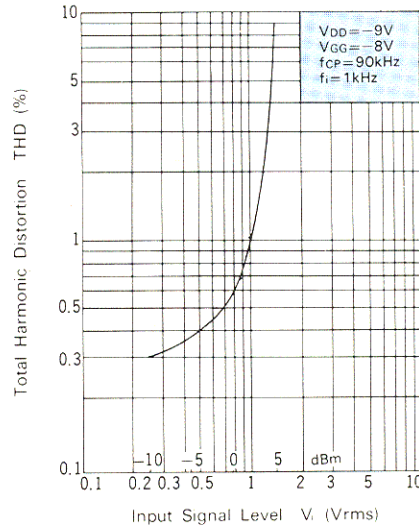
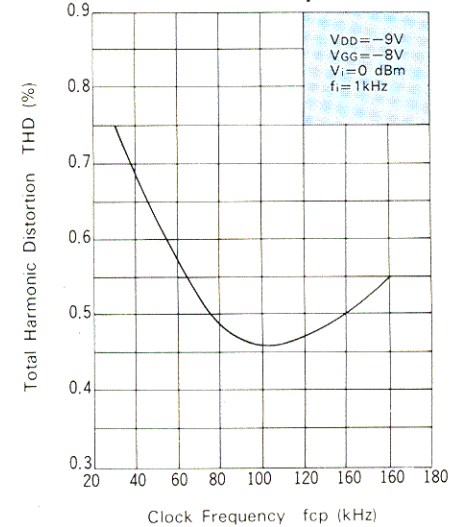
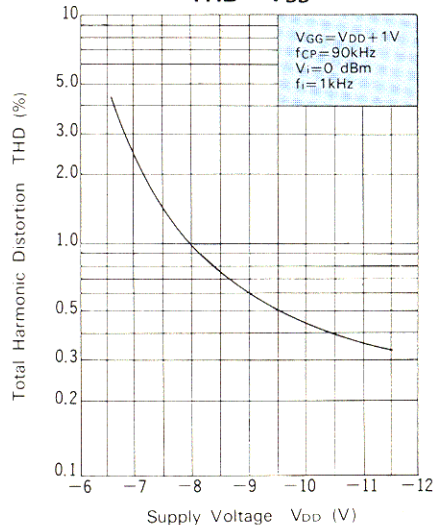
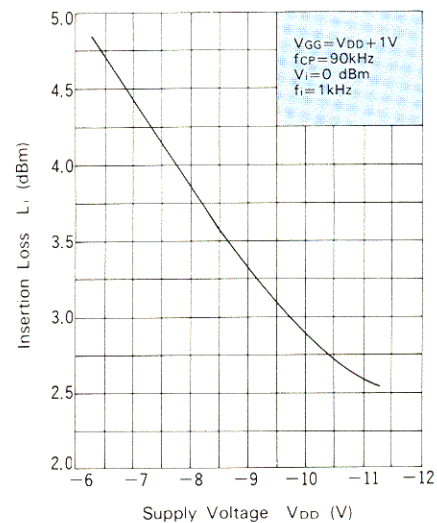
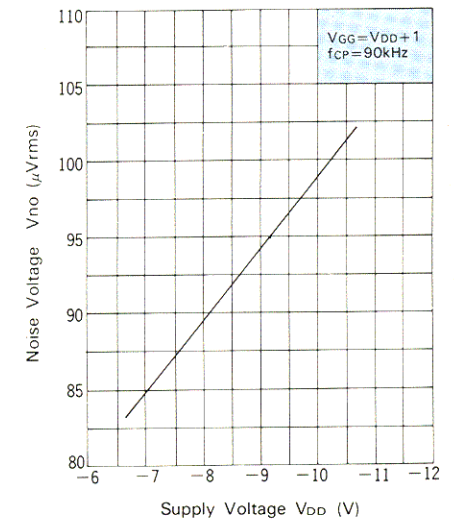


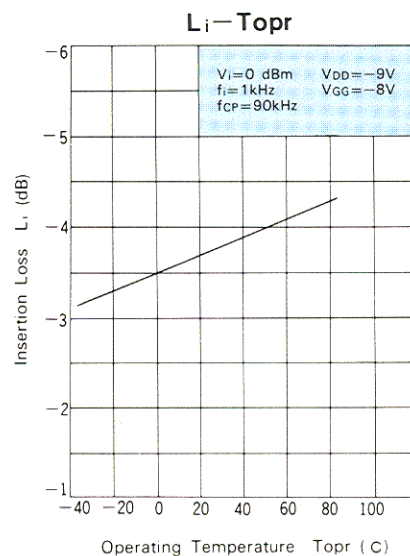
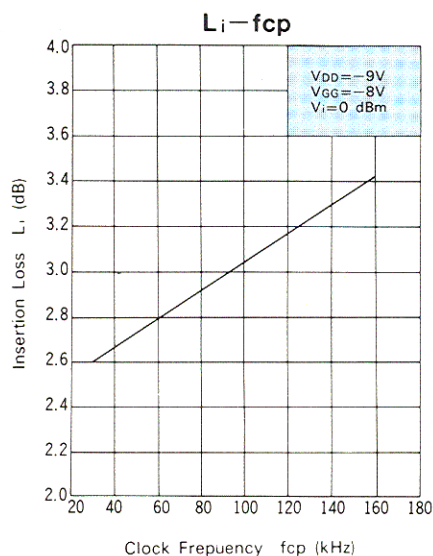
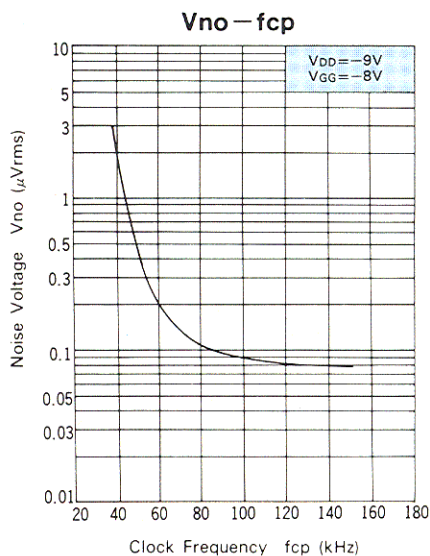
Circuit Diagram



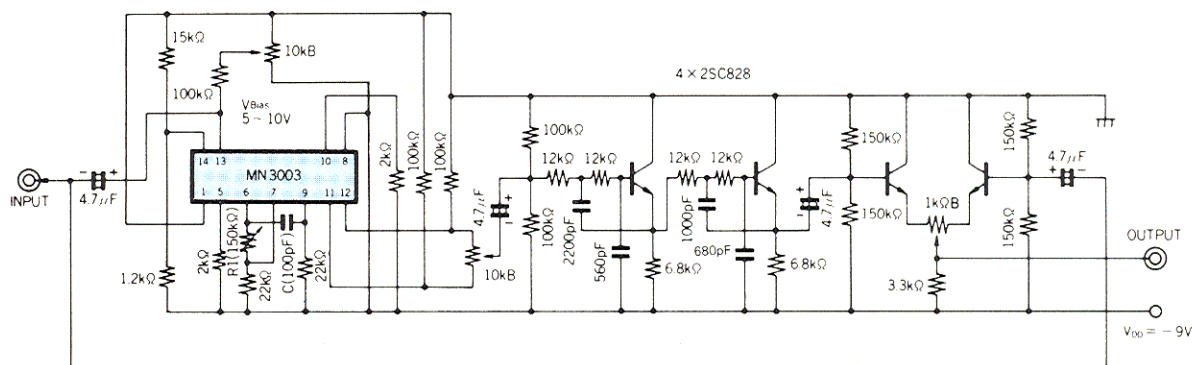
Typical Electrical Characteristic Curves

Clock Frequency Characteristics

 $V_O - V_I$  $V_O - V_I$ THD - V_i THD - f_{cp} THD - V_{DD}  $L_i - V_{DD}$  $V_{no} - V_{DD}$ 



Application Circuit



Chorus Effect Generation Circuit (Incorporating Clock Generator)