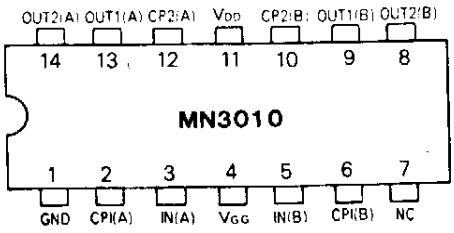
Terminal Assignments



filespec. **Computer-ese for file specification and the heading for our continuing series dedicated to component information. *filespec*'s purpose is to give you a database from which to do your own experimentation. This page is designed to be photocopied, punched and filed. If you need further information on anything mentioned in *filespec*, drop us a line. We'll be glad to help you out.**

In this installment Dave gives us the rundown on another of the Matsushita delay lines the MN3010. Dave will be making the majority of the components covered in this series available through E-Systems, P.O. Box 5305, Berkeley, CA 94710. Write for his price list.

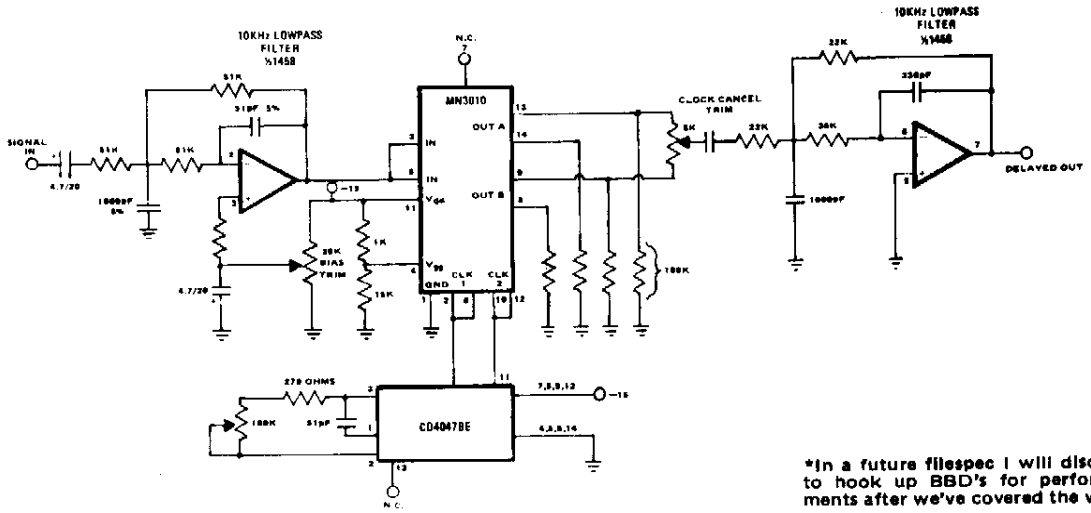
filespec:MN3010

The Matsuchita MN3010 is a dual 512-stage Bucket Brigade Device (BBD) with a useable delay range from 0.3 msec (at f_{cp} = 850KHz) to 32 msec (at f_{cp} = 8KHz). Because of its delay range it is an excellent choice for flanging and chorus effects. When used in a parallel multiplex configuration*, as shown in the schematic below, the best signal-to-noise ratio of all available BBDs (Reticon SAD-1024 included) can be achieved. As with most P-MOS BBDs, the frequency response falls short of full audio bandwidth (15KHZ), but this can be overcome with a little pre-emphasis.

There is a DC bias level shift at the output which is clock frequency dependent and becomes noticeable at around 350KHz and above.

The capacitance of the clock lines is not so high that the CMOS 4047 will not drive it sufficiently. (Although MOS clock drivers would enhance the performance.) Please note that the P-MOS BBD runs off −15V, so that the 4047 must also run off the −15 and ground. All the capacitors below are .01mfd in value and the resistors all have a 5% tolerance.

—Dave



*In a future filespec I will discuss various ways to hook up BBD's for performance enhancements after we've covered the various types. *DT*

	MIN	TYP	MAX	UNIT
Drain Supply Voltage, V_{dd}	−14	−15	−18	V
Gate Supply Voltage, V_{gg}	–	V_{dd}^{+1}	–	V
Clock Frequency, f_{cp}	8	–	850	kHz
Input Signal Frequency [f_{cp} = 40 kHz, V_i @ 1.8 V_{rms}, −3dB point with 0dB ref @ f_i = 1kHz]	–	–	14	kHz
Input Signal Swing, V_i	–	–	1.8	V_{rms}
Insertion Loss [f_{cp} = 40 kHz, f_i = 1kHz]	–	0	–	dB
Total Harmonic Distortion, THD [f_{cp} = 100kHz, "A" weighted]	–	0.4	–	%
Signal to Noise Ratio, S/N	–	85	–	dB