MN3011

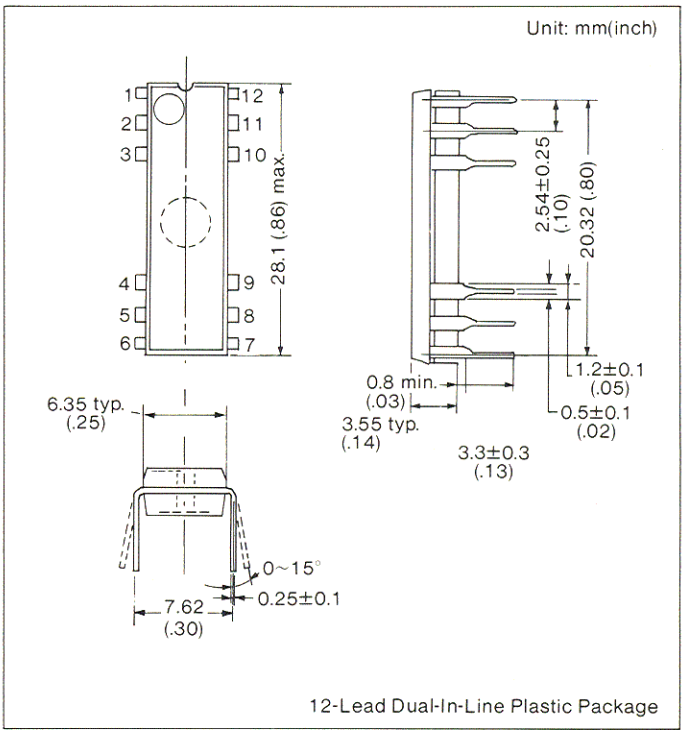
3328 - Stage Multi-Tap BBD (MN3011) for Audio Signal Delays

General Description

The MN3011 is a 3328-stage low noise BBD (Bucket Brigade Device) designed to provide simultaneously six different delay outputs with respect to a signal input. A proper mixing of the six differently delayed signals generates highly effective reverberation. The delay times can be varied by the clock frequency control.

Features

- 3328-stage with 6 different output stages
- 6 stages not in multiple proportion with each other so that a proper mixing of the six differently delayed output signals generates a highly effective reverberation.
- Clock component cancellation capability.
- Wide dynamic range: S/N ≥ 76 dB typ.
- No insertion loss: Li = 0 dB typ.
- Total harmonic distortion: THD = 0.4% typ.
- P-channel silicon gate, tetrode MOS transistors configuration

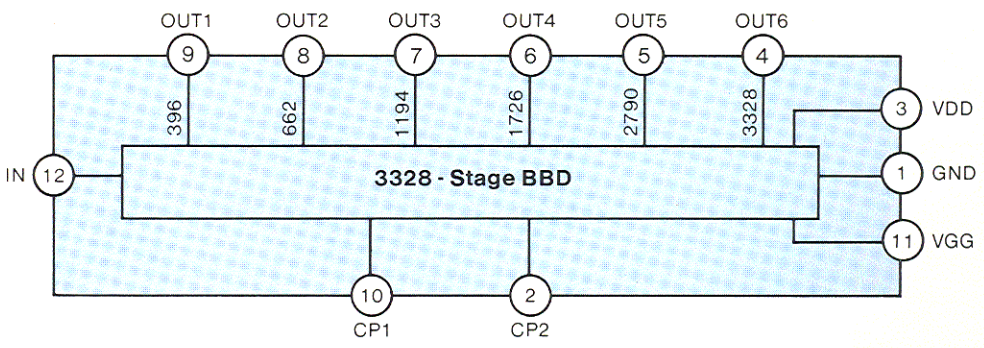


12-Lead Dual-In-Line Plastic Package

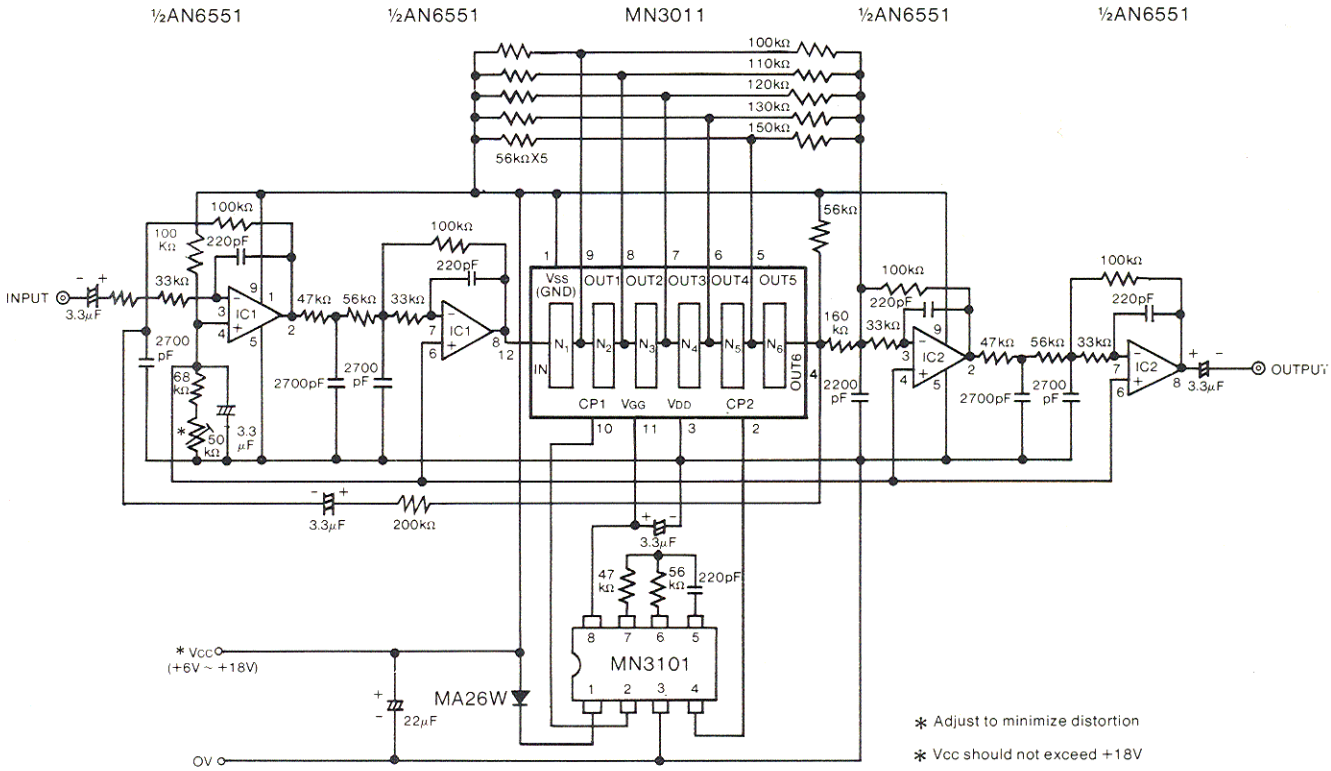
Maximum Delay Times for 6 Different Output Stages

Tapped Output Terminals	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	Remark
BBD stages (stages)	396	662	1194	1726	2790	3328	
Maximum Delay Time (msec.)	19.8	33.1	59.7	86.3	139.5	166.4	Clock 10KHz

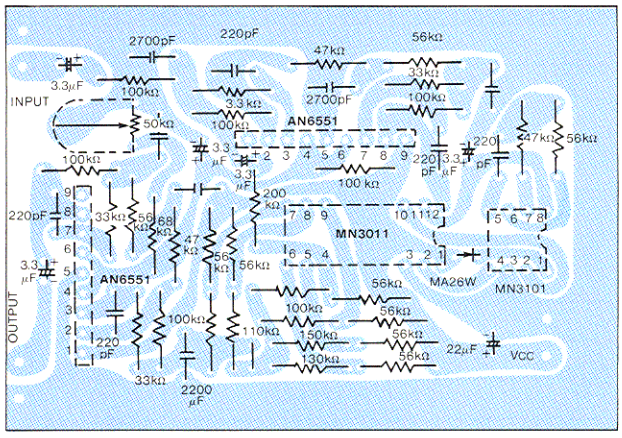
Block Diagram



Application Circuit – Reverberation Effect Generation Circuit



Printed Circuit Board Layout
(Actual Size)



Electrical Characteristics of The Application Circuit
(Vcc = +15V, Ta = 25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Current	Icc			11(8)	15(10)	mA
Total Power Dissipation	Ptot			165 (70)		mW
Signal Delay Time	t_D	OUT6: f_{CP} = 15~20kHz	83	98	111	msec
Cutoff Frequency	f_{CO}			3		kHz
Input Signal Swing	V_i	THD = 2.5%			1.1(0.5)	Vrms
Insertion Loss	L_i	OUT3: f_i = 1kHz V_i = 300mV	0	2	4	dB
Total Harmonic Distortion	THD	f_i = 1kHz V_i V_i(max) –6dB		0.4 (0.5)		%
Output Noise Voltage	Vno	OUT3: V_i = 0V		0.4 (0.4)		mVrms
Signal to Noise Ratio	S/N	$V_S = V_i$(max)		70 (60)		dB

Note: Values in parenthesis for Vcc = +9V.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	VO	−18~+0.3	V
Operating Temperature	Topr	−20~+70	°C
Storage Temperature	Tstg	−55~+125	°C

Note: All voltages with respect to GND = 0V.

Operating Conditions (Ta = 25°C)

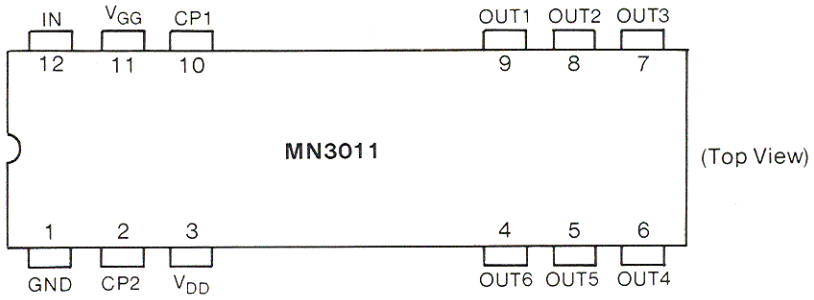
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	VDD	−14	−15	−16	V
Gate Supply Voltage	VGG		VDD + 1		V
Clock Voltage "H" Level	VCPH	0		−1.3	V
Clock Voltage "L" Level	VCPL		VDD		V
Clock Input Capacitance	CCP			2300	pF
Clock Frequency	fcp	10		100	kHz
Clock Pulse Width	tcpw			0.5T *	
Clock Rise Time	tcpr			500	nsec
Clock Fall Time	tcpf			500	nsec

*$T = 1/f_{cp}$

Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 56K\Omega$)

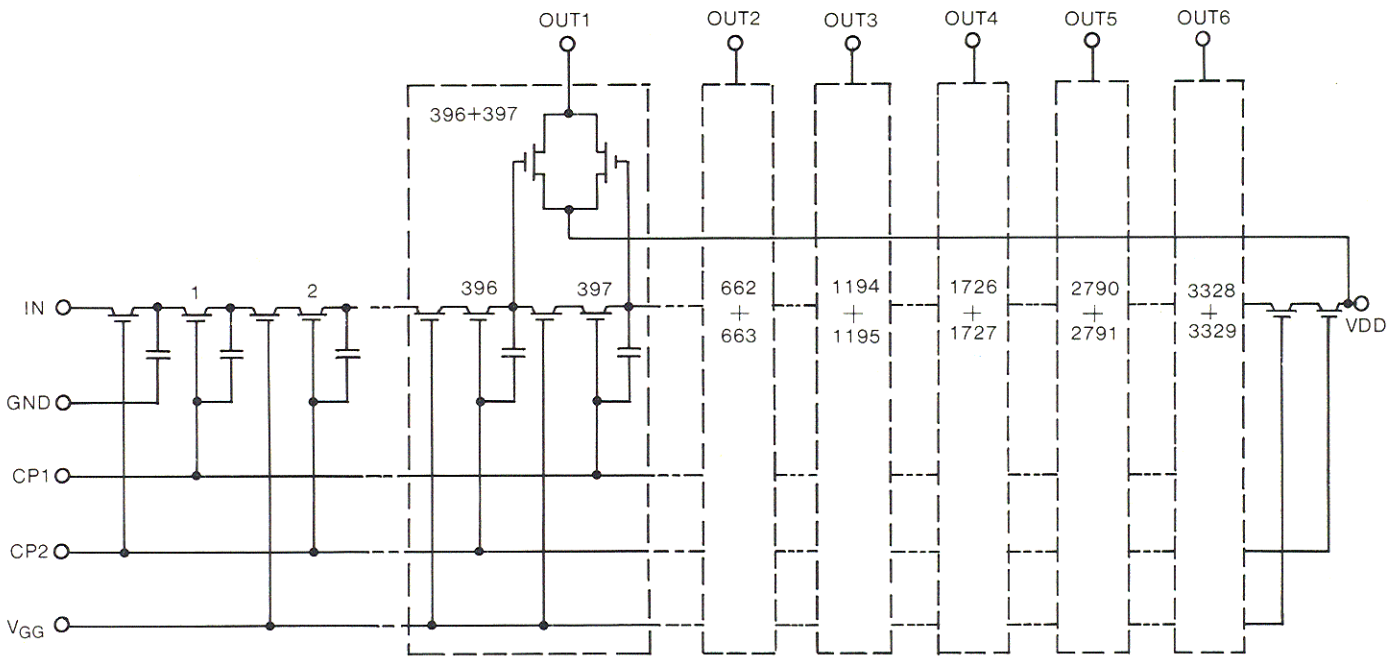
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time						
Terminal OUT1	tD1	fcp = 10kHz~100kHz	1.98		19.8	msec
Terminal OUT2	tD2		3.31		33.1	msec
Terminal OUT3	tD3		5.97		59.7	msec
Terminal OUT4	tD4		8.63		86.3	msec
Terminal OUT5	tD5		13.95		139.5	msec
Terminal OUT6	tD6		16.64		166.4	msec
Input Signal Frequency	fi	fcp = 40kHz − 3dB			11	kHz
Input Signal Swing	Vi	THD = 2.5%			1.1	Vrms
Insertion Loss	Li	fcp = 40kHz, fi = 1kHz,		0		dB
Total Harmonic Distortion	THD	fcp = 40kHz. fi = 1kHz. Vi = 0.78Vrms		0.4		%
Noise Level						
OUT1, OUT2, OUT3	Vno1	fcp = 100KHz Weighted by "A" curve			270	μVrms
OUT4, OUT5, OUT6	Vno2				400	μVrms
Signal to Noise Ratio						
OUT1, OUT2, OUT3	S/N1	fcp = 100kHz Weighted by "A" curve		80		dB
OUT4, OUT5, OUT6	S/N2	Maximum output voltage to noise voltage		76		dB

Terminal Assignments

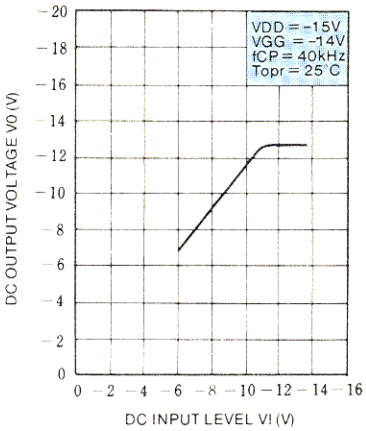


Pin No.	Symbol	Terminal	Functions
1	GND	Grounding	Ground connection
2	CP2	Clock Input 2	Fundamental clock pulse input for charge transfer
3	V_{DD}	V_{DD} Supply	−15V supply
4	OUT6	Output 6	3328th and 3329th stage synthetic output with clock component cancellation
5	OUT5	Output 5	2790th and 2791st stage synthetic output
6	OUT4	Output 4	1726th and 1727th stage synthetic output
7	OUT3	Output 3	1194th and 1195th stage synthetic output
8	OUT2	Output 2	662nd and 663rd stage synthetic output
9	OUT1	Output 1	396th and 397th stage synthetic output
10	CP1	Clock Input 1	Fundamental clock pulse input, inverted with respect to CP2
11	V_{GG}	V_{DD} Supply	V_{GG} bias supply input to each MOS transistor gate connected in series with BBD transfer gates $V_{GG} = V_{DD} + 1$
12	IN	Signal Input	Analog signal input The optimum DC bias must be applied to this terminal

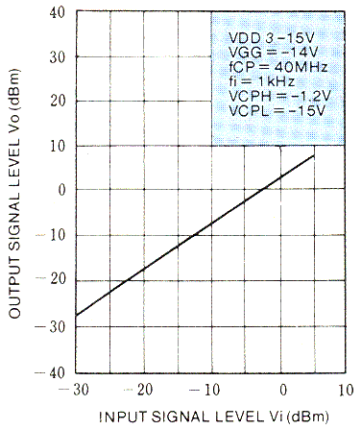
Circuit Diagram



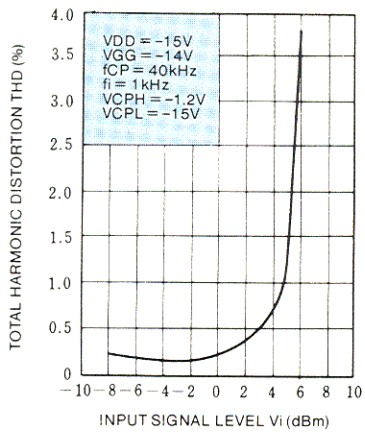
Vo – VI



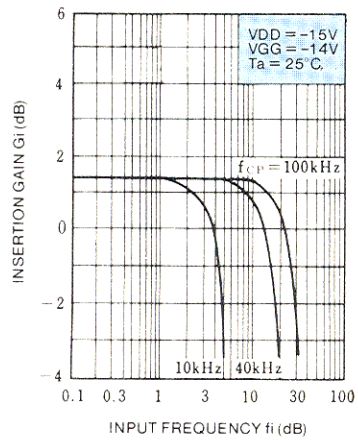
Vo – Vi



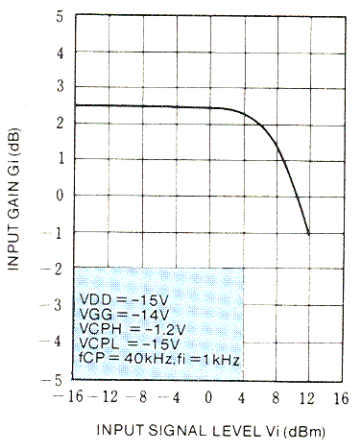
THD – Vi



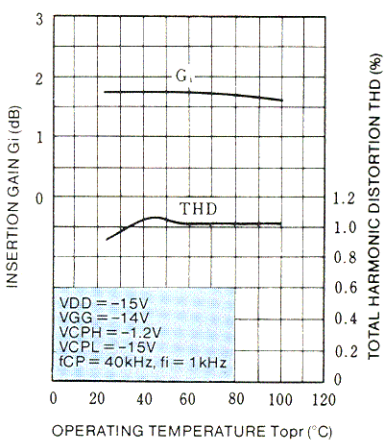
Gi – fi



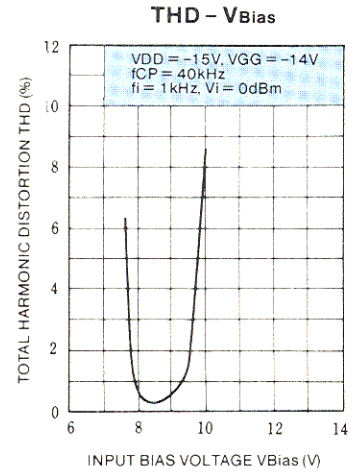
Gi – Vi



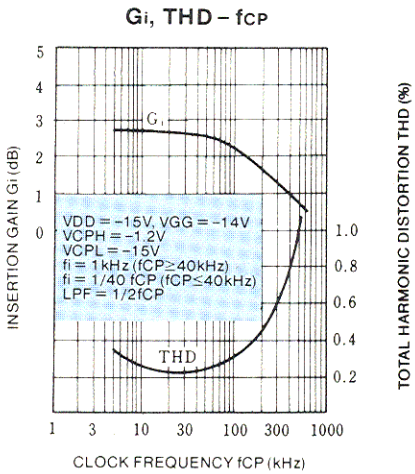
Gi, THD – Topr



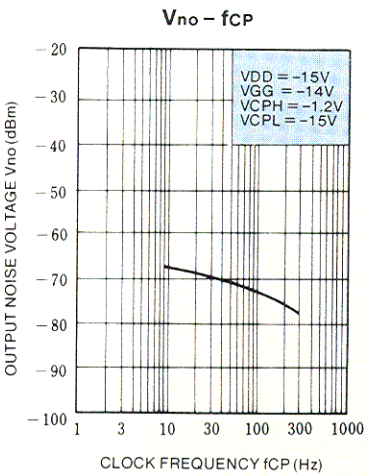
THD – VBias



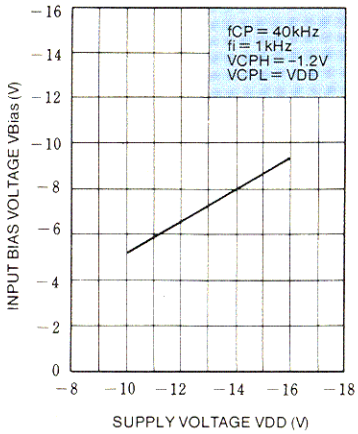
Gi, THD – fCP



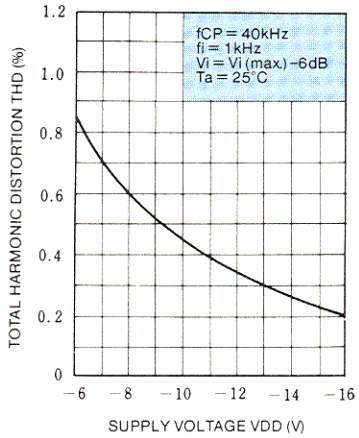
Vno – fCP



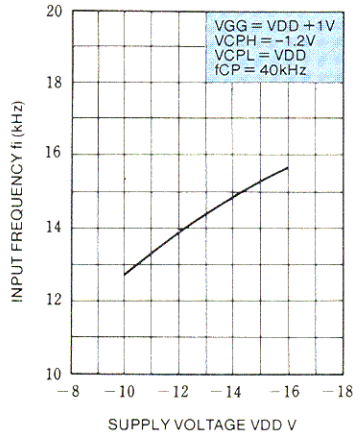
VBias – VDD



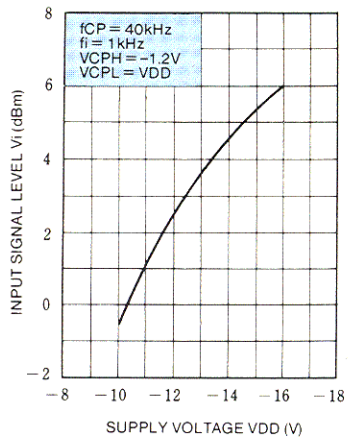
THD – VDD



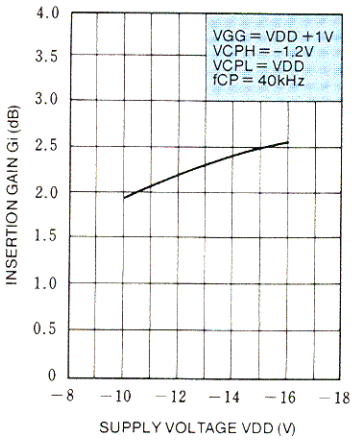
fi – VDD



Vi – VDD



Gi – VDD



S/N, Vno – VDD