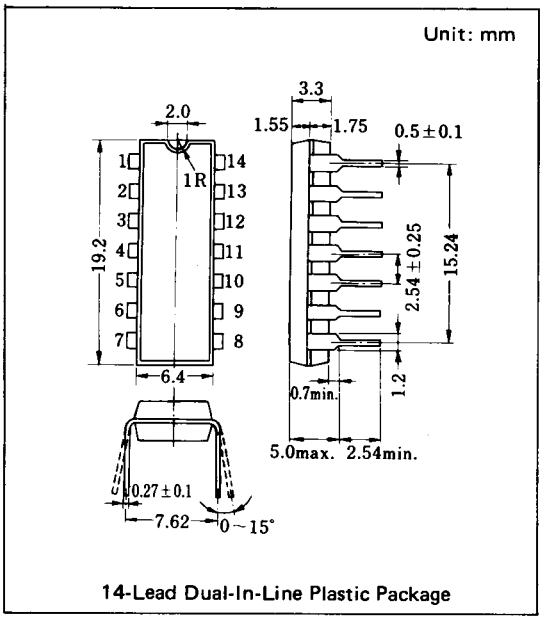
MN3214

1024-STAGE LOW VOLTAGE OPERATION BBD WITH 5 TAPS

■ General description

The MN3214 is a 1024-stage BBD with 5 taps particularly suitable as a device for generation of reverberation effect of audio equipments such as low voltage operation stereo equipments and radio cassette recorders, etc.

Sinal with different delay time is output from 5 tap outputs against the input signal. Natural reverberation effect can easily be realized by mixing these output signals properly, and also delay time can be freely changed by changing the clock frequency.



14-Lead Dual-In-Line Plastic Package

■ Features

- Audio signal delay device with 5 output taps and 1024-stage.
- Stage of each output tap has no relation to multiple, therefore, natural reverberation effect can be obtained by mixing these output signals.
- Clock component cancellation circuit.
- Wide dynamic range: S/N ≧ 73dB type.
- No insertion loss: L_i = 0dB typ.
- Low distortion: THD = 0.4% typ. (V_i = 0.25Vrms).
- Supply voltage range: 4 ~ 10V.
- N-channel silicon gate process.
- 14-lead dual-in-line plastic package.

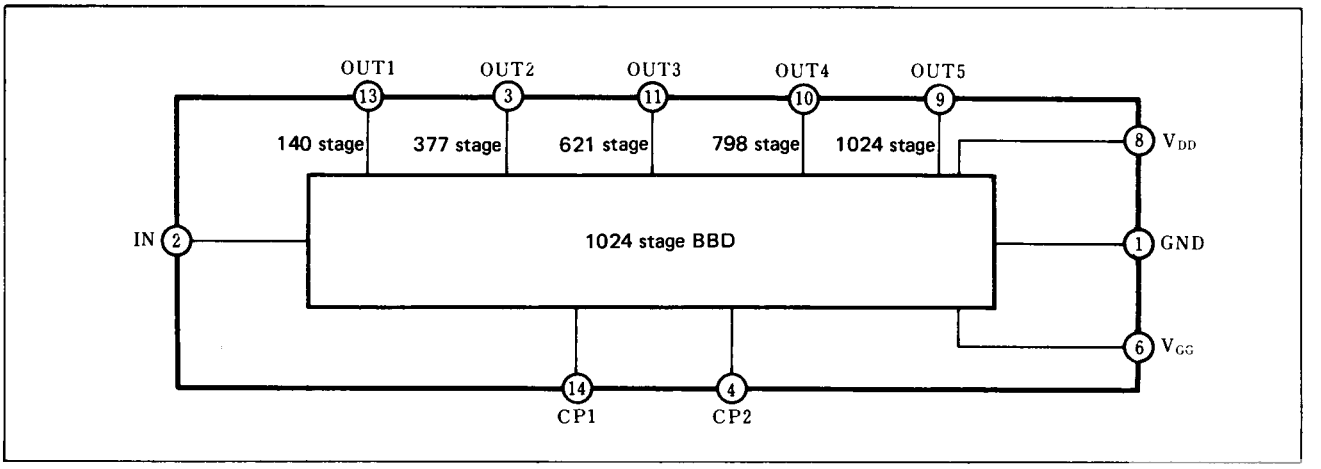
Applications

- Reverberation effect of audio equipments.
- Sound effect in electronic musical instruments.

■ Maximum Delay Time by Tap Output

Terminal of the Tap Output	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	Remarks
Stages of BBD (Stage)	140	377	621	798	1024	
Maximum Delay Time (mS)	7.0	18.85	31.05	39.9	51.2	at clock frequency 10KHz

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Input Output	V_{DD}, V_{GG}	−0.3~+11	V
Terminal Voltage	V_I, V_{CP}, V_O	−0.3~+11	V
Operating Temperature	Topr	−20~+60	℃
Storage temper	Tstg	−55~+125	℃

■ Operating Condition (Ta = 25°C)

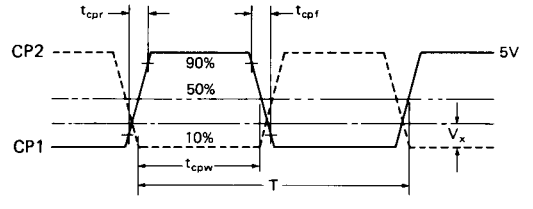
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}			+5		V
Gate Supply Voltage	V_{GG}			$\frac{14}{15}V_{CPH}$		V
Clock Voltage "H" Level	V_{CPH}			V_{DD}		V
Clock Voltage "L" Level	V_{CPL}		0		+1	V
Clock Frequency	f_{CP}		10		200	kHz
Clock Pulse Width Duty Ratio*1	t_{CPW}				0.5T *2	%
Clock Rise Time *1	t_{CPr}				500	ns
Clock Fall Time *1	t_{CPf}				500	ns
Clock Input Capacitance	C_{CP}				700	pF
Clock Cross Point *1	V_X		0		$0.3V_{CPH}$	V

■ Electrical Characteristics

(Ta = 25°C, $V_{DD} = V_{CPH} = 5V$, $V_{CPL} = 0V$, $V_{GG} = 4.67V$, $R_L = 56k\Omega$, LPF $f_c = 20kHz$, Att = 48dB/oct)

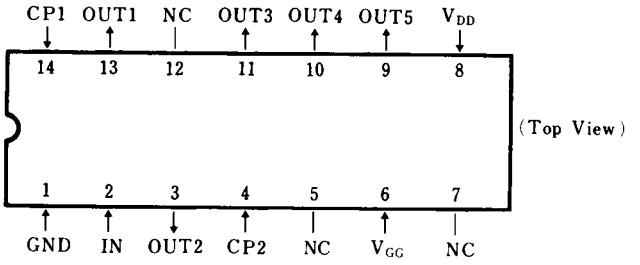
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time							
	OUT 1 Terminal	$t_{D(1)}$	f_{CP}=10kHz~200kHz	0.35		7.0	ms
	OUT 2 Terminal	$t_{D(2)}$		0.9425		18.85	ms
	OUT 3 Terminal	$t_{D(3)}$		1.5525		31.05	ms
	OUT 4 Terminal	$t_{D(4)}$		1.995		39.9	ms
	OUT 5 Terminal	$t_{D(5)}$		2.56		51.2	ms
Input Signal Frequency		f_i	f_{cp} = 40kHz, Output −3dB	10			kHz
Input Signal Swing		V_i	THD=2.5%	0.36			Vrms
Insertion Loss		L_i	f_{CP}=40kHz, f_i=1kHz	−4	0	4	dB
Total Harmonic Distortion		THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.25Vrms		0.4	2.5	%
Output Noise Voltage		V_{no}	f_{cp} = 100kHz, Weighted by "A" curve			0.2	mVrms

*1 Clock Pulse Waveforms



*2 $T = 1/f_{CP}$ (Clock Period)

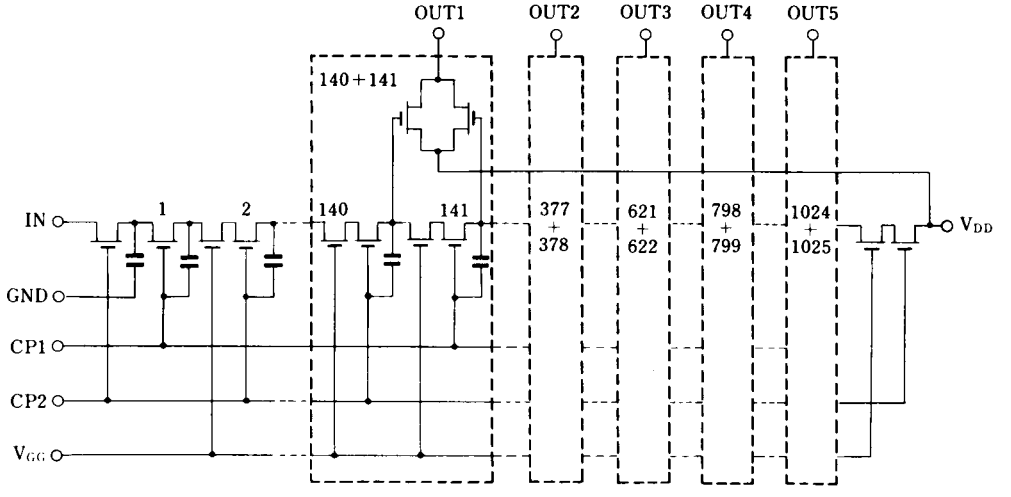
■ Terminal Assignments



■ Terminal Description

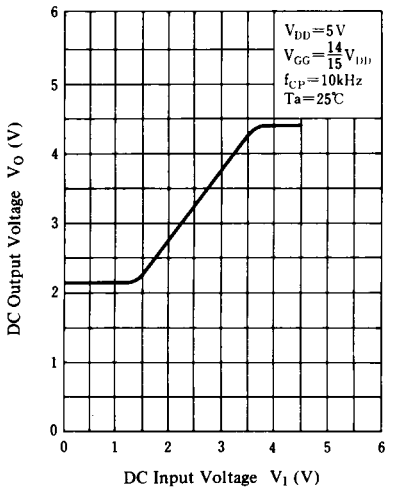
Terminal No.	Symbol	Terminal Name	Description
1	GND	GND terminal	Connected to the GND of circuit.
2	IN	Signal input terminal	Analog signal to be delayed is input. Most suitable DC bias should be applied to this terminal.
3	OUT 2	Output terminal 2	Composed output of 377th and 378th stage are output.
4	CP 2	Clock input 2	Basic clock pulse is applied to transfer electron of BBD.
5	NC	No connection	
6	V_{GG}	V_{DD} apply terminal	Bias of V_{GG} = 14/15V_{DD} is applied to the gate of MOS transistor which is inserted in series with transfer gate of the BBD.
7	NC	No connection	
8	V_{DD}	V_{DD} apply terminal	4 ~ 10V is applied.
9	OUT 5	Output terminal 5	Composed output of 1024th and 1025th stage are output.
10	OUT 4	Output terminal 4	Composed output of 798th and 799th stage are obtained.
11	OUT 3	Output terminal 3	Composed output of 621st and 622nd stage are obtained.
12	NC	No connection	
13	OUT 1	Output terminal 1	Composed output of 140th and 141st stage are obtained.
14	CP 1	Clock input 1	Clock pulse of reverse phase to CP2 is applied.

■ CIRCUIT DIAGRAM

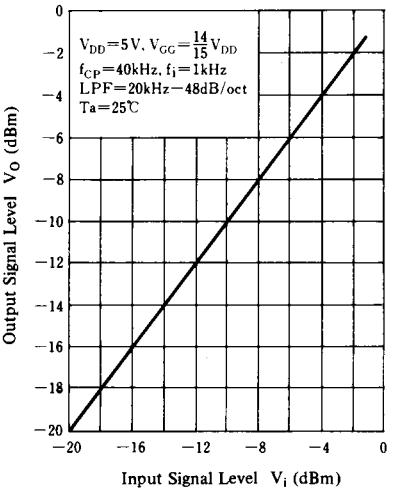


■ Typical Electrical Characteristic Curves

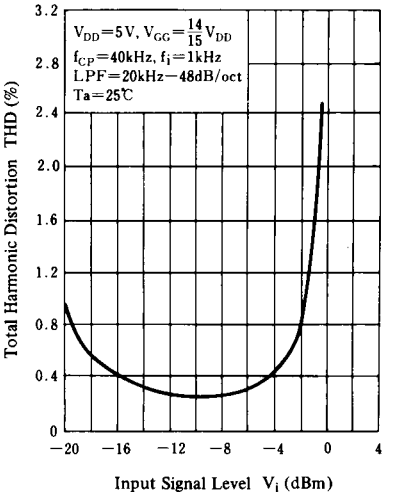
$V_O - V_I$



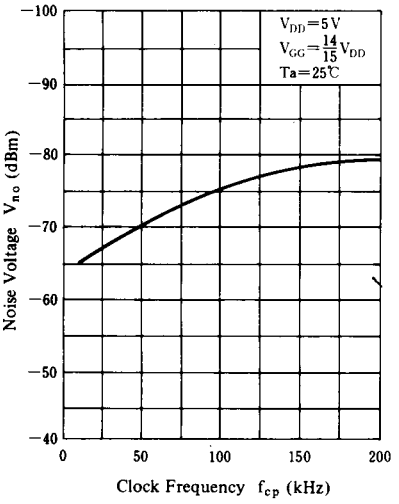
$V_o - V_i$



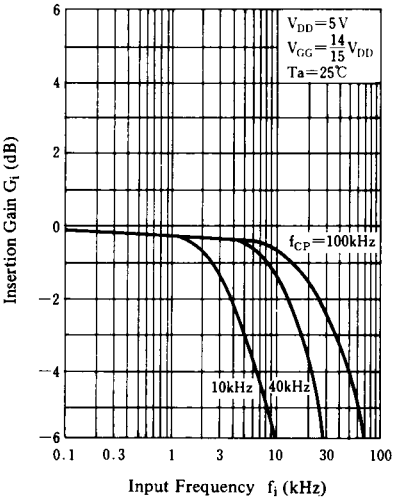
THD − V_i



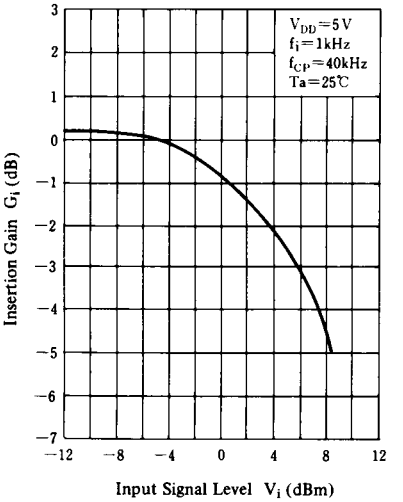
$V_{no} - f_{CP}$



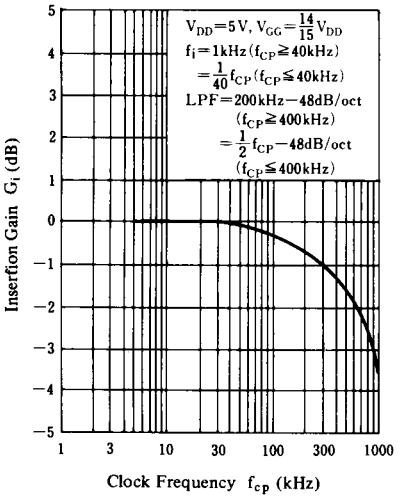
$G_i - f_i$



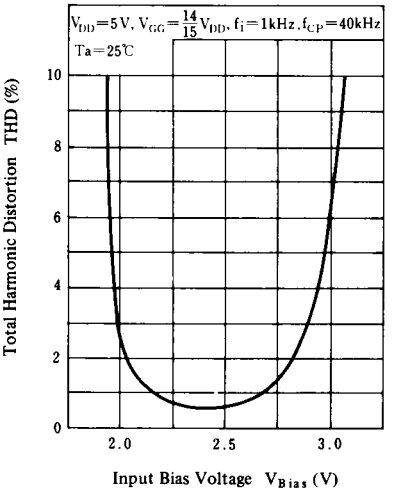
$G_i - V_i$



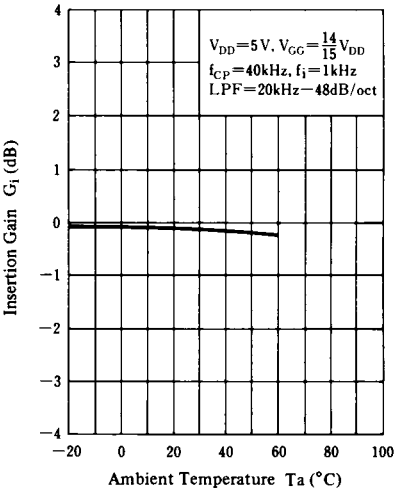
$G_i - f_{CP}$



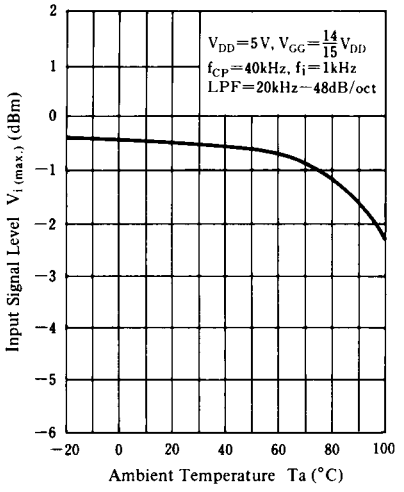
THD − V_{Bias}



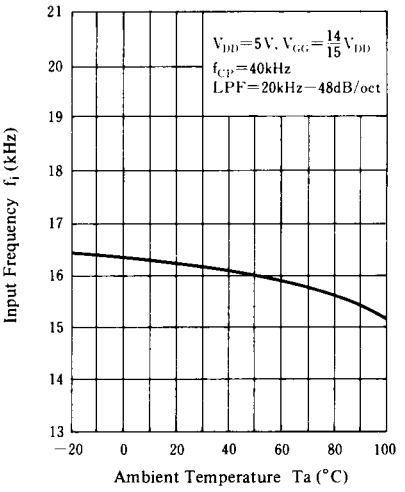
G_i − Ta



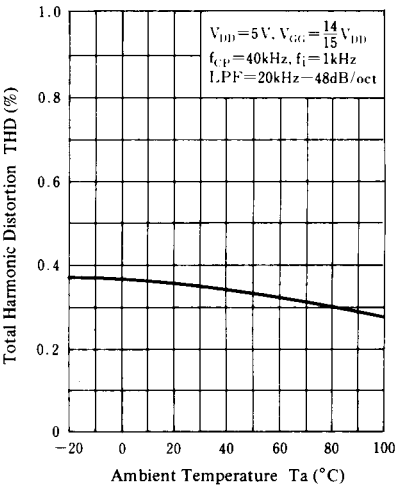
$V_{i(max.)}$ — Ta



f_i — Ta

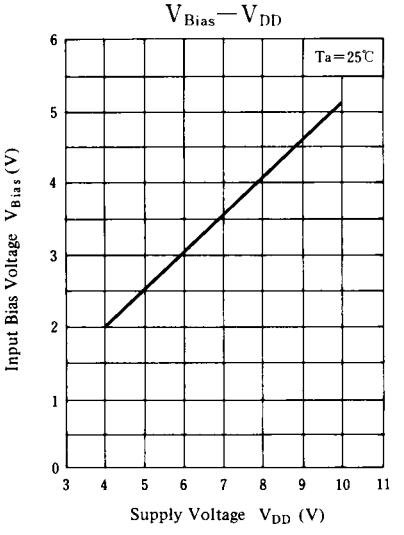


THD — Ta

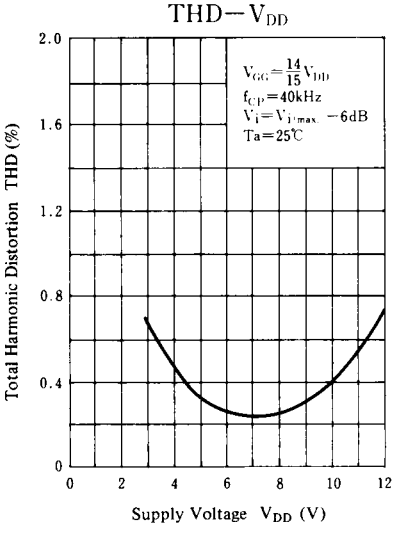


■ Supply Voltage Characteristics

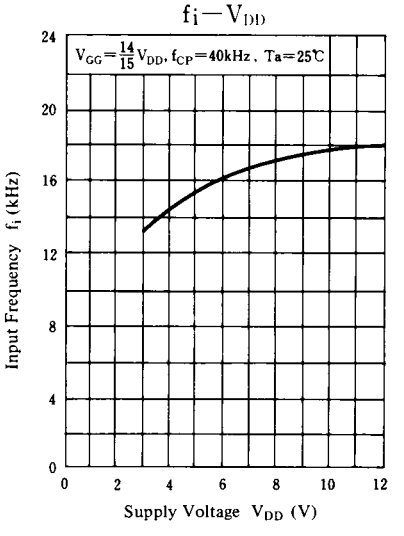
V_{Bias} — V_{DD}



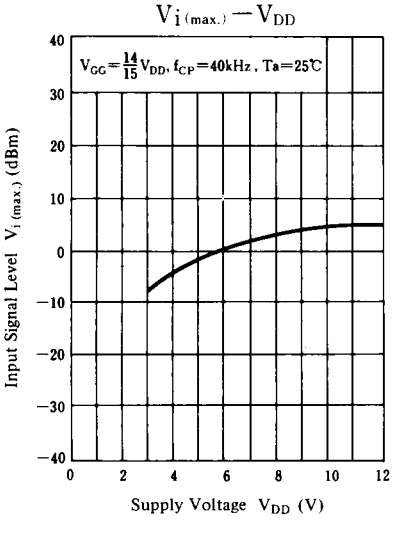
THD — V_{DD}



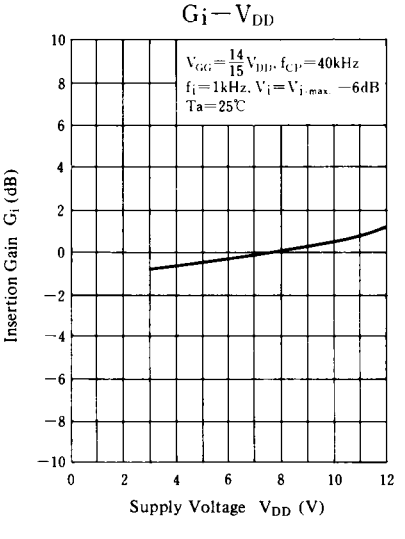
f_i — V_{DD}



$V_{i(max.)}$ — V_{DD}



G_i — V_{DD}



S/N — V_{DD}