1.1 Product Summary

■ Outline

This is a MOS-type sensor of 1/3 type offering 2.1 mega pixels. This product consists of embedded photodiode, pixel block by MOS transistor, column AD converter, built-in timing generator (TG), high speed serial output I/F and functional circuits of various kinds. High definition 12-bit digital image signals offering 2.1 mega pixels are obtained with high speed of 60 fps and with low power consumption.

■ Feature

Features of this MOS type image sensor are follows.

Table 1.1.1 List of Features

Item	Description
Scan mode	progressive scan
Optical size	1/3 type (inch)
Number of active pixels	1944 (H) × 1092 (V) = 2,122,848 (pixel)
Total number of pixels	2010 (H) × 1108 (V) = 2,227,080 (pixel)
Pixel size	2.75 (H)μm × 2.75 (V)μm
Number of pins	104 Pins（including pins of “NC”）
Actual imaging area dimensions (active pixel area)	5.346 (H)mm × 3.003 (V)mm
Color filter arrangement	Bayer arrangement of primary colors: R, G, B
Power supply voltage	3.3V / 1.8V / 1.2V
Master clock	27 MHz / 37.125MHz
Bit number of internal ADC	12 bit
Output signal type	subLVDS DDR method 486Mbps(MCLK=27MHz) 445.5Mbps (MCLK=37.125MHz)
Register I / F	3-lines Serial I/F
Output frame rate per second (Full scan)	2ch 2port 12bit : 60fps 2ch 2port 16bit : 30fps ※1
Electronic shutter (Full scan)	60fps: 1 / 60s ~ 1 / 67500s (1 / 67500s step)
Variable gain（Column amplifier）	Full scan：Standard +0/+6/+12dB
Variable gain (Analog)	Full scan：0dB/6dB
Variable digital gain（Digital processing）	0dB ～ 12dB
Functions	Full scan mode:2.1Mpixel output
	Flip ※2
	Long exposure mode

※ 1 This drive mode is available in chip set with Panasonic DSP (MN2PS00003RF) only.

2 Apply mirror function in DSP.

■ Application

This product is ideal for the field of security camera, network camera, broadcasting camera and industrial camera.

■ Element Configuration

The block configuration and pixel array of this product are described below.

Block configuration

This product consists of pixel block, high speed serial I/F, LVDS output, PLL, Timing generator (TG), Parallel column AD converter and functional circuits of various kinds.

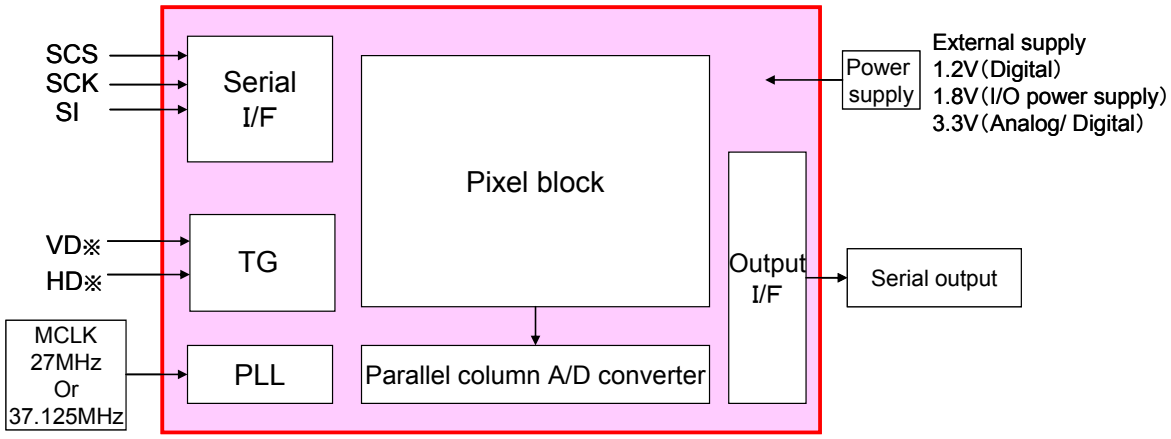


Figure 1.1.1 Block Diagram

※ In sensor slave mode, VD and HD are external input.
In sensor master mode, make these terminals open.

■ Pixel Array Format

Pixel array format is described below.

A1 pin (Upper left)

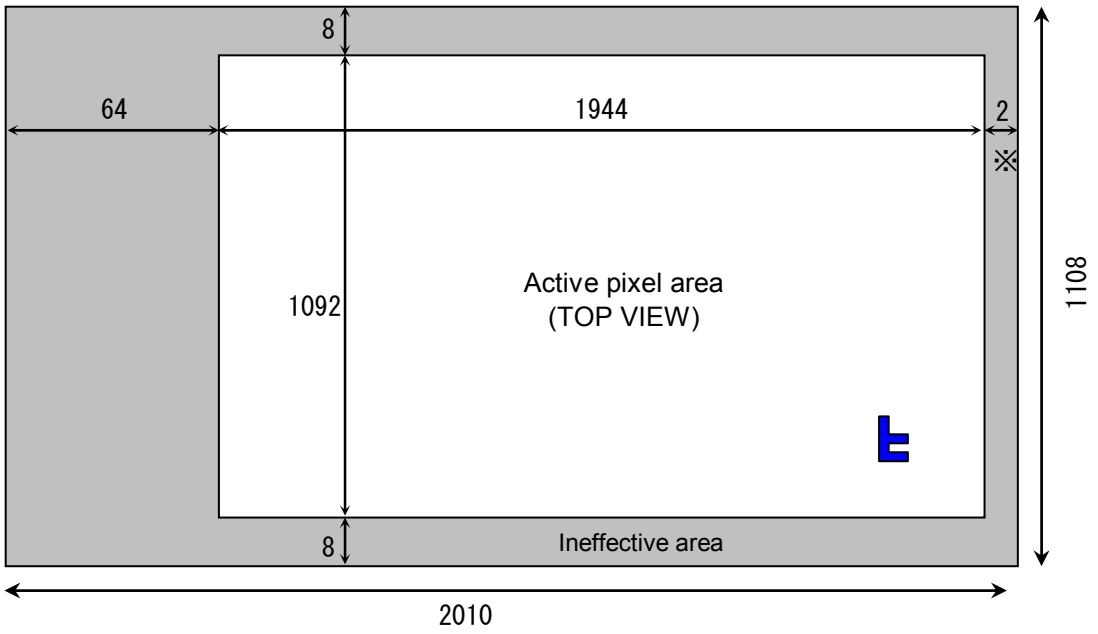


Figure 1.1.2 Pixel Array Configuration

※ In physical pixel array configuration （2010H）, 2 lines of right side are ineffective area.

In LVDS output (2016H), it includes dummy (6 lines) as ineffective data. Totally 8 lines of ineffective data is output. (Refer to the following figure)

＜Reference＞

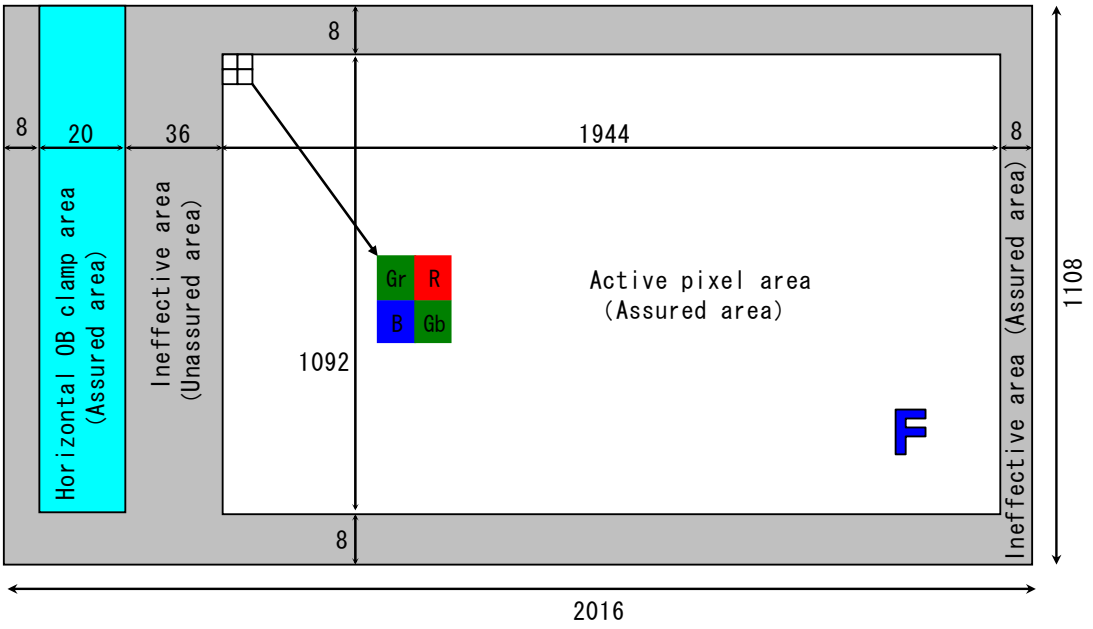


Figure 1.1.3 Pixel Array Configuration（LVDS output）

■ Pins

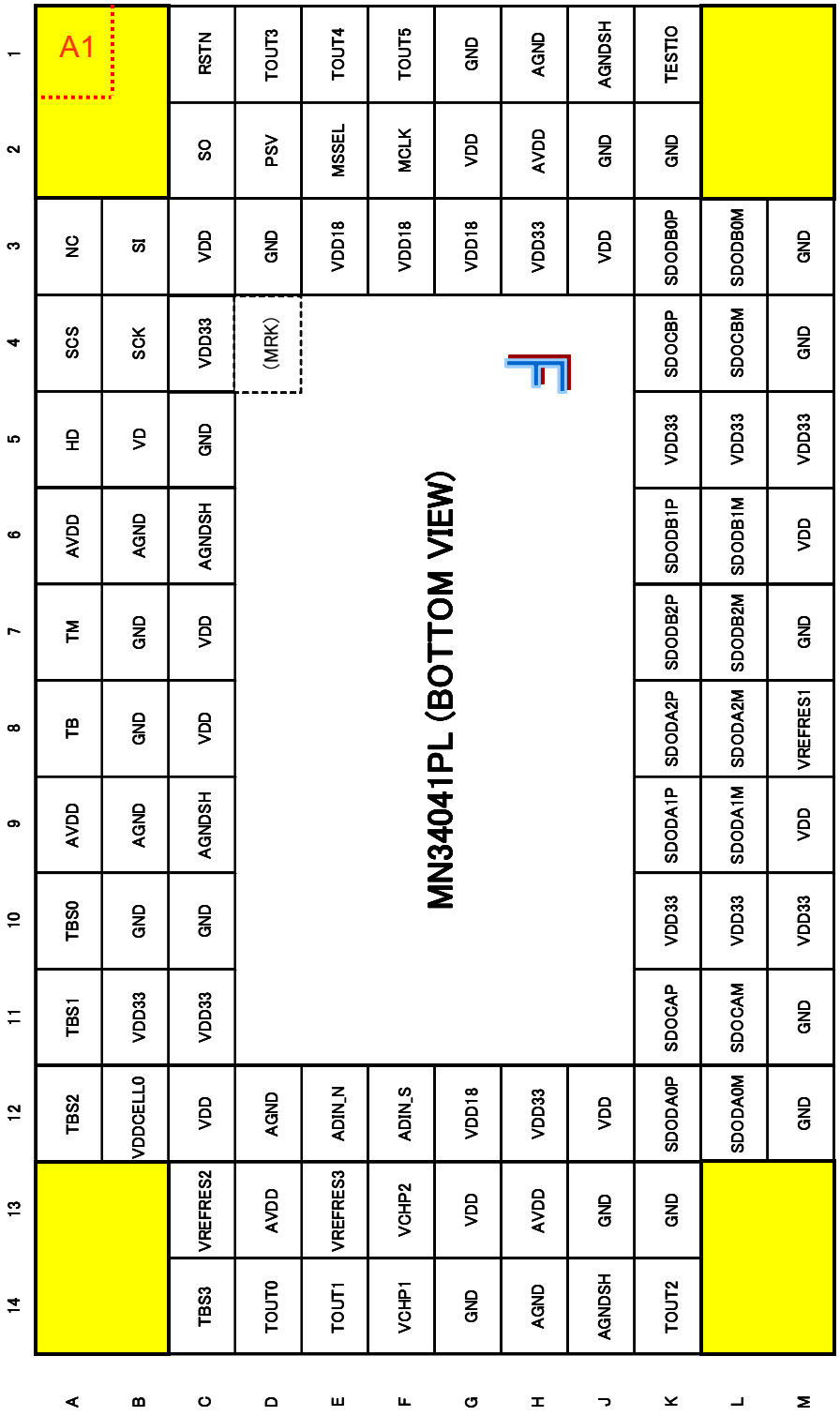


Figure 1.1.4 Pin Connection (BOTTOM VIEW)

Do not connect to the unused pin "NC". Make it OPEN electrically.

D4 (MRK) is a recognition mark of package and it is not a pin.

Pin specifications, process and functions list

Specifications and functions of pins showed in Figure 1.1.4 are the following.

Explanation of symbols: I: INPUT, O: OUT, P: POWER, G: GND

Table 1.1.2 List of Pin Specifications, Process and Functions

Pin No.	Pin name	I/O	Process	Functions
A3	NC	-	OPEN	None(Not connected to device)
A4	SCS	I	Input chip select signal（Low : Select）	Serial chip select
A5	HD	I/O	Sensor master : OPEN Sensor slave : Horizontal synchronous signal input	Horizontal synchronous signal input
A6	AVDD	P	Connect analog 3.3V power supply	Analog 3.3V power supply
A7	TM	I	Connect DGND	Test
A8	TB	O	OPEN	Test
A9	AVDD	P	Connect analog 3.3V power supply	Analog 3.3V power supply
A10	TBS0	O	OPEN	Test
A11	TBS1	O	OPEN	Test
A12	TBS2	O	OPEN	Test
B3	SI	I	Input serial data	Serial data input
B4	SCK	I	Input serial clock	Serial clock input
B5	VD	I/O	Sensor master : OPEN Sensor slave : Vertical synchronous signal input	Vertical synchronous signal
B6	AGND	G	Connect AGND	AGND
B7	GND	G	Connect DGND	DGND
B8	GND	G	Connect DGND	DGND
B9	AGND	G	Connect AGND	AGND
B10	GND	G	Connect DGND	DGND
B11	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply
B12	VDDCELL0	I/O	OPEN	Test
C1	RSTN	I	Input reset signal (Low: Reset)	Reset signal
C2	SO	I/O	Connect 10kΩ between DGND	Serial signal output(Not guaranteed) Register read : output, Others:Hi-z
C3	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
C4	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply
C5	GND	G	Connect DGND	DGND
C6	AGNDSH	G	Connect AGND	AGND
C7	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
C8	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
C9	AGNDSH	G	Connect AGND	AGND
C10	GND	G	Connect DGND	DGND
C11	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply
C12	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
C13	VREFRES2	I	Connect 12kΩ between AGND *1	Reference resistance for internal circuit
C14	TBS3	O	OPEN	Test

Pin No.	Pin name	I/O	Process	Functions
D1	TOUT3	O	OPEN	Test
D2	PSV	I	Input power save signal (Low:Power save)	Power save signal
D3	GND	G	Connect DGND	DGND
D4	(MRK)	-	OPEN(This is not a pin)	Package recognition mark
D12	AGND	G	Connect AGND	AGND
D13	AVDD	P	Connect analog 3.3V power supply	Analog 3.3V power supply
D14	TOUT0	O	OPEN	Test
E1	TOUT4	O	OPEN	Test
E2	MSSEL	I	Sensor mode (High:Slave, Low:Master)	Sensor mode select signal
E3	VDD18	P	Connect 1.8V power supply	Digital 1.8V power supply
E12	ADIN_N	O	OPEN	Test
E13	VREFRES3	I	Connect 12kΩ between AGND *1	Reference resistance for internal circuit
E14	TOUT1	O	OPEN	Test
F1	TOUT5	O	OPEN	Test
F2	MCLK	I	Input master clock	Master clock input
F3	VDD18	P	Connect 1.8V power supply	Digital 1.8V power supply
F12	ADIN_S	O	OPEN	Test
F13	VCHP2	P	Connect 2.2μF bypath capacitance	Down converter (Voltage is generated internally)
F14	VCHP1	P	Connect 2.2μF bypath capacitance	Power supply for pixel (Voltage is generated internally)
G1	GND	G	Connect DGND	DGND
G2	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
G3	VDD18	P	Connect 1.8V power supply	Digital 1.8V power supply
G12	VDD18	P	Connect 1.8V power supply	Digital 1.8V power supply
G13	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
G14	GND	G	Connect DGND	DGND
H1	AGND	G	Connect AGND	AGND
H2	AVDD	P	Connect analog 3.3V power supply	Analog 3.3V power supply
H3	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply
H12	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply
H13	AVDD	P	Connect analog 3.3V power supply	Analog 3.3V power supply
H14	AGND	G	Connect AGND	AGND
J1	AGNDSH	G	Connect AGND	AGND
J2	GND	G	Connect DGND	DGND
J3	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
J12	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
J13	GND	G	Connect DGND	DGND
J14	AGNDSH	G	Connect AGND	AGND

Pin No.	Pin name	I/O	Process	Functions
K1	TESTIO	I/O	OPEN	Test
K2	GND	G	Connect DGND	DGND
K3	SDODB0P	O	Connect latter device	LVDS output(ch2 port0 data+)
K4	SDOCBP	O	Connect latter device	LVDS output(ch2 clock data+)
K5	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
K6	SDODB1P	O	Connect latter device	LVDS output(ch2 port1 data+)
K7	SDODB2P	O	OPEN	LVDS output(ch2 port2 data+)
K8	SDODA2P	O	OPEN	LVDS output(ch1 port2 data+)
K9	SDODA1P	O	Connect latter device	LVDS output(ch1 port1 data+)
K10	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
K11	SDOCAP	O	Connect latter device	LVDS output(ch1 clock data+)
K12	SDODA0P	O	Connect latter device	LVDS output(ch1 port0 data+)
K13	GND	G	Connect DGND	DGND
K14	TOUT2	O	OPEN	Test
L3	SDODB0M	O	Connect latter device	LVDS output(ch2 port0 data-)
L4	SDOCBM	O	Connect latter device	LVDS output(ch2 clock data-)
L5	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
L6	SDODB1M	O	Connect latter device	LVDS output(ch2 port1 data-)
L7	SDODB2M	O	OPEN	LVDS output(ch2 port2 data-)
L8	SDODA2M	O	OPEN	LVDS output(ch1 port2 data-)
L9	SDODA1M	O	Connect latter device	LVDS output(ch1 port1 data-)
L10	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
L11	SDOCAM	O	Connect latter device	LVDS output(ch1 clock data-)
L12	SDODA0M	O	Connect latter device	LVDS output(ch1 port0 data-)
M3	GND	G	Connect DGND	DGND
M4	GND	G	Connect DGND	DGND
M5	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
M6	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
M7	GND	G	Connect DGND	DGND
M8	VREFRES1	I	Connect 12kΩ between DGND *1	Reference resistance for internal circuit
M9	VDD	P	Connect 1.2V power supply	Digital core 1.2V power supply
M10	VDD33	P	Connect digital 3.3V power supply	Digital 3.3V power supply (LVDS)
M11	GND	G	Connect DGND	DGND
M12	GND	G	Connect DGND	DGND

∗1) Connect resistive element (12 kΩ ± 0.5 %) between VREFRES 1, 2, 3 pin and GND shown as Figure 1.2.1.

■ Absolute Maximum Ratings and Operating Voltage Condition

Table 1.1.3 Values for Absolute Maximum Ratings and Operating Voltage Condition

Name	Unit	Absolute Maximum Ratings		Operating Voltage Condition			Remarks
		Lower limit	Upper limit	Minimum	Standard	Maximum	
AVDD	V	- 0.3	4.5	3.15	3.3	3.45	-
VDD33	V	- 0.3	4.5	3.15	3.3	3.45	-
VDD18	V	- 0.3	2.5	1.62	1.8	1.98	-
VDD	V	- 0.3	1.6	1.08	1.2	1.32	-
VCHP1	V	-	-	-	-	-	Voltage is internally generated.
VCHP2	V	-	-	-	-	-	Voltage is internally generated.
AGND GND	V	GND		-	0	-	-

・The absolute maximum ratings are the limit values applied to the chip, which do not lead to damage.
They shall not guarantee proper operation.

・Connect bypath ceramic capacitance (0.1μF) between all of power supply pins and GND nearby these pins. Connect also bypath ceramic capacitance (2.2μF or more) together.

■ Drive current

Table 1.1.4 Power supply current

Item	Unit	Lower limit	Standard	Upper limit	Remarks
AVDD current	mA	-	64	87	VDD33 = AVDD = 3.3V、 VDD18 = 1.8V、VDD=1.2V、 Full scan, 60fps, 25℃, Column amplifier gain = Standard, Analog gain = 0dB, Digital gain = 0dB, MCLK=27MHz, Saturating illuminance, Measured by tester of Panasonic
VDD33 current	mA	-	20	22	
VDD18 current	mA	-	0.1	1	
VDD current	mA	-	143	153	

■ Temperature Conditions

Table 1.1.5 Temperature Conditions

Item	Unit	Lower limit	Standard	Upper limit	Remarks
Operating temperature	℃	-10	25	75	(＊1)
Performance assurance temperature	℃	0	25	60	(＊2)
Storage temperature	℃	-30	25	85	(＊3)

＊1 Operating temperature and storage temperature are defined by the temperature around the sensor. Operating temperature shall not guarantee the characteristics.

＊2 Performance assurance temperature is defined by the temperature of wafer. Characteristics are measured in 60℃ (Wafer inspection), standard (Room temperature), 25℃ (Final inspection). Other temperatures are assured as design guarantee.

＊3 Storage temperature is defined by the temperature of around the sensor.

1.2 Operation

1. 2. 1 List of Drive Mode

■ Drive Mode

Table 1.2.1 Drive Mode (General)

Mode	Output				Frame rate (fps)	Number of active pixels		Frame format		
	MCLK	Data rate(MHz)	LVDS format	Number of ADC output bit		H pix	V line	H clock	V line	HCYCLE (MCLK)
Full scan	27	162	12bit 2ch 2port	12	60p	1944	1092	2400	1125	400
	37.125	148.5	12bit 2ch 2port	12	60p	1944	1092	2200	1125	550

※ LVDS output data rate 486Mbps (MCLK:27MHz), 445.5Mbps (MCLK:37.125MHz)

※ HCYCLE in frame format shows the number of clock in pixel rate.

1. 2. 2 Reference Circuit

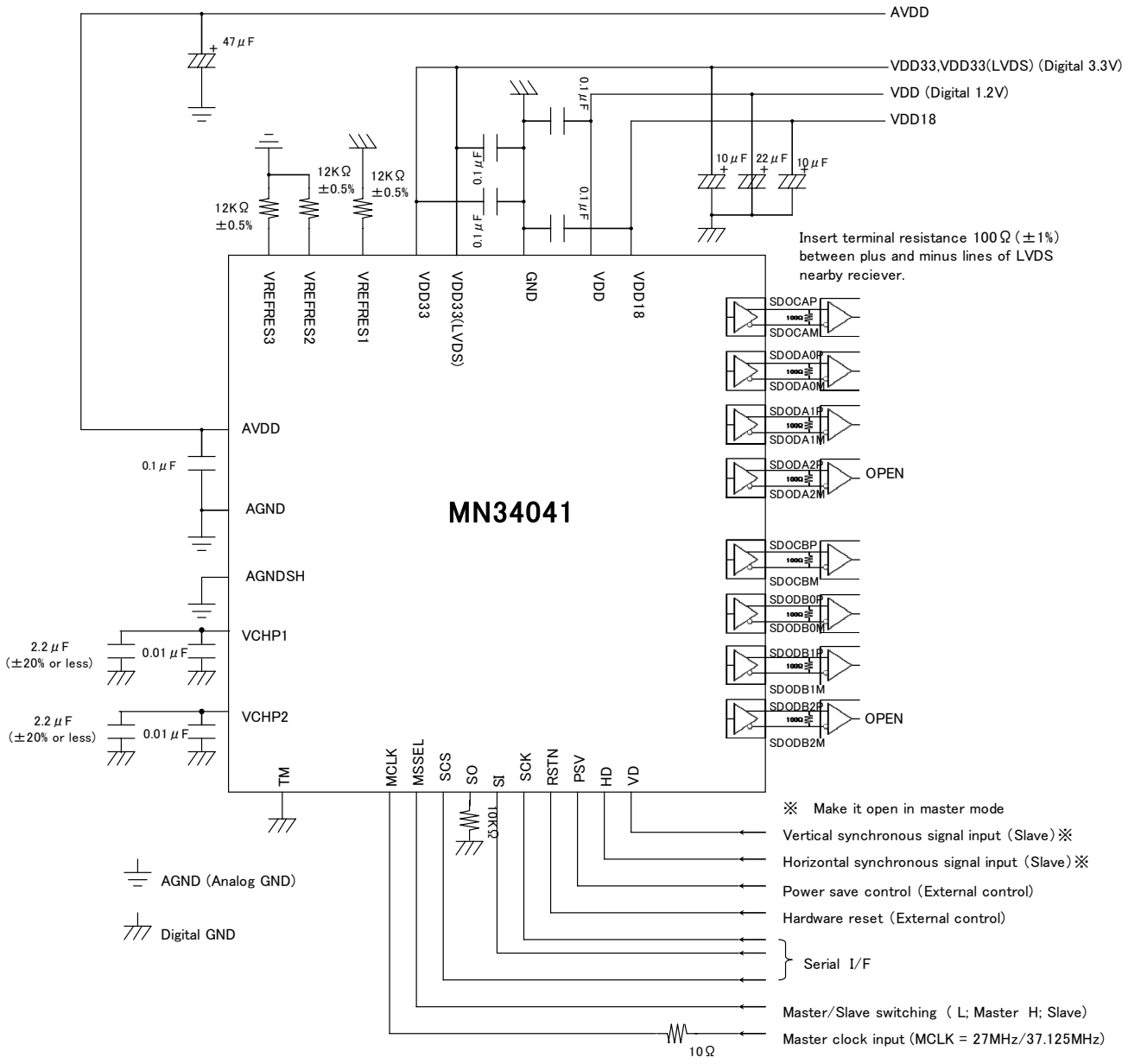


Figure 1.2.1 Reference circuit

■ Recommended Coupling Parts for Each Power Supply Pin (decoupling capacitor)

Apply decoupling capacitance (about 0.1μF) with small parasitic series inductance to a pair of power supply and GND near the pin as possible to cut high-frequency noise.

For example, decoupling capacitances in four corners of the chip in each four pairs of AVDD and AGND are recommended.

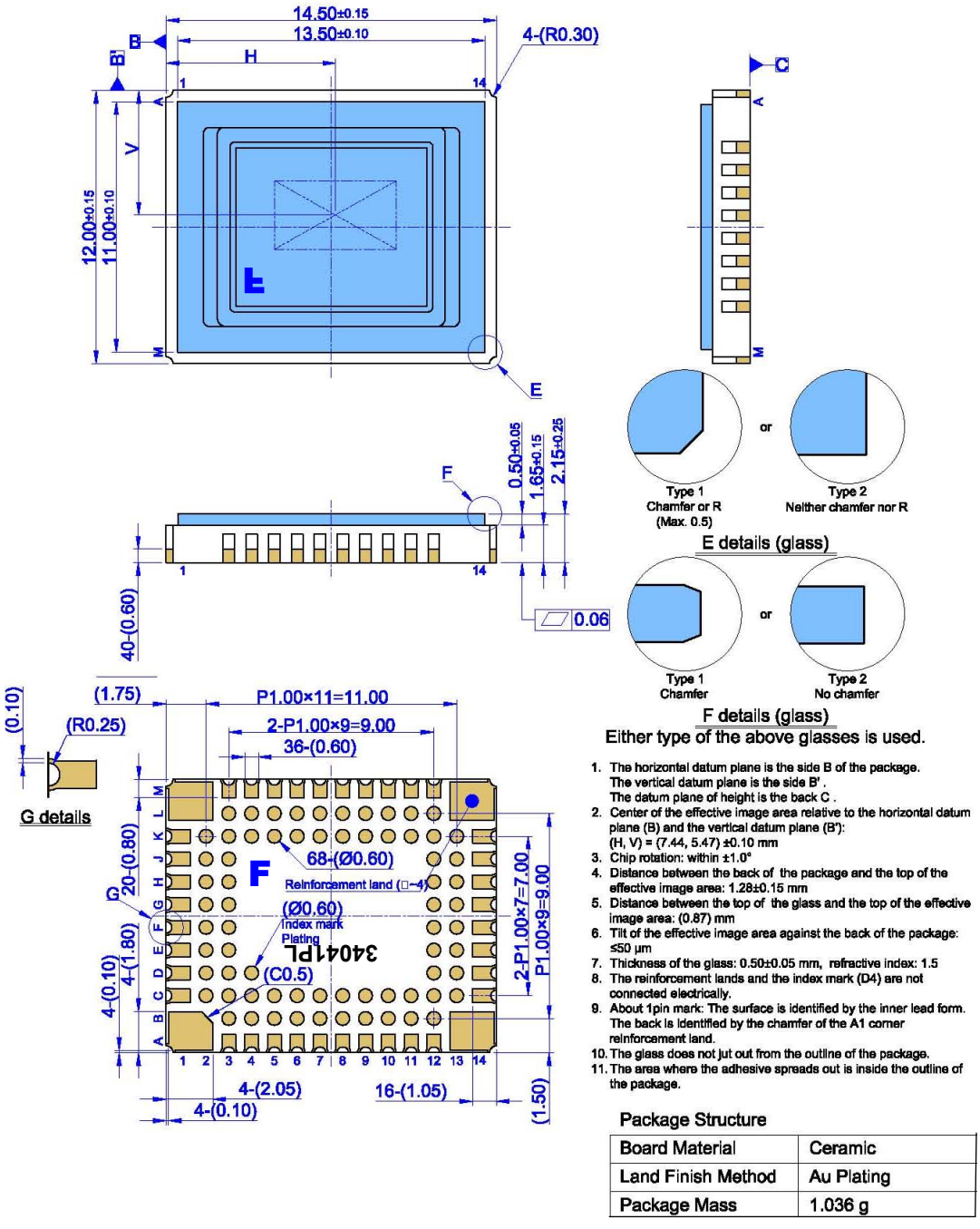
■Connect SO pin if need to read registers though it is not guaranteed.

1. 3 Package

1. 3. 1 Dimensions

【External view of package】
External dimensional drawing
LGA104-C-120145-IA01

UNIT : mm
Tolerance without directions : ±0.20



Either type of the above glasses is used.

1. The horizontal datum plane is the side B of the package. The vertical datum plane is the side B'. The datum plane of height is the back C.
2. Center of the effective image area relative to the horizontal datum plane (B) and the vertical datum plane (B'): (H, V) = (7.44, 5.47) ±0.10 mm
3. Chip rotation: within ±1.0°
4. Distance between the back of the package and the top of the effective image area: 1.28±0.15 mm
5. Distance between the top of the glass and the top of the effective image area: (0.87) mm
6. Tilt of the effective image area against the back of the package: ≤50 µm
7. Thickness of the glass: 0.50±0.05 mm, refractive index: 1.5
8. The reinforcement lands and the index mark (D4) are not connected electrically.
9. About 1pin mark: The surface is identified by the inner lead form. The back is identified by the chamfer of the A1 corner reinforcement land.
10. The glass does not jut out from the outline of the package.
11. The area where the adhesive spreads out is inside the outline of the package.

Package Structure

Board Material	Ceramic
Land Finish Method	Au Plating
Package Mass	1.036 g

Figure 1.3.1 Package Dimensions (LGA104-C-120145-IA01)

Documents

This product has documents of data sheet, product detail specifications, specification of registers, and application notes necessary to set design.

If you need more information, please download documents from the web page or request it from semiconductor support system.

Title	Explanation	MN34041
Datasheet	Product overview, application circuit, package outline, etc.	Download
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Register specifications	Detailed specifications of registers	Contact Us (For Registered Users)
Application note	Notes on the design for applications, etc.	Contact Us (For Registered Users)

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