MN3671RE

Color CCD Linear Image Sensor with 1024 Pixels for R and B Colors/2048 Pixels for G Color

■Overview

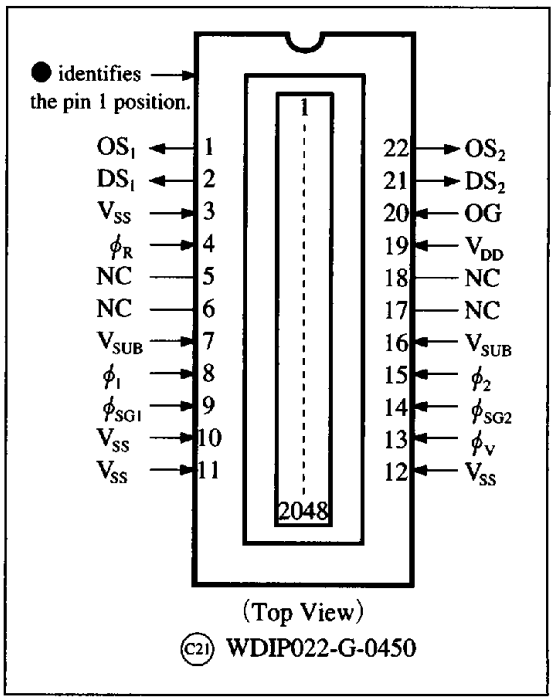
The MN3671RE is a high responsivity CCD color linear image sensor with 1024 pixels each for R and B and 2048 G pixels, and having low dark output floating photodiodes in the photodetector region and CCD analog shift registers for read out.

It can read a B4 size color document with a high quality and a maximum pseudo resolution of 200dpi. In addition to being used as a color sensor, this device can also be used as a black and white sensor if only the G row is used, and in this case, it is possible to read a B4 size document with a full resolution of 200dpi. Since a one line delay analog memory is built in so as to compensate for the difference in the positions of reading out between the R, B rows and the G row, the configuration of the signal processing circuit becomes simpler.

■Features

- 4096 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- It is possible to read a B4 size color document with a high pseudo resolution of 200dpi.
- RGB primary colors type on chip color filters are used for color separation.
- In order to compensate for the distance between the photodiode rows for the R, B colors and the G color, the device has a built-in analog memory that can store the signals of one line of the R-B colors row.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- Large signal output of typically 1.2V at saturation can be obtained.

■Pin Assignments



(Top View)

C21 WDIP022-G-0450

■Application

- Graphic and character read out in fax machines, image scanners, etc.

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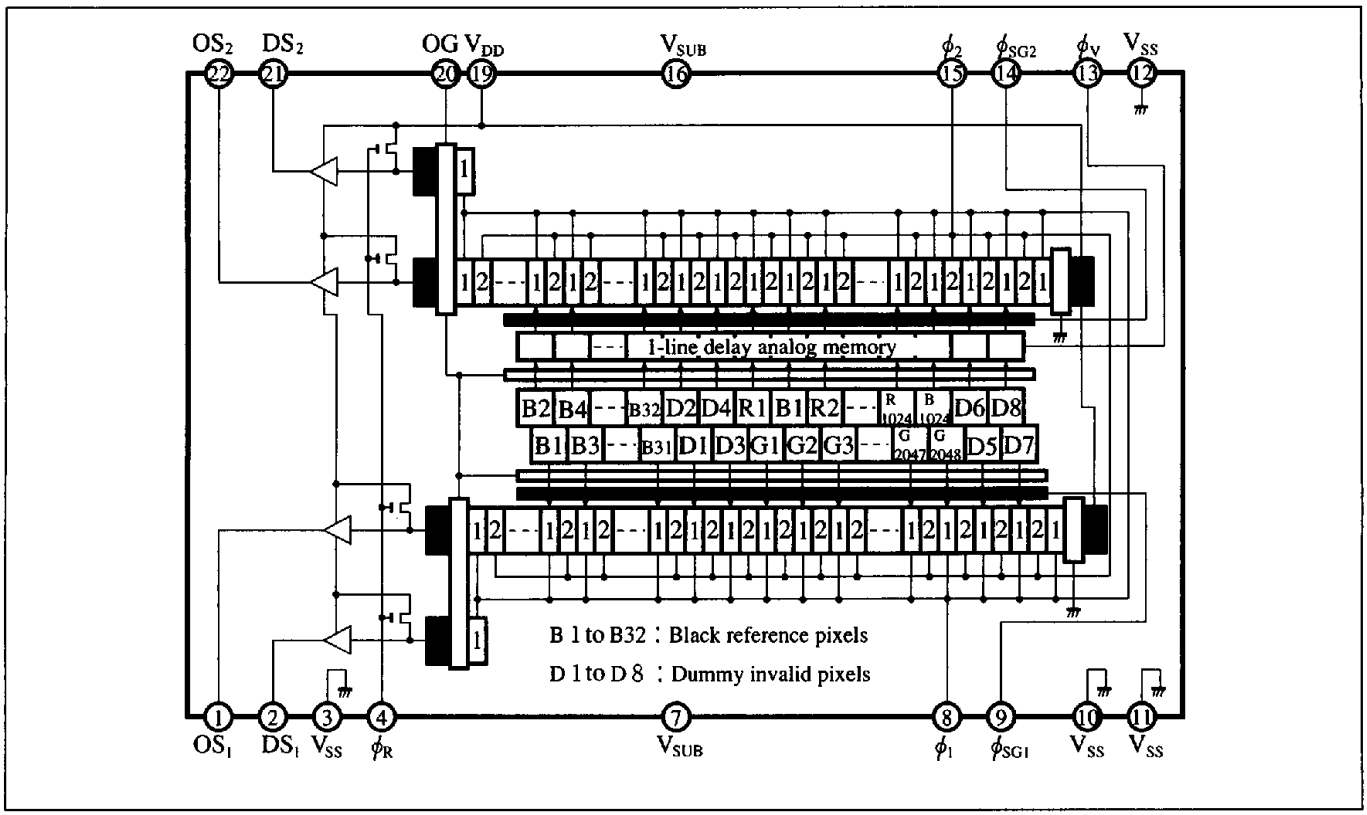
■Block Diagram



■Absolute Maximum Ratings (Ta=25℃, VSS=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to +17	V
	V_{OG}	−0.3 to +17	V
Input voltage	V_I	−0.3 to +17	V
Output voltage	V_O	−0.3 to +17	V
Operating temperature range	T_{opr}	0 to +60	℃
Storage temperature range	T_{stg}	−25 to +85	℃

■Operating Conditions

●Voltage conditions (Ta=0 to +60℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.5	12.0	13.0	V
Substrate voltage	V_{sub}	$V_{sub}=V_{DD}$	11.5	12.0	13.0	V
Output gate voltage	V_{OG}	$V_{DD}=12.0V$	4.2	4.5	4.8	V
Vertical transfer clock High level	V_{VH}	ϕ_V	$V_{DD}-1$	V_{DD}	V_{DD}	V
Vertical transfer clock Low level	V_{VL}	ϕ_V	0	0.5	0.8	V
CCD shift register clock High level	$V_{\phi H}$	ϕ_1, ϕ_2	$V_{DD}-1$	V_{DD}	V_{DD}	V
CCD shift register clock Low level	$V_{\phi L}$	ϕ_1, ϕ_2	0	0.5	0.8	V
Shift gate clock High level	V_{SH}	ϕ_{SG1}, ϕ_{SG2}	$V_{DD}-1$	V_{DD}	V_{DD}	V
Shift gate clock Low level	V_{SL}	ϕ_{SG1}, ϕ_{SG2}	0	0.5	0.8	V
Reset gate clock High level	V_{RH}	ϕ_R	$V_{DD}-1$	V_{DD}	V_{DD}	V
Reset gate clock Low level	V_{RL}	ϕ_R	0	0.5	0.8	V

■Operating Conditions (continued)

●Timing conditions (Ta=0 to +60℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C=1/2T	0.1	1.0	3.0	MHz
Reset clock frequency	f_R	f_R=1/2T	0.1	1.0	3.0	MHz
Shift register clock rise time	t_{Cr}		0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Shift clock 1 rise time	t_{SG1r}		0	15	50	ns
Shift clock 1 fall time	t_{SG1f}		0	15	50	ns
Shift clock 1 pulse width	t_{SG1w}		5	10	50	μs
Vertical transfer clock rise time	t_{Vr}		0	15	50	ns
Vertical transfer clock fall time	t_{Vf}		0	15	50	ns
Vertical transfer clock set up time	t_{Vs}	ϕ_{SG1} and ϕ_V should be the same timing.	0.5	1.0	2.0	μs
Vertical transfer clock pulse width	t_{Vw}		5	10	50	μs
Vertical transfer clock hold time	t_{Vh}		0	1.0	2.0	μs
Shift clock 2 rise time	t_{SG2r}		0	15	50	ns
Shift clock 2 fall time	t_{SG2f}		0	15	50	ns
Shift clock 2 set up time	t_{SG2s}		0.5	1.0	2.0	μs
Shift clock 2 pulse width	t_{SG2w}		5	10	50	μs
Reset clock rise time	t_{Rr}		0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock pulse width	t_{Rw}		50	100	—	ns
Reset clock hold time	t_{Rh}		10	20	—	ns

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■Electrical Characteristics

●Clock input capacitance (Ta=0 to +60℃)

Parameter	Symbol	Condition	min	typ	max	Unit
CCD Shift register clock input capacitance	C_1, C_2	V_{IN}=12V f=1MHz	—	400	—	pF
Vertical transfer clock input capacitance	C_V		—	100	—	pF
Reset clock input capacitance	C_{RS}		—	20	—	pF
Shift clock input capacitance	C_{SG1}, C_{SG2}		—	150	—	pF

●DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}=+12V	—	20	50	mA

●AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t_{OS}		—	50	—	ns

■Optical Characteristics

<Inspection conditions>

- Ta=25℃, V_{DD}=12V, $V_{\phi H}$=V_{VH}=V_{SH}=V_{RH}=12V (pulse), f_C=f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp with IR/UV cutting filter
- Optical system: A slit with an aperture dimensions of 20mm×20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 1024 valid R and B pixels and the 2048 valid G pixels excluding the dummy pixels D1 to D8.

■Optical Characteristics (continued)

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R_R	Note 1	0.5	0.7	0.9	V/lx·s
	R_G	Note 1	0.9	1.2	1.5	
	R_B	Note 1	0.5	0.8	1.1	
Photo response non-uniformity	PRNU	Note 2	—	5	15	%
Saturation output voltage	V_{SAT}	Note 3	0.8	1.2	—	V
Saturation exposure	SE_R	Note 4	0.89	1.71	—	lx·s
	SE_G	Note 4	0.53	1.00	—	
	SE_B	Note 4	0.73	1.50	—	
Dark signal output voltage	V_{DRK1}	OS_1, Dark condition, see Note 5	—	0.5	1.0	mV
	V_{DRK2}	OS_2, Dark condition, see Note 5	—	1.0	2.0	
Dark signal output non-uniformity	DSNU1	OS_1, Dark condition, see Note 6	—	0.1	2.0	mV
	DSNU2	OS_2, Dark condition, see Note 6	—	0.2	4.0	
Shift register total transfer efficiency	STTE		92	—	—	%
Dynamic range	DR	Note 7	—	1200	—	

Note 1) Responsivity (R)

This is the value obtained by dividing the average output voltage (V) of the all pixels by the exposure (lx·s).
The exposure (lx·s) is the product of the illumination intensity (lx) and the accumulation time (s).
Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

Note 2) Photo response non-uniformity (PRNU)

This is defined by the following equation where X_{ave} is the average output voltage of the valid pixels of each of the colors R, G, and B, and Δx is the difference between the output voltage of the maximum (or minimum) output pixel and X_{ave}, when the photodetector region is illuminated with light of a uniform illumination intensity distribution.

$$PRNU = \frac{\Delta x}{X_{ave}} \times 100 \ (\%)$$

The incident light intensity shall be 50% of the standard saturation llight intensity.

Note 3) Saturation output voltage (V_{SAT})

This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 4) Saturation Exposure (SE)

This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

Note 5) Dark signal output voltage (V_{DRK})

This is defined as the average of the output from all the valid pixels in the dark condition at Ta=25℃, T_{int}=10ms. Normally, the dark signal output voltage gets doubled for every 8 to 10℃ increase in Ta and is proportional to T_{int}. The dark signal output voltage (V_{DRK2}) on the OS_2 side will be larger than the dark signal output voltage (V_{DRK1}) on the OS_1 side because there is a delay memory on the OS_2 side.

Note 6) Dark signal non-uniformity (DSNU)

This is defined as the difference between the maximum value among the output voltages from the all active pixels at Ta=25℃ and T_{int}=10ms and V_{DRK}.

Note 7) Dynamic range (DR)

This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

■Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS_1	Signal output 1 (for G)	
2	DS_1	Compensation output 1 (for G)	
3	V_{SS}	Ground	
4	ϕ_R	Reset clock	
5	NC	Non connection	Connect externally to V_{SS}.
6	NC	Non connection	Connect externally to V_{SS}.
7	V_{SUB}	Substrate	Should be left open or connected to V_{DD} voltage.
8	ϕ_1	CCD shift register clock	
9	ϕ_{SG1}	Shift clock gate 1	
10	V_{SS}	Ground	
11	V_{SS}	Ground	
12	V_{SS}	Ground	
13	ϕ_V	Vertical transfer clock	
14	ϕ_{SG2}	Shift clock gate 2	
15	ϕ_2	CCD shift register clock	
16	V_{SUB}	Subustrate	Should be left open or connected to V_{DD} voltage.
17	NC	Non connection	Connect externally to V_{SS}.
18	NC	Non connection	Connect externally to V_{SS}.
19	V_{DD}	Power supply	
20	OG	Output gate	
21	DS_2	Compensation output 2 (for R and B)	
22	OS_2	Signal output 2 (for R and B)	

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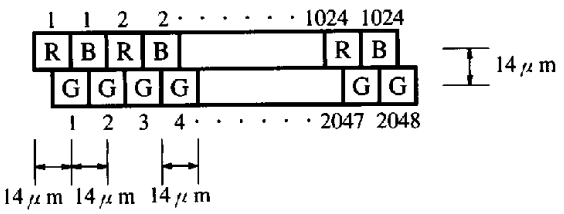
■Construction of the Image Sensor

The MN3671RE can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11 μm floating photodiode and a 3 μm channel stopper (isolation region) per pixel, and such pixels are arranged in a linear row with a pitch of 14 μm along the main scanning direction.
- The R-B row has 1024 pixels each of the red and blue colors arranged alternatingly, and the G row has 2048 pixels. The R-B row and G row are placed with a spacing of one line (14 μm) along the sideways scanning direction. The pixels of the G row are displaced by half the pixel pitch (7 μm) relative to the pixels of the R-B row in the main scanning direction.



- A one line analog delay memory is built in the chip in order to compensate for the difference in the positions of the R-B and G rows in the sideways scanning direction.
- The photodetector window is a rectangle of dimensions 8 μm (Horizontal) × 11 μm (Vertical), and the areas other than the photodetector window are optically shielded.
- The photodetector region has a total of 32 optically shielded (black reference) pixels that can be used as the black level reference, with 16 pixels each for the R-B row and the G row.

b) CCD Transfer region (shift register)

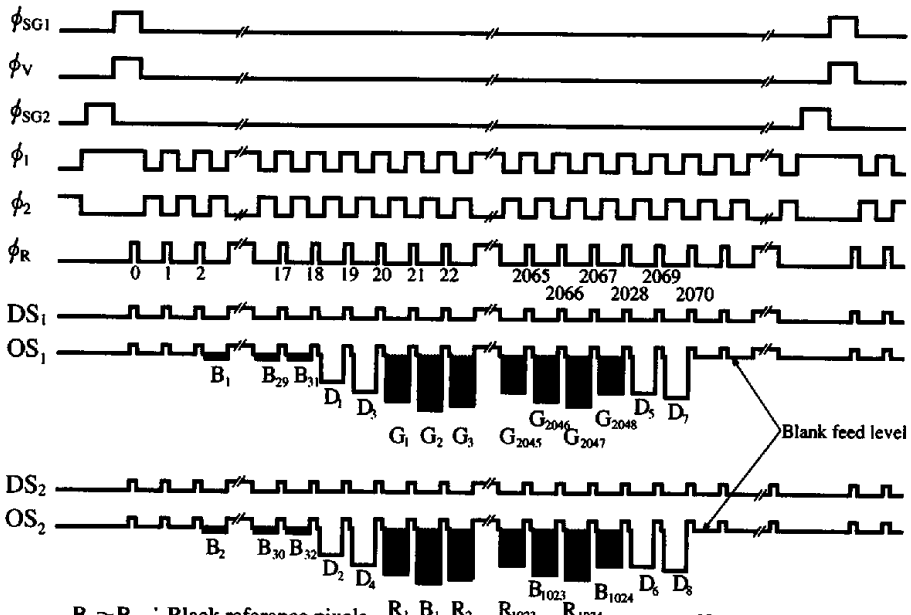
- The signal charges obtained by photoelectric conversion are transferred to the CCD transfer regions of the respective colors during the period when the shift gate (ϕ_{SG}) is at the High level. The signal charges transferred to this analog shift register are successively transferred to the output region.
- A buried type CCD that can be driven by a two phase clock (ϕ_1, ϕ_2) is used for the analog shift register.

c) Output region

- The signal charge transferred to the output region is first sent to the charge to voltage conversion region where it is converted into a voltage level corresponding to the amount of the signal charge, and then output after impedance conversion in a two stage source follower amplifier.
- The DC level component not containing the optical signal and the clock noise component are output at the DS pin.
- It is possible to obtain a signal with a high S/N ratio with reduced clock noise, etc., by carrying out differential amplification of the OS and DS outputs externally.

■Timing Diagram

(1) I/O timing



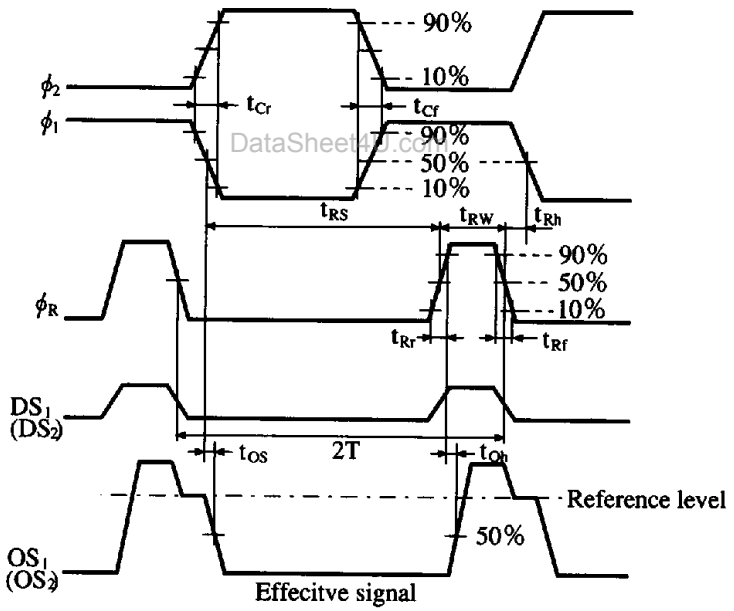
$B_1 \sim B_{32}$: Black reference pixels

$D_1 \sim D_8$: Dummy invalid pixels

* OS_2 outputs the previous line signal.

Note) Repeat the transfer pulses (ϕ_1, ϕ_2) for more than 2070 periods.

(2) Drive timing



■Graphs and Characteristics