MICRO NETWORKS

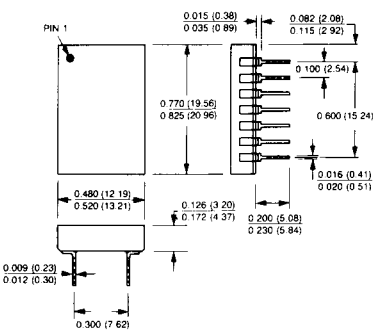
MN374

HIGH-SPEED
HIGH-RESOLUTION
TRACK-HOLD AMPLIFIER

FEATURES

- 4μsec Max Acquisition Time (20V Step to ±0.003%)
- Compatible with All DIP Packaged 14-16 Bit A/D's
- 400psec Aperture Jitter
- ±1μV/μsec Max Droop Rate
- 90dB Min Feedthrough Attenuation
- Small 14-Pin DIP
- Pin and Function Compatible with SHC76
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN374 is a high-speed (4μsec max acquisition time for a 20V step acquired to ±0.003%), high-resolution (±0.003%FSR max linearity error), unity-gain, inverting track-hold (T/H) amplifier designed to be compatible with virtually all DIP-packaged, 14-16 bit A/D converters available today. In particular, MN374 mates well with Micro Networks MN5290/5291 (40μsec, 16-bit A/D's) and MN5295/5296 (17μsec, 16-bit A/D's) as well as with other industry-standard 16-bit A/D's (ADC71/72, ADC76, AD376, etc.).

The TTL-compatible MN374 makes the speed/precision trade-off very well. Its impressive d.c. specifications include a maximum ±0.02% gain error, a maximum ±3mV offset error and a maximum ±4mV pedestal. Dynamic specifications include 4μsec max acquisition time (20V step acquired to ±0.003%); 3μsec max track-to-hold transient settling time (to ±0.003%FSR); 400psec aperture jitter; and ±30V/μsec slew rate. MN374's outstanding ±1μV/μsec maximum output droop rate enables the device to hold signals to the 14-bit level for up to 600μsec and to the 16-bit level for up to 150μsec. These performance levels make MN374 ideal for high-resolution data acquisition in either single-channel, multichannel sequenced, or multichannel simultaneous-sampling applications.

An application note in this data sheet describes how to mate MN374 with MN5295 (16-bit, 17μsec A/D) to create a 40kHz sampling A/D that guarantees 14-bit "no missing codes" over its full temperature range.

MN374 is packaged in a small, 14-pin, single-wide, ceramic DIP, and it carries the pinout that has become the de facto standard for high-resolution T/H's. MN374 is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN374H/B CH is fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

Contact factory for availability of CH devices.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN374 HIGH-SPEED HIGH-RESOLUTION T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN374	0°C to +70°C
MN374H, MN374H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 11)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Analog Input (Pin 13)	± 15 Volts
Digital Input (Pin 1)	−0.5 to +7 Volts
Output Current (Note 1)	± 20 mA

ORDERING INFORMATION

PART NUMBER ——— 374H/B CH

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" devices.

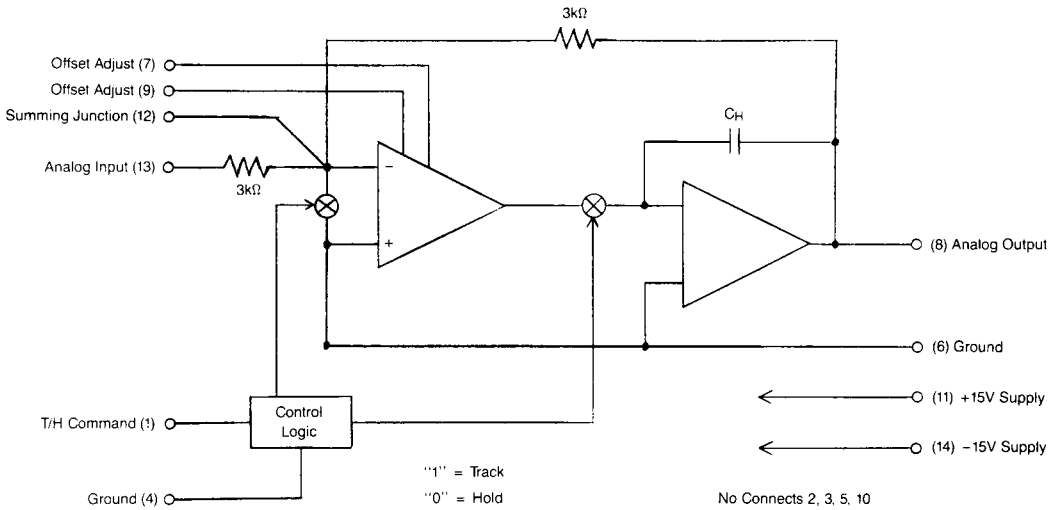
SPECIFICATIONS (T_A = +25°C, ± Vcc = ± 15V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	± 10	± 11		Volts
Input Impedance (Note 2)		3		kΩ
Output Current (Note 1)	± 5			mA
Output Impedance (Note 2)		1		Ω
Maximum Capacitive Load (Note 2)		250		pF
DIGITAL INPUT				
Logic Levels: Logic "1" (Track Mode)	+2.0			Volts
Logic "0" (Hold Mode)			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
TRANSFER CHARACTERISTICS (Note 3)				
Gain		−1		V/V
Gain Linearity Error		± 0.001	± 0.003	%FSR
Gain Accuracy: Initial (+25°C)		± 0.01	± 0.02	%
Drift (Note 6)		± 1	± 5	ppm/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 0.02	± 0.07	%
Offset Voltage (Track Mode, Note 4): Initial (+25°C)		± 0.5	± 3	mV
Drift (Note 6)		± 5	± 20	μV/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 1	± 5	mV
Pedestal (Note 5): Initial (+25°C)		± 2	± 4	mV
Drift (Note 6)		± 10	± 40	μV/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 3	± 8	mV
DYNAMIC CHARACTERISTICS				
Acquisition Time:				
20V Step to ± 0.003% (± 0.6mV)		2.5	4	μsec
20V Step to ± 0.01% (± 2mV, Note 2)		1.5	3	μsec
10V Step to ± 0.003% (± 0.3mV, Note 2)		3		μsec
10V Step to ± 0.01% (± 1mV, Note 2)		1.2		μsec
Track-to-Hold Transient (Note 2):				
Amplitude		200		mV
Settling Time to ± 0.003% FSR (± 0.6mV)		0.5	3	μsec
Settling Time to ± 0.01% FSR (± 2mV)		0.3	2	μsec
Aperture Delay Time (Note 2)		30		nsec
Aperture Jitter (Note 2)		400		psec
Output Slew Rate (Note 2)		± 30		V/μsec
Small Signal Bandwidth (−3dB, Note 2)		1.5		MHz
Full Power Bandwidth (Note 2)		500		kHz
Output Droop Rate: +25°C		± 0.1	± 1	μV/μsec
0°C to +70°C		± 10	± 100	μV/μsec
−55°C to +125°C ("H" Models)		± 50	± 500	μV/μsec
Feedthrough Attenuation (20kHz, 20Vp-p input)	90	100		dB
Output Noise (d.c. to 1MHz, Note 2) Track Mode		200		μV(rms)
Hold Mode		200		μV(rms)
POWER SUPPLIES				
Voltage Range (Note 7)	± 14.5	± 15	± 15.5	Volts
Power Supply Rejection: +15V Supply		± 75		μV/V
−15V Supply		± 75		μV/V
Quiescent Current Drain: +15V Supply		+15	+24	mA
−15V Supply		−11	−13	mA
Power Consumption		390	495	mW

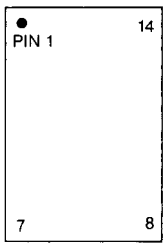
SPECIFICATION NOTES:

1. MN374's output is not short-circuit protected. Continuous shorts to ground or instantaneous shorts to either supply will result in destruction. In normal operation, continuous output current should not exceed ± 10mA.
2. These parameters are listed for reference only and are not tested.
3. FSR stands for full scale range and is equal to 20 Volts for the MN374. ± 0.003%FSR is equivalent to ± ½LSB for a 14-bit system.
4. Initial track-mode offset error is adjustable to zero with a user-optional external potentiometer. The offset adjust may also be used to compensate for pedestal. See Offset Adjustment.
5. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN374, pedestal is constant regardless of input/output level.
6. MN374 is fully specified for 0°C to +70°C operation. MN374H and MN374H/B are fully specified for −55°C to +125°C operation.
7. MN374 will operate with ± Vcc supplies down to ± 11.4 Volts if input/output voltage is kept below ± 7.5V.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 T/H Command	14 −15V Supply (−Vcc)
2 No Connect	13 Analog Input
3 No Connect	12 Summing Junction
4 Ground	11 +15V Supply (+Vcc)
5 No Connect	10 No Connect
6 Ground	9 Offset Adjust
7 Offset Adjust	8 Analog Output

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from the MN374. The unit's two Ground pins (pins 4 and 6) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible. If your system distinguishes between analog and digital ground, pin 6 may be connected to system analog ground and pin 4 to system digital ground.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines. Input and output signal lines should be kept as short as possible, and if external offset adjustment is used, the potentiometer should be located as close to the unit as possible. If offset adjust is not used, pins 7 and 9 should be left open.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

OFFSET ADJUSTMENT—MN374's track-mode offset error can be reduced to zero using a 10kΩ to 20kΩ potentiometer connected between pins 7 and 9 with its wiper connected to −15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

TRACK-HOLD COMMAND—A TTL logic "1" applied to pin 1 will put the MN374 into the track (sample) mode. In this mode, the device acts as an inverting unity-gain amplifier, and its output will follow (track) its input. A logic "0" applied to pin 1 will put the MN374 into the hold mode, and after the switching transient settles, the output will be held constant at the level present when the hold command was given.

USING MN374 WITH SUCCESSIVE APPROXIMATION A/D CONVERTERS—Successive approximation (SA) type A/D converters are oftentimes severely analog input slew-rate and bandwidth limited and can easily produce errors when used to digitize dynamically changing signals. These input-signal bandwidth limitations arise from the fact that successive approximation type A/D's sequentially determine output-bit values (from MSB to LSB) by comparing the analog equivalent of output bits already determined to the instantaneous analog input signal. The conversion process demands that the analog input signal remain "constant", and the analog input slew-rate and bandwidth limitations derive from the requirement that input signals not change more than ± ½ LSB (for the appropriate resolution) during the conversion period.

These A/D converter input-bandwidth limitations can be overcome by using track-hold (T/H) amplifiers to track and subsequently "freeze" (hold) analog input signals that are changing too rapidly for the A/D alone to accurately digitize. If other parameters are appropriate, the slew-rate and bandwidth limiting factor of the T/H-A/D combination will become the T/H's aperture jitter (aperture uncertainty), and the T/H-A/D combination will now be able to accurately sample and digitize signals slewing as much as ± ½LSB during the T/H's aperture jitter time. The formulas for determing how fast a signal a given T/H can accurately capture when used in conjunction with a given A/D converter are the same as those stated above with ± ½LSB defined for the A/D converter and with the variable (conversion time) replaced by aperture jitter. Needless to say, aperture jitter is a significantly smaller number than conversion time, and the bandwidth improvement when using the T/H vs. not using the T/H will equal the ratio of A/D conversion time to T/H aperture jitter.

$$\text{Input Slew Rate Limit} = \frac{\pm \frac{1}{2}\text{LSB}}{\text{Conversion Time}}$$

$$\text{Input Bandwidth*} = \frac{\pm \frac{1}{2}\text{LSB}}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

$$\text{Input Bandwidth*} = \frac{(\text{FSR}/2^{n+1})}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

*For full scale sine waves
FSR = A/D converter full scale range
n = resolution in bits

As an example, consider Micro Networks MN5295 16-bit A/D converter. This device guarantees "no missing codes" to the 14-bit level, and it performs a full 16-bit conversion in 17μsec (maximum). For this device operating on its full ± 10V input voltage range, ± ½LSB/conversion time = ±0.61mV/17μsec = ±0.036mV/μsec (calculated for a 14-bit LSB). This is equivalent to the highest slew rate encountered in a full-scale (± 10V) sine wave with a frequency of 0.57Hz. When used in conjunction with MN5295, MN374 with its 400psec aperture jitter, is capable of capturing signals (to 14-bit accuracy) with slew rates up to ± ½LSB/aperture jitter = ± 0.61mV/400psec = ±1.525V/μsec. This is the highest slew rate one would encounter in a full-scale sine wave with a frequency of 24.3kHz. As expected, the improvement ratio of 24.3kHz to 0.57Hz is equal to the ratio of 17μsec to 400psec.

Using T/H's in conjunction with A/D's to increase analog bandwidth will reduce throughput (conversion rate) in that new digital output data cannot be realized until after the T/H has acquired a new signal (acquisition time) and the A/D has converted it (conversion time). Another consideration when calculating T/H-A/D throughput is the T/H's Track-to-Hold Transient Setting Time. If the same timing pulse is used to put the T/H into the hold mode and initiate the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable and accurate input when it makes the final decision on whether its MSB output should be "1" or "0". This decision normally takes place one clock period after a conversion has begun.

Other considerations when using T/H's with successive approximation A/D's involve the T/H's output stage. In the hold mode, it should exhibit a very low output impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency. Also, the T/H should be able to fully recover (to ± ½LSB) from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source high frequency current transients and recover within one clock period. The MN374 output is not current limited, and in the hold mode, output impedance is typically below 1Ω. It recovers from output current transients (to ± 0.003%FSR) in well under 1μsec.

For slower speed A/D converters, the most popular technique used to control the T/H's operation is to drive the T/H directly with the A/D's status line. For virtually all high-resolution A/D's in use today, including MN5295/5296, this technique does *not* work because the T/H's track-to-hold transients will

not reliably settle fast enough. The application described below is a much more cautious way to control the T/H-A/D timing because it uses a timed one-shot to delay the start of the A/D conversion. The circuit allocates a predetermined amount of time for the track-to-hold transient to fully settle before initiating the A/D conversion. After the conversion has been completed, the circuit immediately drives the T/H back into the track mode.

The principles discussed below are general and can be used for virtually any T/H-A/D combination. The system is run by an externally applied clock whose frequency determines the overall sampling/digitizing rate. Please refer to the timing and schematic diagrams below as well as the MN5295/96 data sheet.

The system consists of the A/D, the T/H, a single one-shot and a dual flip-flop. The falling edge of the system clock triggers the 74LS123 one-shot, and the system clock can have any duty cycle as long as it has a minimum positive pulse width of 50nsec to accommodate the setup-time requirement of the one-shot.

The one-shot produces a 500nsec pulse, and both the Q and $\overline{Q}$ outputs are utilized. The Q output becomes the start pulse for the MN5295/5296, and the $\overline{Q}$ output drives the set pin of the first half of the 74LS74 flip-flop. The $\overline{Q1}$ output of the flip-flop controls the operational mode of the MN374 T/H. The falling edge of the $\overline{Q}$ output of the 74LS123 asynchronously sets the flip-flop driving its Q1 output high and its $\overline{Q1}$ output low. The MN374, which has an active-low control line, is immediately driven into its hold mode by the falling edge of $\overline{Q1}$.

The pulse width of the 74LS123 has been selected so that there is now ample time for the MN374 track-to-hold transient to fully decay before the A/D conversion begins. After 500nsec, the Q output of the one-shot drops to "0" initiating the A/D conversion, and driving the Status output (pin 1) of the A/D to a "1". The T/H remains in hold because the rising edge of the $\overline{Q}$ output of the one-shot does not affect the first flip-flop. The rising edge of Status asynchronously resets the second flip-flop driving the Q2 output low.

The T/H remains in the hold mode for the next 17μsec as the A/D completes its conversion. At the end of the conversion, the A/D's Status line drops to a "0", and this sets the second flip-flop. The Q2 output goes high clocking the first flip-flop which has a "0" on its D line. This forces the Q1 output low and the $\overline{Q1}$ output high driving the T/H back into the signal-acquisition (track) mode.

The status of this system can be monitored at a number of different points. Whenever pin 1 (Status) of MN5295/5296 is a logic "1", the A/D is performing a conversion, and output data is not valid. The falling edge of this line signals that the conversion is complete and that output data is now valid. The Q1 output of the first flip-flop can be used to monitor the T/H. Whenever this line is a "1", the T/H is in the hold mode. When it is a "0", the T/H is in the track mode. The falling edge here also indicates that a conversion has just been completed and that output data is now valid. If an external latch is to be used to clock data away from MN5295/5296, either of the falling edges described above may be used to strobe the latch.

Remember that the above application does not automatically take care of the T/H acquisition time and that this time must be allowed for in determining the external clock period. If the MN5295/5296 requires 17μsec to make a conversion, and the T/H requires 4μsec for acquisition time, adding 2μsec of overhead time yields a period of 23μsec. That means the system can be clocked at 43kHz and still be guaranteed to meet full accuracy and linearity performance.

It is unnecessary to have the 74LS123 one-shot in the application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 43kHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5295/5296 directly, and it can be inverted to drive the 74LS74.