MN3880S

NTSC CCD Video Signal Delay Element

■ Overview

The MN3880S is a CCD signal delay element for video signal processing applications.

It contains such components as a shift register clock driver, charge I/O blocks, two CCD delay elements, a clamp bias circuit, resampling output amplifiers, and booster circuits.

The MN3880S samples the input using the supplied clock signal with a frequency of 7.15909 MHz, twice the NTSC color signal subcarrier frequency, and after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines.

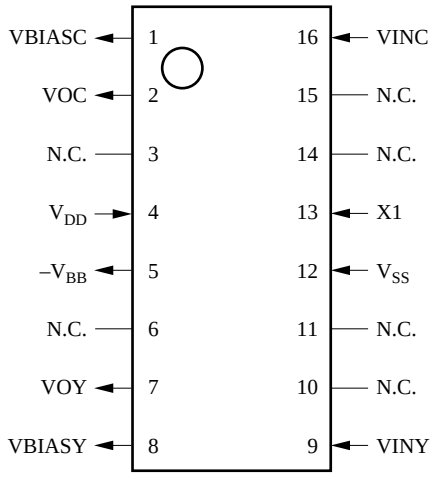
■ Features

- Single 4.9 V power supply
- Single chip combining luminance signal delay element and delay element for chrominance signal after passing through a low pass filter

■ Applications

- VCRs

■ Pin Assignment



(TOP VIEW)

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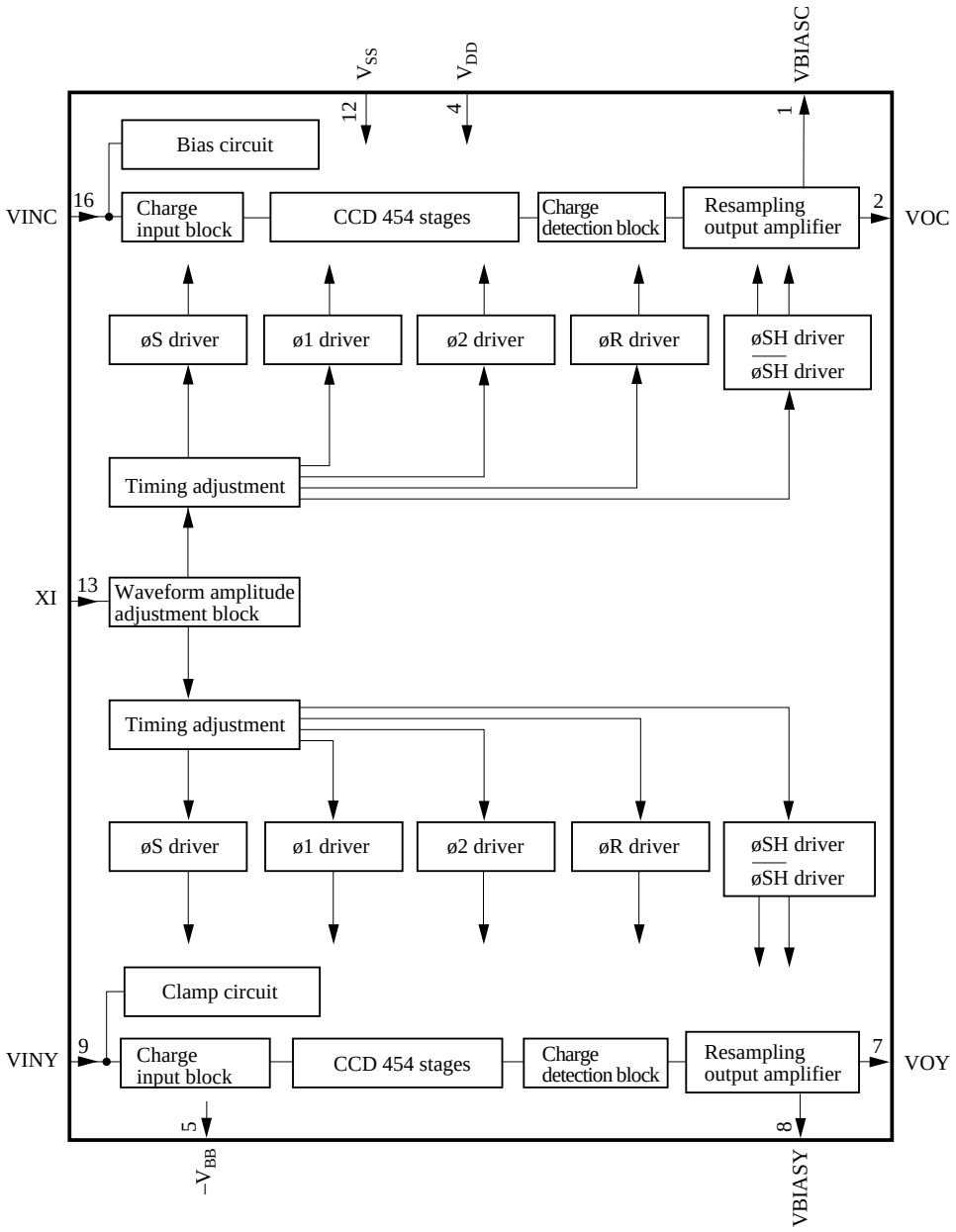
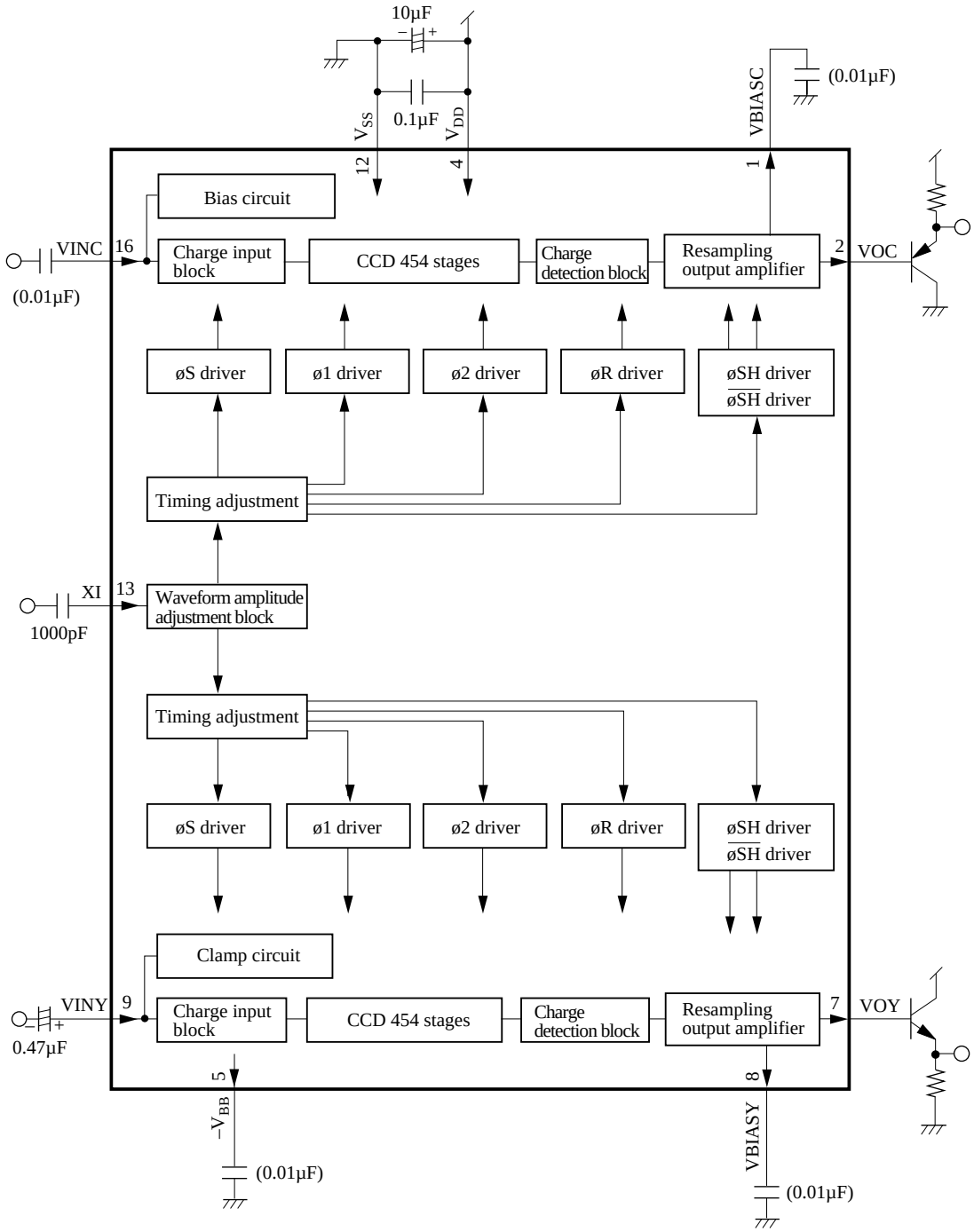
■ Block Diagram



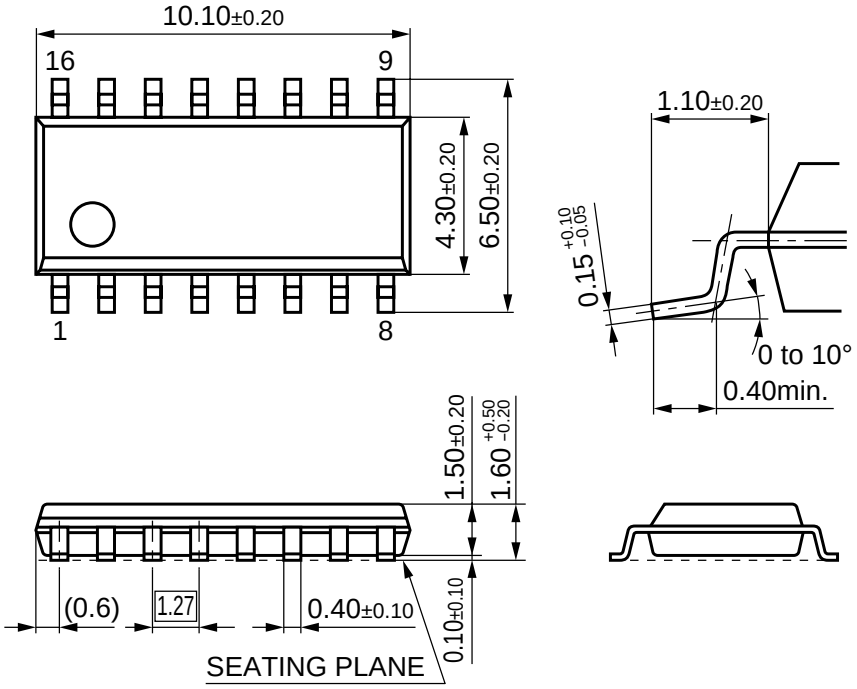
■ Pin Descriptions

Pin No.	Symbol	Pin Name	Remarks
1	VBIASC	Output gate connection (C)	
2	VOC	Signal output (C)	
3	N.C.	No connection	
4	V_{DD}	Power supply	
5	$-V_{BB}$	Substrate connection	Negative voltage pin
6	N.C.	No connection	
7	VOY	Signal output (Y)	
8	VBIASY	Output gate connection (Y)	
9	VINY	Signal output (Y)	
10	N.C.	No connection	
11	N.C.	No connection	
12	V_{SS}	GND	
13	XI	Clock input	
14	N.C.	No connection	
15	N.C.	No connection	
16	VINC	Signal output (C)	

■ Application Circuit Example



Note: If the external capacitor attached to pin 5 is an electrolytic capacitor, attach the negative pole to pin 5.

■ Package Dimensions (Unit:mm)

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