New

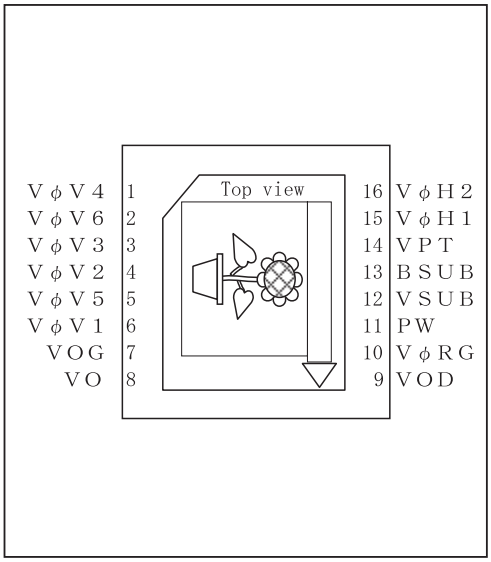
Panasonic

Opposing corner 7.17mm(1/2.5type) 3.34 million pixels

CCD Area Image Censor MN39592PJ

■ Overview

MN39592PJ is a CCD ½.5 3.34 million pixels area image sensor suits high-quality digital still camera.On-chip color filter presents excellent color repeatability by adopting RGB bayer. It also keeps 3.34 million total number of pixels(Horizontally:2.140 × Vertically: 1.560) to hold stable and high-quality pictures.



■ Features

- Available pixel number 2.088(horizoontal), 1,550(vertical)
- Supersensitivity
- Low-smear
- Square pixel alignment
- Lower power consumption by adopting horizontal CCD, 3.3V
- 16-pin plastic package

■ Applications

Digital still camera

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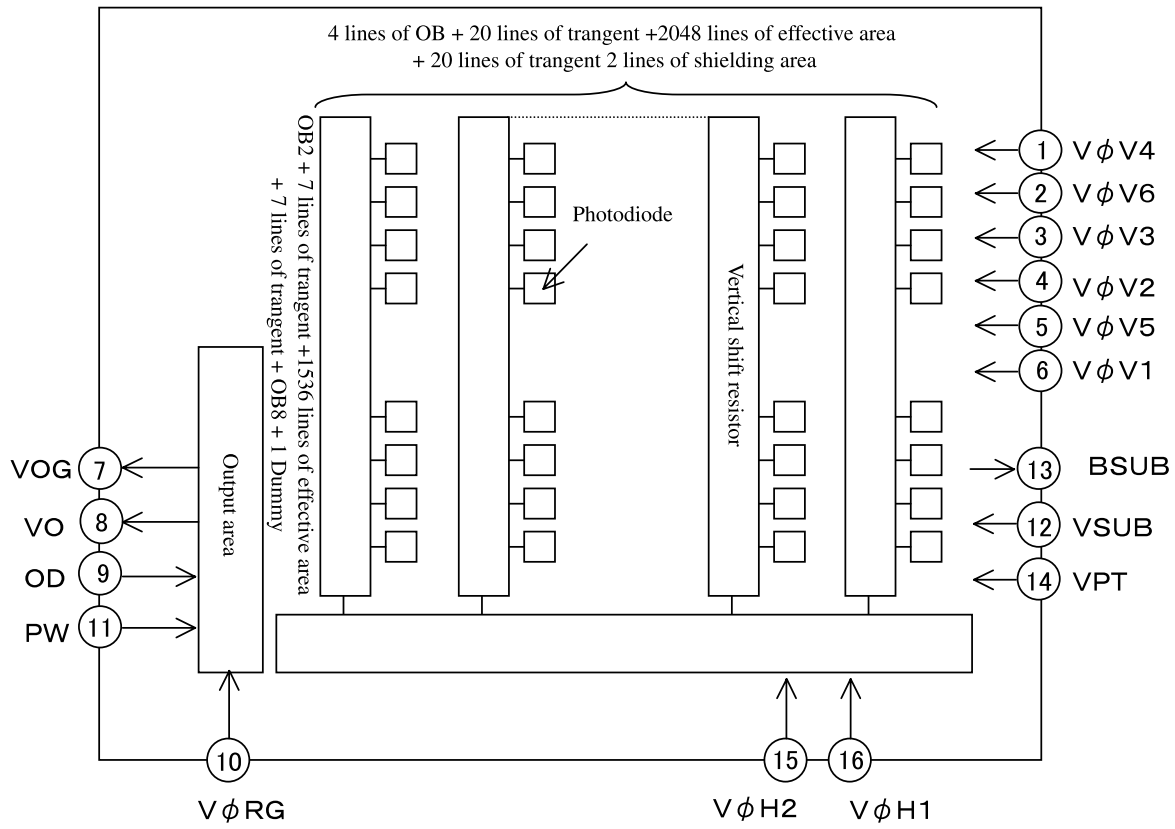
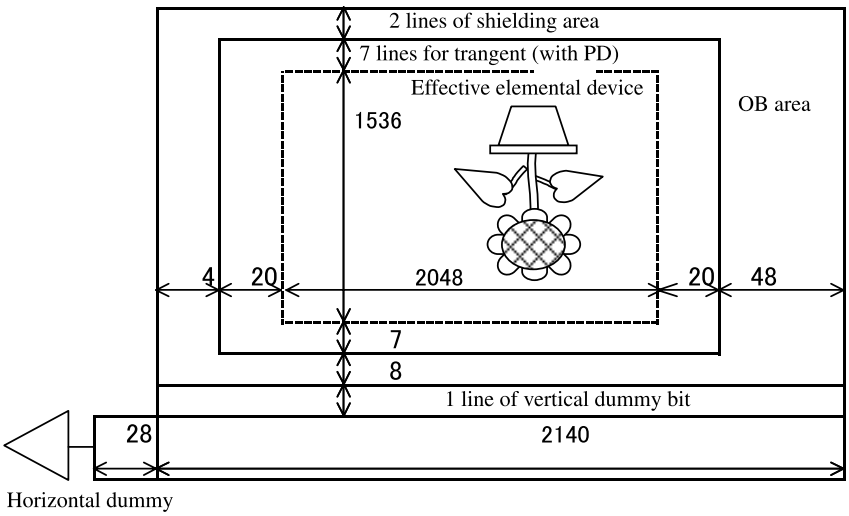
E00125AE

New publication, effective from Jun.04 2002.

■ Block Diagram



■ Elemental device structure

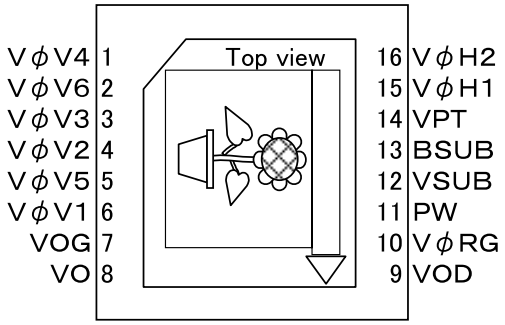


■ Terminal description

1. Terminal description

Terminal No	Name	Terminal description
1 pin	VφV4	Vertical shift register clock pulse (4)
2 pin	VφV6	Vertical shift register clock pulse (6)
3 pin	VφV3	Vertical shift register clock pulse (3)
4 pin	VφV2	Vertical shift register clock pulse (2)
5 pin	VφV5	Vertical shift register clock pulse (5)
6 pin	VφV1	Vertical shift register clock pulse (1)
7 pin	VOG	Output gate
8 pin	VO	CCD output
9 pin	VOD	Output drain
10 pin	VφRG	Reset pulse
11 pin	PW	GND
12 pin	VSUB	Circuit board
13 pin	BSUB	Breeder SUB
14 pin	VPT	Protection P wel
15 pin	VφH1	Horizontal shift resistor clock pulse (1)
16 pin	VφH2	Horizontal shift resistor clock pulse (2)

2. Alignment of terminals



3. Device parameter

Parameter	Numeric value	Unit
Total pixel number	2,140(H) × 1,560(V) = 3,338,400	pcs
Available pixel number (including trangents)	2,088(H) × 1,550(V) =3,236,400	pcs
Effective pixel numbers	2,048(H) × 1,536(V) =3,145,728	pcs
Pixel size	2.8 × 2.8	μm^2
Effective picture size	5.7344(H) × 4.3008(V)	μm^2

■ Absolute maximum ratings

Terminal name		PW		PT		SUB		Note
	Unit	High	Low	High	Low	High	Low	
VOD	V	15.0	-0.2	-		15.0	-25.0	Note 1,2
VPT	V	0.2	-10.0	Standard		0.2	-35.0	
PW	V	Standard		10.0	-0.2	0.2	-25.0	
Vsub	V	25.0	-0.2	35.0	-0.2	Standard		Note 1
BSUB	V	15.0	-0.2	-		15.0	-25.0	
VOG	V	5.0	-0.2	-		5.0	-25.0	
VϕRG	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
VϕH1	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
VϕH2	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
VϕV1, 5	V	15.0	-10.0	25.0	-0.2	15.0	-35.0	
VϕV2	V	12.0	-10.0	22.0	-0.2	12.0	-35.0	
VϕV3,6	V	15.0	-10.0	25.0	-0.2	15.0	-35.0	
VϕV4	V	12.0	-10.0	22.0	-0.2	12.0	-35.0	
VO	V	15.0	-10.0	-		15.0	-35.0	Note 2

■ Absolute maximum ratings between gates

Terminal name	Unit	High	Low	Note
Horizontal clock input terminal (between VϕV1 and VϕV6)	V	12.0	-10.0	Note 3
Vertical clock input terminal (between VϕV1 and VϕV6)	V	5.0	-5.0	
VϕH1-VϕV4	V	12.0	-12.0	

■ Operation temperature

Parameter	Unit	High	Low	Note
Operation temperature	°C	60	-10.0	

Note 1. Always keep VOD-Vsub ≦10V.

Note 2. Always keep VOD-VO≦5V.

Note 3. When clock width < 10μs, Dudy<0.1%, 25V is guaranteed.

■ Imaging characteristics

Testing specification (Tentative)

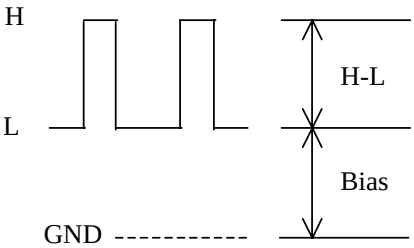
Parameter		Symbol	Condition	Test point	Min.	Standard	Max.	Unit
Saturation power		Vsat	F1.4:J chart	Signal output	500	550		mV
Sensitivity	(G)	SoG	F8:J chart (1/7.5 accumulated conversion value)	Signal output	200	235	285	mV
	(R)	SoR		Signal output	120	165	205	
	(B)	SoB		Signal output	90	110	140	
Sensitivity ratio	R/G		Sensitivity measurement conditions	Signal output	0.42	0.70	1.03	
	B/G			Signal output	0.31	0.47	0.70	
Smear	Frame monitors	Sm	1/10V	G signal output		-87	-81	dB
						-77	-71	
OB bump			60°C light shielding	Signal output	-0.6	0	0.6	mV
Color shading (1)(2)			Standard light sensitivity	Average signal output		4.0	8.0	%
Dark signal			Ta=60°C,1/5.24 second accumulation shielding condition	Signal output		3.0	6.0	mV
Dark signal shading (H, V)			Ta=60°C,1/5.24 second accumulation shielding condition	Signal output		4.0	6.0	mV
Blooming control circuit voltage		Vsub	1000 times more light than normal amount	Monitor	No blooming caused by the inner voltage of Vsub			
ϕ VH voltage reliability (Shutter with a scratch)			1/8 times more light than normal amount	Monitor	No scratches under the condition of ϕ VH voltage operation			
OB transmission			One hundred thousand times more light than normal amount	Signal output	Less than 10mV of OB signal output			

Note: above values are testing values only.

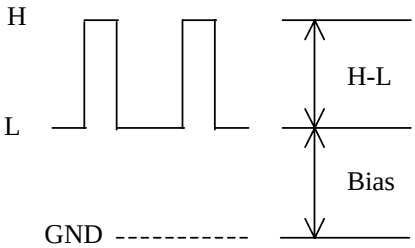
■ Clock power voltage conditions

Terminal name		Unit	Operating conditions			Note
			Max.	Standard	Min.	
VOD		V	12.0	12.0	-11.5	
VPT		V	-7.5	-8.0	-8.5	
PW		V	-	0	-	
VOG		V	Inside			
VϕRG	H-L		3.6	3.3	3.0	Note 1
	Bias	V	Inside			
VϕH1	H	V	3.6	3.3	3.0	Note 3
	L	V	0.2	0	-0.2	
VϕH2	H	V	3.6	3.3	3.0	
	L	V	0.2	0	-0.2	
Vsub	Bias	V	Inside			Note2
	ϕVsub	V	21.0	20.0	19.0	
VϕV1 VϕV5	H	V	12.5	12.0	11.5	Note 4
	M	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
VϕV2	M	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
VϕV3 VϕV6	H	V	12.5	12.0	11.5	
	M	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
VϕV4	M	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
IOD		mA		43		

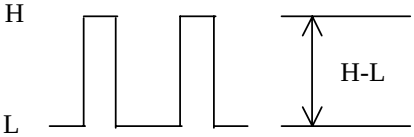
Note 1) Reset (VϕRG)



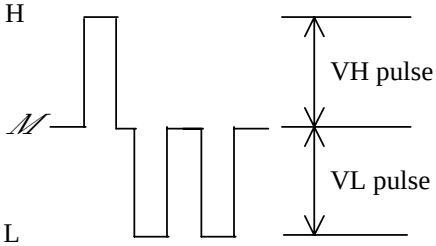
Note 2) Circuit board (VϕVSUB)



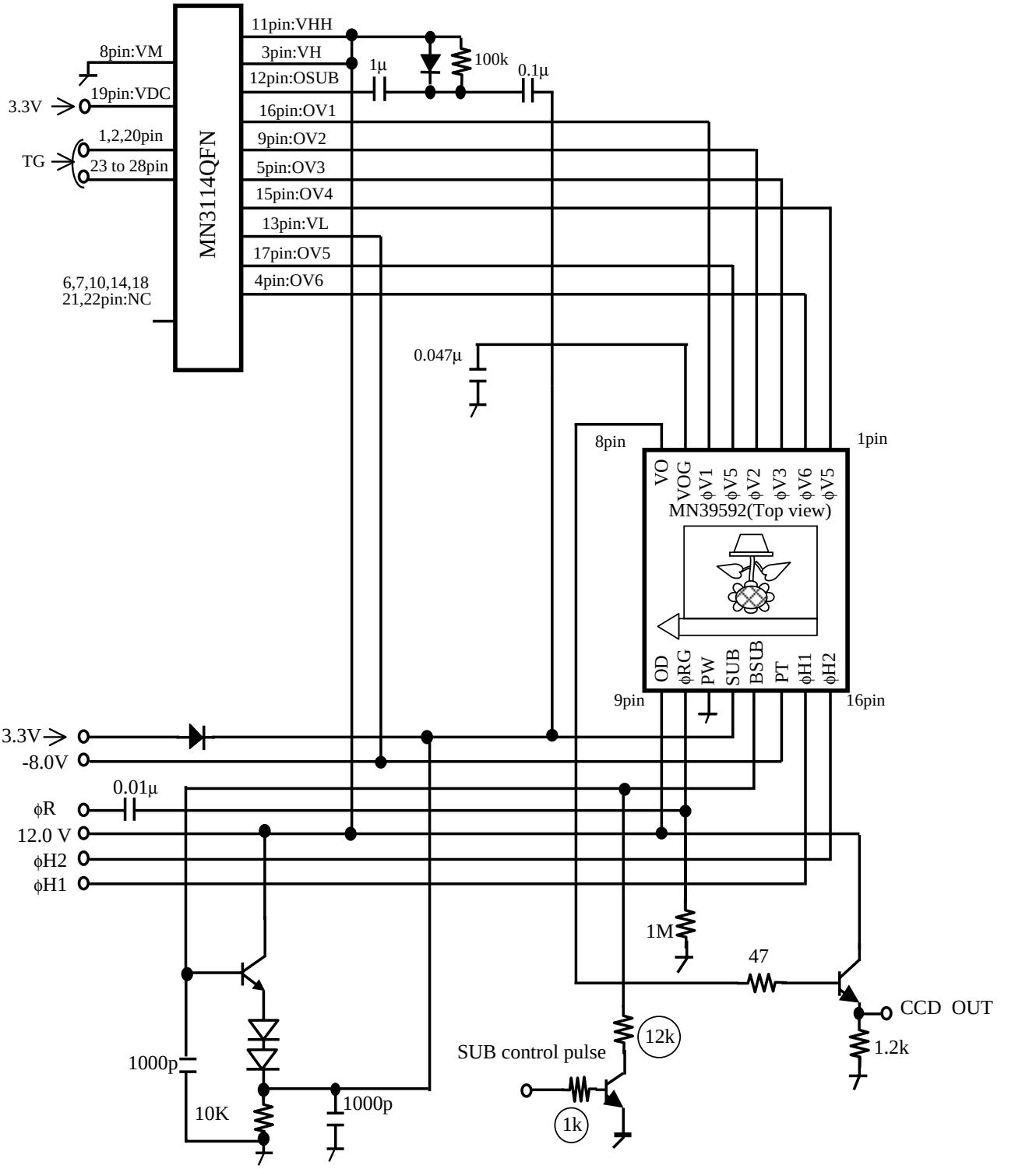
Note 3) Horizontal shift resistor (VϕH1, VϕH2)



Note 4) Vertical shift resistor (VϕV1 to V6)

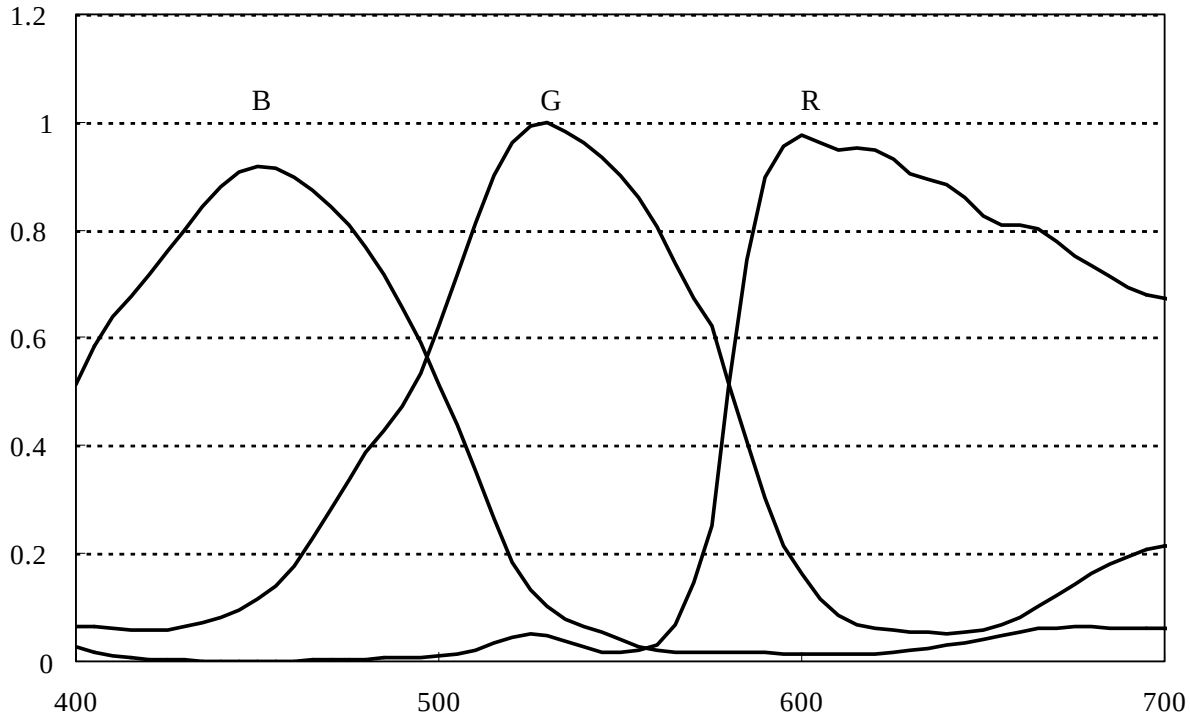


■ Recommended circuit example



Adjustment of Base resistance 1kΩ is required depending on the ability of current supply of SUB control pulse output circuit.

■ Characteristics of prismatic



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