

MN4006B/MN4006BS

18-Bit Static Shift Registers

Description

The MN4006B/S are maximum 18-bit static shift registers composed of two 4-bit shift registers and five 5-bit shift registers. Clock pulses for all registers are input through the common CP. By properly combining input and output, shift registers with the arbitrary stages of 4, 5, 8, 9, 10, 12, 13, 14, 16 and 17 are enabled.

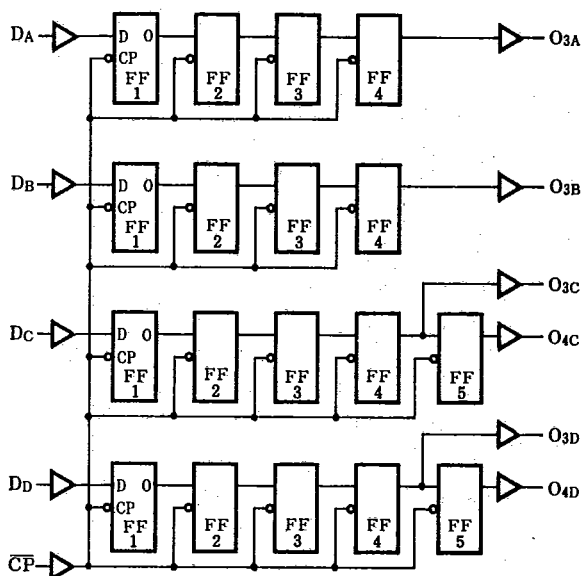
The MN4006B/S are equivalent to MOTOROLA MC14006B and RCA CD4006B.

Truth Table

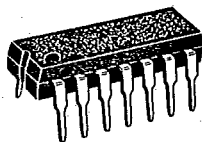
D_n	$\overline{CP}$	O_{n+1}
D_i		D_i
X		no change

Note) X : don't care

Logic Diagram



P-1



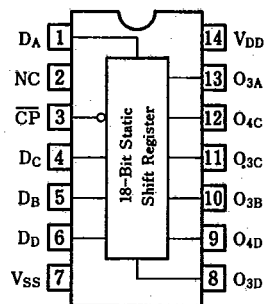
14-Pin • Plastic DIL Package

P-2



14-Pin • Pinflat Package (SO-14D)

Pin Configuration



■ Maximum Ratings (Ta=25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	$-0.5 \sim +18$	V
Input Voltage		V_I	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		V_O	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta = -40 ~ +60°C	P_D	max. 400	mW
	Ta = +60 ~ +85°C		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		T_{opr}	$-40 \sim +85$	°C
Storage Temperature		T_{stg}	$-65 \sim +150$	°C

* $V_{DD} + 0.5V$ should be under 18V

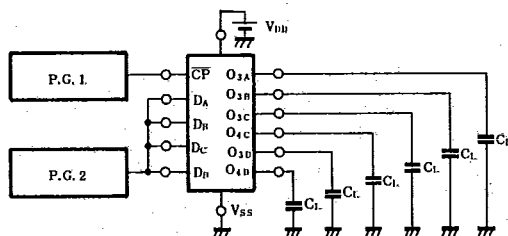
■ DC Characteristics (V_{SS}=0V)

Item	V _{DD} (V)	Sym- bol	Conditions	Ta = -40°C		Ta = 25°C		Ta = 85°C		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_I = V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_O < 1\mu A$ $V_O = 0.5V$ or $4.5V$	—	1.5	—	1.5	—	1.5	V
	10		$ I_O < 1\mu A$ $V_O = 1V$ or $9V$	—	3	—	3	—	3	
	15		$ I_O < 1\mu A$ $V_O = 1.5V$ or $13.5V$	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_O < 1\mu A$ $V_O = 0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	—	V
	10		$ I_O < 1\mu A$ $V_O = 1V$ or $9V$	7	—	7	—	7	—	
	15		$ I_O < 1\mu A$ $V_O = 1.5V$ or $13.5V$	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O = 0.4V$, $V_I = 0V$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_O = 0.5V$, $V_I = 0V$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_O = 1.5V$, $V_I = 0V$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 4.6V$, $V_I = 0V$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_O = 9.5V$, $V_I = 0V$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_O = 13.5V$, $V_I = 0V$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 2.5V$, $V_I = 0V$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0V$ or $15V$	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, Vss=0V, CL=50pF)

Item	VDD (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP} \rightarrow On(H \rightarrow L)$	5	t_{PHL}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{CP} \rightarrow On(L \rightarrow H)$	5	t_{PLH}	—	90	270	ns
	10		—	40	120	
	15		—	35	105	
Minimum Clock Pulse Width	5	t_{WCPH}	—	30	90	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time $D_n \rightarrow \overline{CP}$	5	t_{su}	—	10	30	ns
	10		—	5	15	
	15		—	0	10	
Hold Time $D_n \rightarrow \overline{CP}$	5	t_{hold}	—	-5	10	ns
	10		—	0	10	
	15		—	0	10	
Maximum Clock Frequency	5	f_{max}	9	18	—	MHz
	10		15	30	—	
	15		18	36	—	
Input Capacitance		C_i	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms

