

MN4076B / MN4076BS

4-Bit D-Type Registers

Description

The MN4076B/S are 4-bits registers composed of quad D-type flip-flops with tristate outputs and controlled by the common clock and reset inputs.

All inputs ($D_0 \sim D_3$) are stored in four flip-flops on the positive going edge of the clock, when the data enable inputs ($\overline{ED}_0, \overline{ED}_1$) are Low.

In other combinations of the data enable inputs, 4 flip-flops hold the previous stage even after the going edge of the clock.

When output enable inputs ($\overline{EO}_0, \overline{EO}_1$) are Low, each flip-flop's outputs are from $O_0 \sim O_3$.

In other combinations of the output enable inputs, all outputs are High impedance.

A High on the reset input makes outputs Low asynchronously.

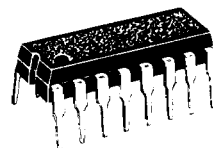
The MN4076B/S are equivalent to MOTOROLA MN14076B and RCA CD4076B.

Truth Table

MR	CP	Input		D_0	$\overline{EO}_0$	$\overline{EO}_1$	Output O_{0n+1}
		$\overline{ED}_0$	$\overline{ED}_1$				
	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L		H	X	X	L	L	no change
L		X	H	X	L	L	no change
L		L	L	H	L	L	H
L		L	L	L	L	L	L
L		X	X	X	L	L	no change
L	X	X	X	X	L	L	no change

Note) X : don't care
Z : high impedance

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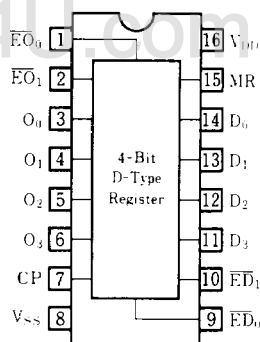
16-Pin • Plastic DIL Package

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16-Pin • Panaflat Package (SO-16D)

Pin Configuration



Pin Explanation

$D_0 \sim D_3$: Data input (4 Bits)

$\overline{ED}_0, \overline{ED}_1$: Data enable input

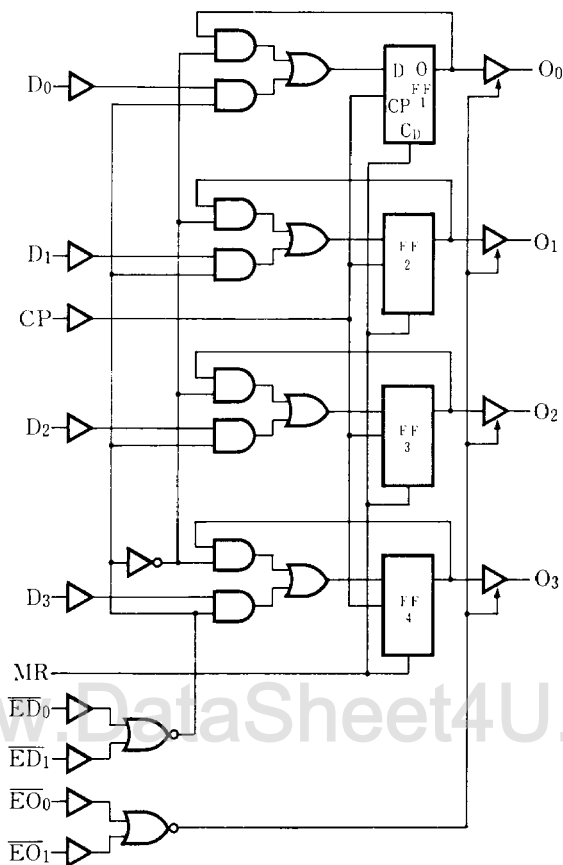
$\overline{EO}_0, \overline{EO}_1$: Output enable input

CP : Clock input

MR : Reset input

$O_0 \sim O_3$: Data output (4 Bits)

■ Logic Diagram



■ Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	$-0.5 \sim +18$	V
Input Voltage	V_I	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage	V_O	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current	$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta = $-40 \sim +60^\circ\text{C}$	max. 400	mW
	Ta = $+60 \sim +85^\circ\text{C}$	Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	Topr	$-40 \sim +85$	°C
Storage Temperature	Tstg	$-65 \sim +150$	°C

* $V_{DD} + 0.5\text{V}$ should be under 18V

■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Sym- bol	Conditions	$T_a=-40^{\circ}C$		$T_a=25^{\circ}C$		$T_a=85^{\circ}C$		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_i=V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_i=V_{SS}$ or V_{DD} $ I_O < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_i=V_{SS}$ or V_{DD} $ I_O < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_O < 1\mu A$ $V_O=0.5V$ or $4.5V$ $V_O=1V$ or $9V$ $V_O=1.5V$ or $13.5V$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_O < 1\mu A$ $V_O=0.5V$ or $4.5V$ $V_O=1V$ or $9V$ $V_O=1.5V$ or $13.5V$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O=0.4V$, $V_i=0$ or $5V$ $V_O=0.5V$, $V_i=0$ or $10V$ $V_O=1.5V$, $V_i=0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=4.6V$, $V_i=0$ or $5V$ $V_O=9.5V$, $V_i=0$ or $10V$ $V_O=13.5V$, $V_i=0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=2.5V$, $V_i=0$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_i$	$V_i=0$ or $15V$	—	0.3	—	0.3	—	1	μA
3-State Output Pin	Leakage Current High Level	15	I_{OZH} $V_O=V_{DD}$	—	1.6	—	1.6	—	12	μA
	Leakage Current Low Level	15	$-I_{OZL}$ $V_O=V_{SS}$	—	1.6	—	1.6	—	12	

■ Switching Characteristics ($T_a=25^{\circ}C$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	150	450	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	

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