MN4094B/MN4094BS

8-Stage Shift-and-Store Bus Register

■ Outline

The MN4094B/S is a shift-and-store bus register consisting of an 8-bit shift register and an 8-bit latch.
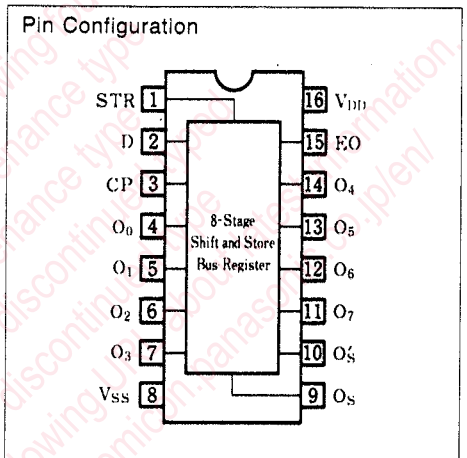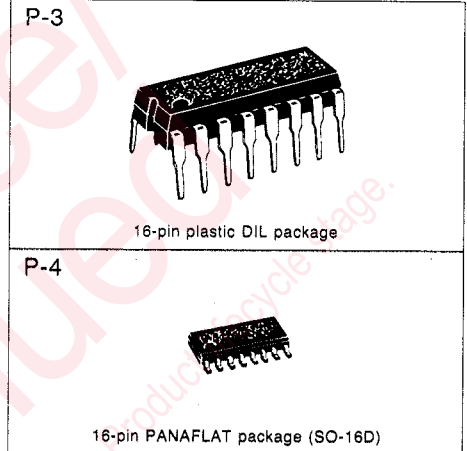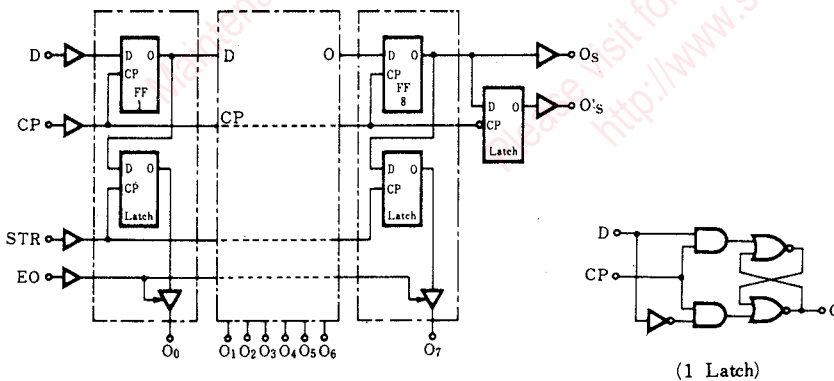
It is possible to hold the output in the data transfer mode since each data read in the shift register can be read into the latch by the asynchronous strobe input. The parallel outputs can be directly connected to an 8-bit bus line since they are of 3-state structure. This shift-and-store bus register is suitable for application to a data serial/parallel converter, a data receiver, etc.

■ Truth Table

Input				Parallel Output		Serial Output	
CP	EO	STR	D	O_0	O_n	O_s	O'_s
↗	L	×	×	Z	Z	O'_6	nc
↘	L	×	×	Z	Z	nc	O_7
↗	H	L	×	nc	nc	O'_6	nc
↗	H	H	L	L	O_{n-1}	O'_6	nc
↗	H	H	H	H	O_{n-1}	O'_6	nc
↘	H	H	H	nc	nc	nc	O_7

Note) × : don't care
Z : High impedance
nc : No change
O'_6 : State of shift resistor at 7th stage

■ Logic Diagram

(1 Latch)

P-3

16-pin plastic DIL package

P-4

16-pin PANAFLAT package (SO-16D)

Pin Configuration

STR	1	16 V_{DD}
D	2	15 EO
CP	3	14 O_4
O_0	4	13 O_5
O_1	5	12 O_6
O_2	6	11 O_7
O_3	7	10 O'_s
V_{SS}	8	9 O_s

8-Stage Shift and Store Bus Register

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■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	$-0.5 \sim +18$	V
Input voltage		V_I	$-0.5 \sim V_{DD}+0.5^*$	V
Output pin voltage		V_O	$-0.5 \sim V_{DD}+0.5^*$	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=$-40 \sim +60$°C	P_D	max. 400	mW
	Ta=$+60 \sim +80$°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	$-40 \sim +85$	°C
Storage temperature		T_{stg}	$-65 \sim +150$	°C

* $V_{DD}+0.5$V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item		V_{DD} (V)	Symbol	Condition	Ta=-40°C		Ta=25°C		Ta=85°C		Unit
					min.	max.	min.	max.	min.	max.	
Static supply current		5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
		10			—	40	—	40	—	300	
		15			—	80	—	80	—	600	
Output voltage low level		5	V_{OL}	V_I=V_{SS} or V_{DD} $|I_O|<1\mu$A	—	0.05	—	0.05	—	0.05	V
		10			—	0.05	—	0.05	—	0.05	
		15			—	0.05	—	0.05	—	0.05	
Output voltage high level		5	V_{OH}	V_I=V_{SS} or V_{DD} $|I_O|<1\mu$A	4.95	—	4.95	—	4.95	—	V
		10			9.95	—	9.95	—	9.95	—	
		15			14.95	—	14.95	—	14.95	—	
Input voltage low level		5	V_{IL}	V_O=0.5V or 4.5V $|I_O|<1\mu$A	—	1.5	—	1.5	—	1.5	V
		10		V_O=1V or 9V	—	3	—	3	—	3	
		15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level		5	V_{IH}	V_O=0.5V or 4.5V $|I_O|<1\mu$A	3.5	—	3.5	—	3.5	—	V
		10		V_O=1V or 9V	7	—	7	—	7	—	
		15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level		5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
		10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
		15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level		5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
		10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
		15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level		5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input leakage current		15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-state output pin	Leakage current high level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
	Leakage current low level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

■ Switching Characteristics (Ta=25°C, V$_{SS}$=0V, C$_L$=50pF)

Item	V$_{DD}$(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5		—	60	180	
	10	t$_{TLH}$	—	30	90	ns
	15		—	20	60	
Output fall time	5		—	60	180	
	10	t$_{THL}$	—	30	90	ns
	15		—	20	60	
Propagation time CP→Os (H→L)	5		—	135	405	
	10	t$_{PHL}$	—	65	195	ns
	15		—	50	150	
Propagation time CP→Os (H→H)	5		—	105	315	
	10	t$_{PLH}$	—	50	150	ns
	15		—	40	120	
Propagation time MR→O's (H→L)	5		—	105	315	
	10	t$_{PHL}$	—	50	150	ns
	15		—	40	120	
Propagation time MR→O's (L→H)	5		—	105	315	
	10	t$_{PLH}$	—	50	150	ns
	15		—	40	120	
Propagation time CP→On (H→L)	5		—	165	495	
	10	t$_{PHL}$	—	75	225	ns
	15		—	55	165	
Propagation time CP→On (L→H)	5		—	150	450	
	10	t$_{PLH}$	—	70	210	ns
	15		—	55	165	
Propagation time STR→On (H→L)	5		—	110	330	
	10	t$_{PHL}$	—	50	150	ns
	15		—	35	105	
Propagation time STR→On (L→H)	5		—	100	300	
	10	t$_{PLH}$	—	45	135	ns
	15		—	35	105	
High level output disable time EO→On (H)	5		—	75	225	
	10	t$_{PHZ}$	—	40	120	ns
	15		—	30	90	
Low level output disable time EO→On (L)	5		—	80	240	
	10	t$_{PLZ}$	—	40	120	ns
	15		—	30	90	
High level output enable time EO→On (H)	5		—	40	120	
	10	t$_{PZH}$	—	25	75	ns
	15		—	20	60	
Low level output enable time EO→On (L)	5		—	40	120	
	10	t$_{PZL}$	—	25	75	ns
	15		—	20	60	
Set-up time D→CP	5		—	30	90	
	10	t$_{su}$	—	10	30	ns
	15		—	5	15	

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■ Switching Characteristics (cont.)

Item	$V_{DD}(V)$	Symbol	min.	typ.	max.	Unit
Hold time D→CP	5	t_{hold}	5	−15	—	ns
	10		20	5	—	
	15		20	5	—	
Minimum clock pulse width	5	t_{WCPL}	60	20	—	ns
	10		30	15	—	
	15		24	12	—	
Minimum strobe pulse width	5	t_{WSTRH}	40	20	—	ns
	10		30	15	—	
	15		24	12	—	
Maximum clock frequency	5	f_{max}	5	10	—	MHz
	10		11	22	—	
	15		14	28	—	
Input capacitance		C_l	—	—	7.5	pF

■ Timing diagram

Clock Input(CP)

Data Input(D)

Strobe Input(STR)

Output Enable Input(EO)

Internal(O'_0)(FF 1)

Output(O_0)

Internal(O'_6)(FF7)

Output(O_6)

Serial Output(O_S)

Serial Output(O'_S)

Z·state

Z·state
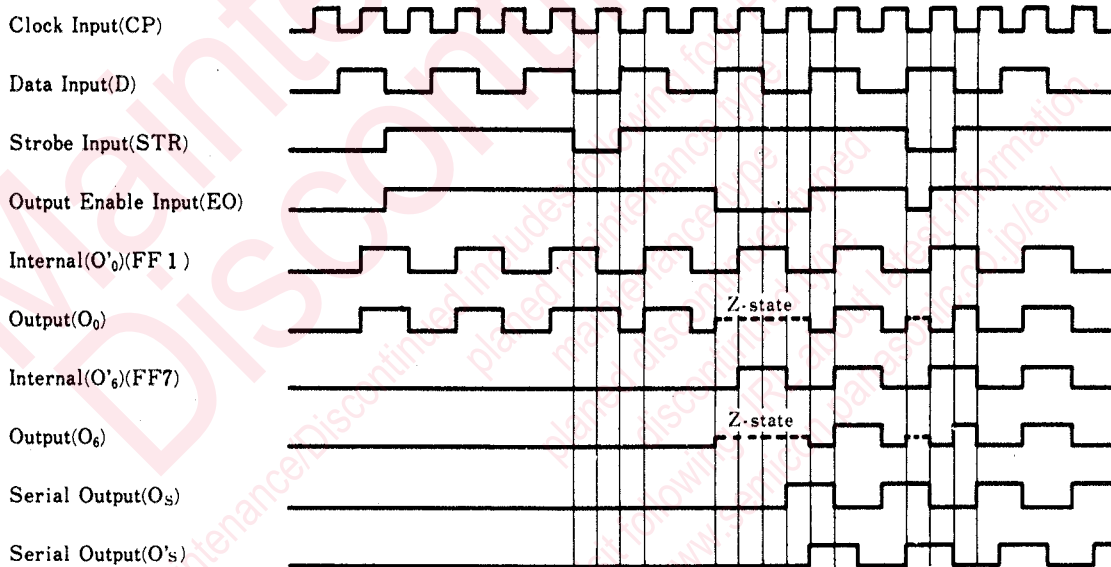
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