MN4517B / MN4517BS

Dual 64-Bit Static Shift Registers

■ Description

The MN4517B/S are dual 64-bit static shift registers which have two independent 64-bit registers.
Each register can be used independently since they have their own clock input and write enable.
Outputs of 16, 32, 48 and 64 bits are available.
Data added in the data input is input to the register by clock regardless of the write enable input mode.
When wire enable input becomes "H" level, output becomes disable (high impedance mode), and when the clock pulse is applied, it is input to the input data 16, 32 and 48-bit tapes.
Accordingly, the contents of 64 bit is filled by 16 clock pulses.
Tap output at every 16 bits can also be used for bus-logic.
The MN4517B/S are used in time-delay circuits, tentative memory circuits, etc.

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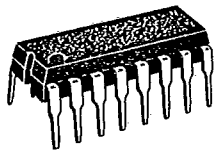

16-Pin • Plastic DIL Package

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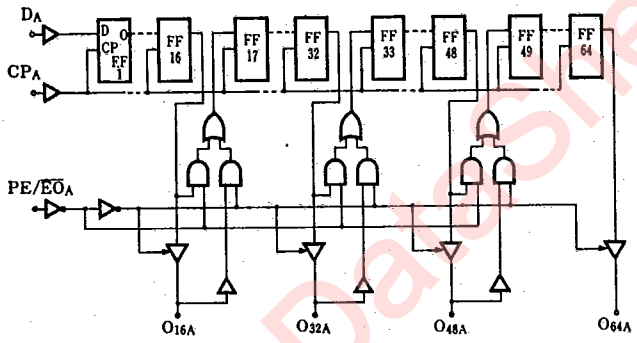
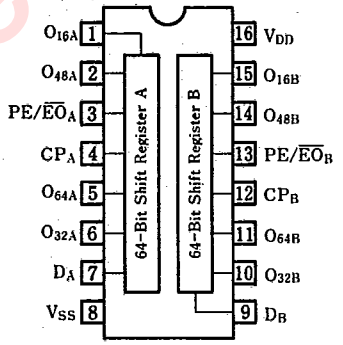
16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration



■ Truth Table

CP	PE/EO	D	O_{16}	O_{32}	O_{48}	O_{64}
0	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
0	1	×	High impedance	High impedance	High impedance	High impedance
1	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
1	1	×	High impedance	High impedance	High impedance	High impedance
↗	0	Enter into first bit	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit dispaly	Contents of 64-bit display
↗	1	Enter into first bit	Data entering into 17th bit	Data entering into 33rd bit	Data entering into 49th bit	High impedance
↘	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
↘	1	×	High impedance	High impedance	High impedance	High impedance

Note) X : don't care

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	50	—	50	—	375	μA
	10				—	100	—	100	—	700	
	15				—	200	—	200	—	1500	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}		—	1.6	—	1.6	—	12	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	220	660	ns
	10		—	85	255	
	15		—	60	180	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
High Level Output Disable Time PE/$\overline{EO}$→On (H)	5	t_{PHZ}	—	40	120	ns
	10		—	30	90	
	15		—	25	75	
Low Level Output Disable Time PE/$\overline{EO}$→On (L)	5	t_{PLZ}	—	50	150	ns
	10		—	30	90	
	15		—	25	75	
High Level Output Enable Time PE/$\overline{EO}$→On (H)	5	t_{PZH}	—	45	135	ns
	10		—	25	75	
	15		—	20	60	
Low Level Output Enable Time PE/$\overline{EO}$→On (L)	5	t_{PZL}	—	60	180	ns
	10		—	30	90	
	15		—	25	75	
Set-up Time On, D→CP	5	t_{su}	—	10	30	ns
	10		—	5	25	
	15		—	5	20	
Hold Time On, D→CP	5	t_{hold}	—	15	45	ns
	10		—	10	30	
	15		—	10	25	
Maximum Clock Frequency	5	fmax	2	5	—	MHz
	10		6	12	—	
	15		8	16	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms