MICRO NETWORKS

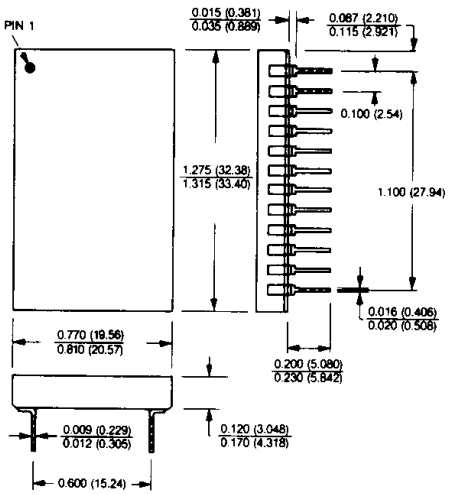
MN5160

HIGH-SPEED
8-Bit A/D CONVERTER
with LATCHED, 3-STATE OUTPUTS

FEATURES

- Fast 2.0μsec Conversion Time
- Latched, 3-State Output Buffer
- ±1/2LSB Linearity and No Missing Codes Over Temperature
- Adjustment-Free No Gain or Offset Adjustments Necessary
- Fully Specified 0°C to +70°C (MN5160) or −55°C to +125°C (MN5160H and MN5160H/B)
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5160 is a high-speed, 8-bit, successive approximation A/D converter with an onboard, latched, 3-state output buffer for easy data bus interfacing. Fast (2μsec maximum) conversion time, ± ½ LSB linearity, ±1 LSB absolute accuracy and "no missing codes" guaranteed over the entire operating temperature range make the MN5160 an excellent choice for industrial or military, high-speed, single or multi-channel data acquisition systems in monitoring or automatic test equipment. In very high-speed applications, the latched, 3-state output buffer provides a significant advantage over unlatched A/D's in that it allows valid parallel output data from the previous conversion to be held and read during an ongoing conversion.

MN5160 is packaged in a 24-pin, double-wide, hermetically sealed DIP and features 5 user-selectable input ranges. The stability of our Micro Networks laser-trimmed thin-film resistor networks allows MN5160 to operate without external gain and offset adjustments and maintain full accuracy and linearity over temperature.

Units are available and fully specified for 0°C to +70°C (MN5160) or −55°C to +125°C (MN5160H and MN5160H/B) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN5160H/B is available with Environmental Stress Screening, while MN5160H/B CH is screened in accordance with MIL-H-38534. Contact factory for availability of "CH" device types.

Part Number	Temperature Range for Guaranteed No Missing Codes	
MN5160	8 Bits	0°C to +70°C
MN5160H	8 Bits	−55°C to +125°C
MN5160H/B	8 Bits	−55°C to +125°C
MN5160H/B CH	8 Bits	−55°C to +125°C

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MN5160 HIGH-SPEED 8-Bit A/D CONVERTER with LATCHED 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5160	0°C to +70°C
MN5160H, MN5160H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 16)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 13)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 6)	−0.5 to +7 Volts
Analog Inputs (Pins 11, 12)	±20 Volts
Digital Inputs (Pins 7, 15, 23, 24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN5160 H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.
Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ± Vcc = ±15V, + Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 0 to +10 ±2.5, ±5, ±10		Volts Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V 0 to +10V, ±5V ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Start, Clock, Latch, $\overline{OE}$)				
Logic Levels All Inputs: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Start: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V) Clock, Latch, $\overline{OE}$: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+80 −1.6 +40 −1.6	μA mA μA mA
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Linearity Error (Note 4): Initial (+25°C) Over Temperature (Note 5)		±¼ ±¼	±½ ±½	LSB LSB
Temperature Range for Guaranteed No Missing Codes (Note 5): MN5160 MN5160H, MN5160H/B	 0 −55		 +70 +125	 °C °C
Full Scale Absolute Accuracy Error (Notes 4, 6): Initial (+25°C) Over Temperature (Note 5)		 ±½ ±1	 ±1 ±2	 LSB LSB
Unipolar Offset Error (Notes 4, 7): Initial (+25°C) Over Temperature (Note 5)		 ±¼ ±½	 ±½ ±1	 LSB LSB
Bipolar Zero Error (Notes 4, 8): Initial (+25°C) Over Temperature (Note 5)		 ±¼ ±½	 ±½ ±1	 LSB LSB
DIGITAL OUTPUTS (Parallel, Serial, Status)				
Output Coding (Note 9): Unipolar Ranges Bipolar Ranges		SB OB		
Logic Levels All Outputs: Logic "1" (Isource ≤ 400μA) Logic "0" (Isink ≤ 8 mA) Leakage (Parallel Outputs) in High - Z State (Note 2)	+2.4	 ±20	 +0.4	Volts Volts μA
REFERENCE OUTPUT				
Internal Reference (Note 2): Voltage Accuracy Tempco External Current		+6.3 ±10 ±10	 200	Volts % ppm/°C μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 10)			2.0	μsec
External Clock Frequency			4	MHz
Clock Pulse Width (Note 2): High Low	20 50			nsec nsec
Setup Time Start Low to Clock (Note 2)	20			nsec
Latch Enable Pulse Width (Note 2)	50			nsec
Delay From Output Enable to Data Valid (Note 2)			50	nsec

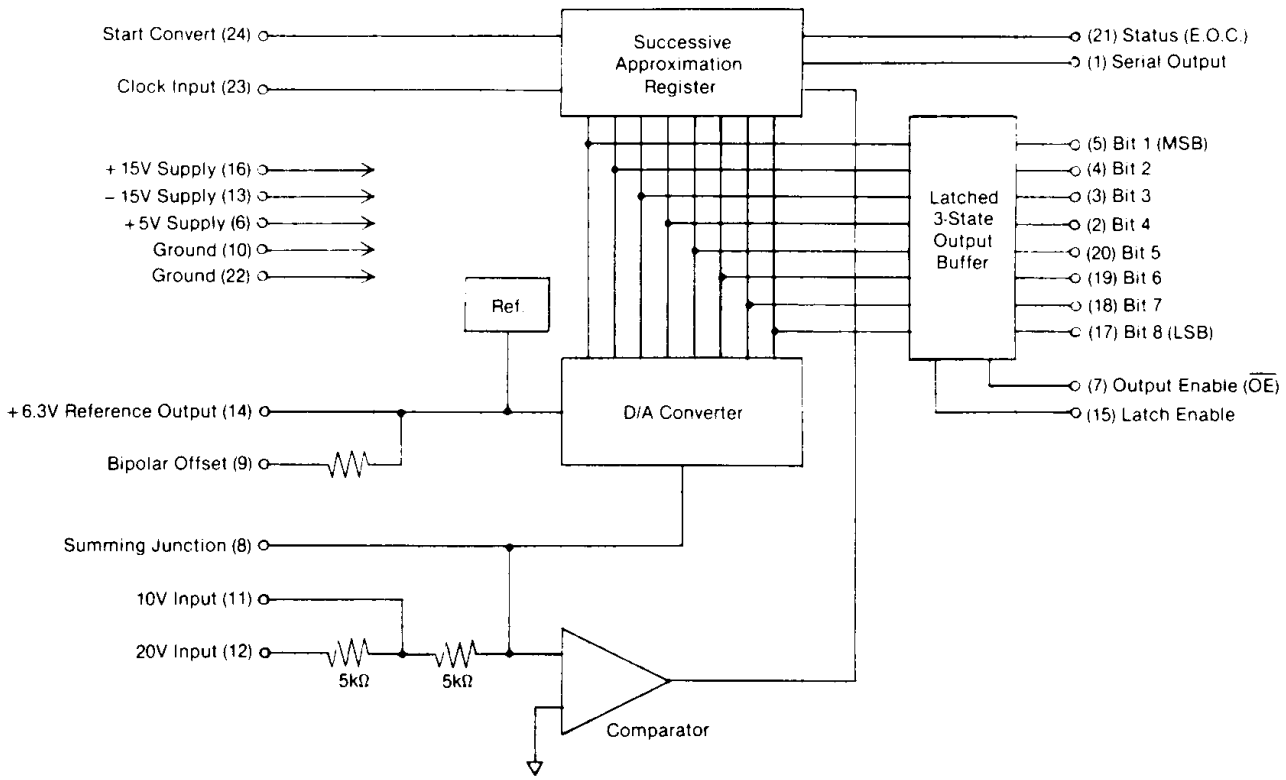
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Notes 3, 11): +15V Supply		± 0.03	± 0.06	%FSR/%Supply
−15V Supply		± 0.01	± 0.02	%FSR/%Supply
Current Drain: +15V Supply		+16	+22	mA
−15V Supply		−10	−18	mA
+5V Supply		+100	+140	mA
Power Consumption		890	1300	mW

SPECIFICATION NOTES:

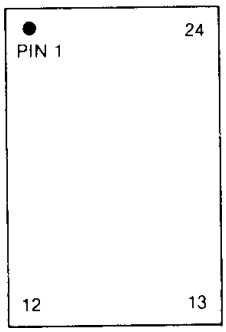
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ± 10V operation has a 20V FSR. A unit connected for 0 to + 10V, ± 5V operation has a 10V FSR. A unit connected for 0 to + 5V, ± 2.5V operation has a 5V FSR.
4. 1 LSB for 8 bits in 20V FSR is 78mV.
   1 LSB for 8 bits in 10V FSR is 39mV.
   1 LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0 °C to + 70 °C temperature range for standard products, and over the − 55 °C to + 125 °C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input range. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 for unipolar and bipolar input ranges. Additionally it describes the accuracy of the 0000 0000 to 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½ LSB below the nominal positive full scale voltage. The latter ideally occurs + ½ LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 when operating MN5160 on a unipolar range. The ideal value at which this transition should occur is + ½ LSB. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5160 on a bipolar range. The ideal value at which this transition should occur is − ½ LSB. See Digital Output Coding.
9. SB = straight binary. OB = offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Serial Output	24	Start Convert
2	Bit 4	23	Clock Input
3	Bit 3	22	Ground
4	Bit 2	21	Status (E.O.C.)
5	Bit 1 (MSB)	20	Bit 5
6	+5V Supply (+Vdd)	19	Bit 6
7	Output Enable ($\overline{OE}$)	18	Bit 7
8	Summing Junction	17	Bit 8 (LSB)
9	Bipolar Offset	16	+15V Supply (+Vcc)
10	Ground	15	Latch Enable
11	10V Input	14	Reference Output (+6.3V)
12	20V Input	13	−15V Supply (−Vcc)

APPLICATIONS INFORMATION

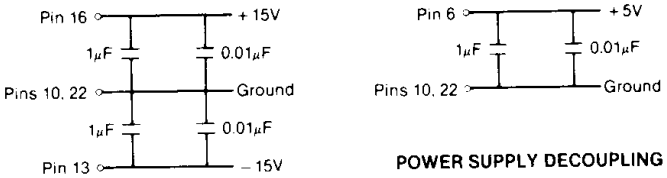
DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

As you recall, digital output bits are reset to 0111 1111 at the beginning of the successive approximation conversion process and that valid parallel output data can only be read between conversions. MN5160's Latch Enable (pin 15) and Output Enable (pin 7) allow data from a prior conversion to be latched and read while the next conversion is in progress. If desired, valid output data may be latched by applying a "0" to "1" edge to Latch Enable (pin 15). If this is done, output data from the just completed conversion will be latched in MN5160's 3-state output latch. Once latched, output data may be read by bringing Output Enable ($\overline{OE}$, pin 7) low. Output data will be valid 50nsec maximum after Output Enable is low. Output data bits are returned to the high-impedance state by bringing Output Enable high.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5160. The unit's two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

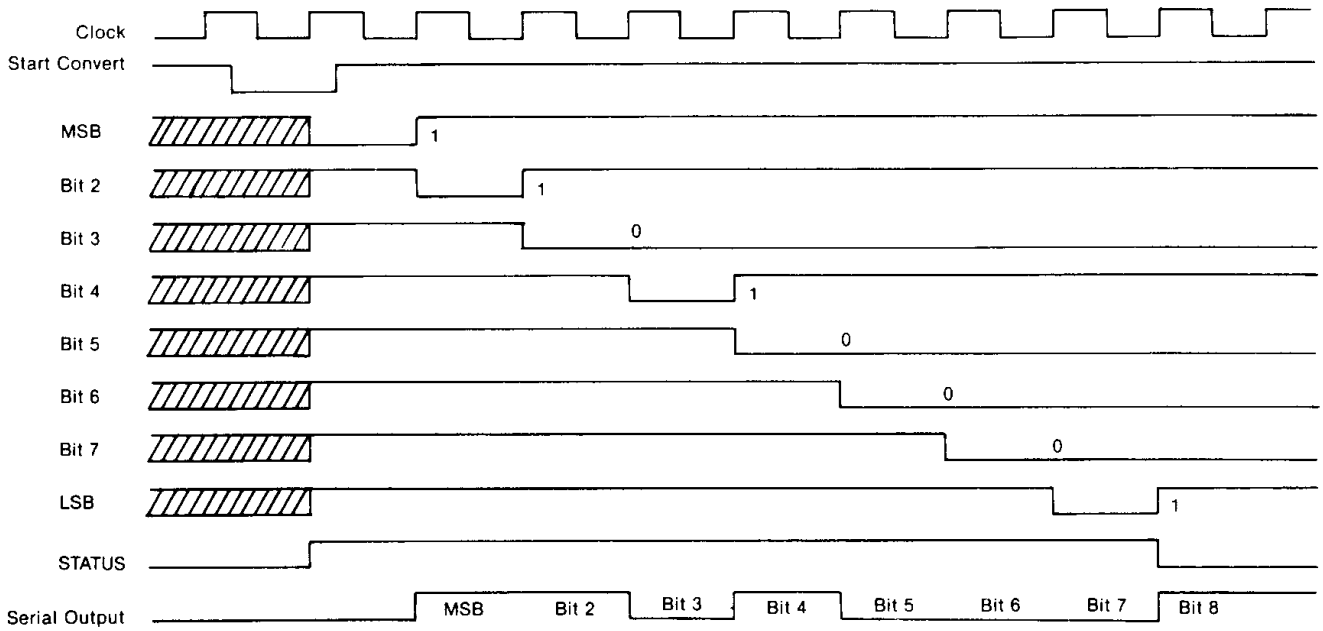


POWER SUPPLY DECOUPLING

CONTINUOUS CONVERTING—The MN5160 A/D converters can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

STATUS OUTPUT—The Status or End Of Conversion (E.O.C., pin 21) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 100nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the Status can be made the input of a D flip flop whose clock input is the same as the converter clock. In this situation, the Q output will change one clock period after Status changes.

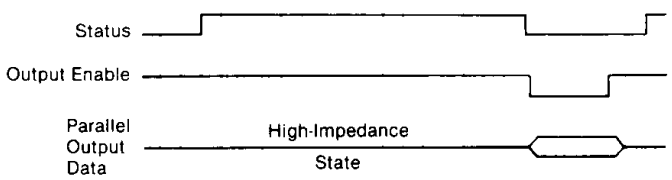
TIMING DIAGRAM



TIMING DIAGRAM NOTES:

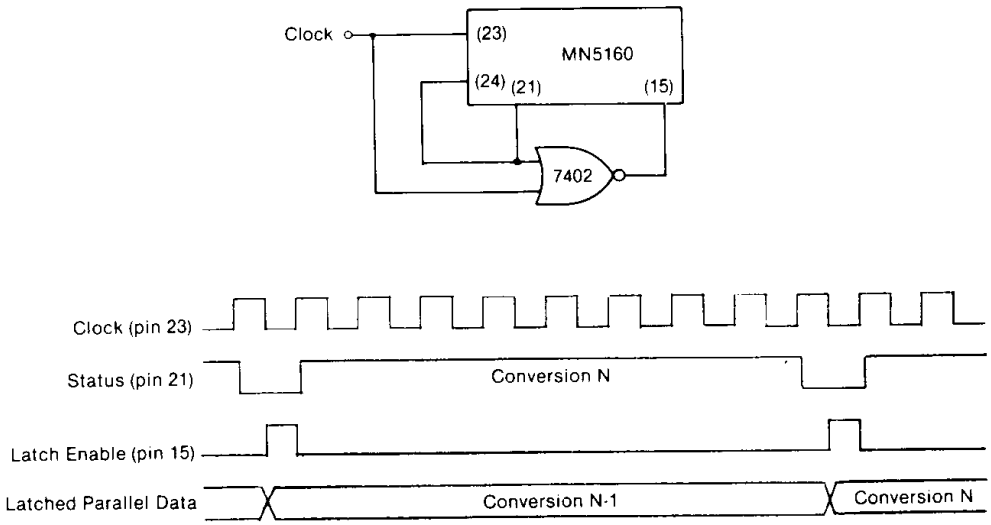
1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 100nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. Parallel output data can be latched at the end of a conversion by a "0" to "1" edge applied to Latch Enable (pin 15).
9. Parallel output data can be enabled by bringing Output Enable ($\overline{OE}$, pin 7) low. Parallel output bits can be returned to the high impedance state by setting Output Enable high.
10. For continuous conversion, connect the Status output (pin 21) to the Start Convert input (pin 24). See section on Continuous Conversion.
11. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

OUTPUT ENABLE—Output Enable ($\overline{OE}$, pin 7) controls the state of the parallel outputs. When a conversion is complete, valid parallel output data may be enabled by bringing Output Enable low. Data will be available 50nsec maximum after Output Enable is low. Output data is returned to the high-impedance state by bringing Output Enable high. See diagram below.



LATCH ENABLE—Valid parallel output data can be latched in MN5160's output buffer by the rising edge ("0" to "1" transition) of Latch Enable input (pin 15). When continuously converting, data from the previous conversion can be latched and read during a subsequent conversion. The Status (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion. Once latched, output data can be enabled and read by bringing Output Enable ($\overline{OE}$, pin 7) low.

LATCHING DATA CONTINUOUS CONVERSIONS



INPUT RANGE SELECTION

Connect	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Input to Pin	11	11	11	11	12
Pin 8 to Pin	12	Open	12,9	9	9
Pin 9 to Pin	Ground	Ground	8	8	8
Input Impedance	2.5kΩ	5kΩ	2.5kΩ	5kΩ	10kΩ

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Output	
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB	LSB
+5.000	+10.000	+2.500	+5.000	+10.000	1111	1111
+4.981	+9.961	+2.481	+4.961	+9.922	1111	111Ø*
+2.519	+5.039	+0.019	+0.039	+0.078	1000	000Ø*
+2.500	+5.000	0.000	0.000	0.000	ØØØØ	ØØØØ*
+2.481	+4.961	−0.019	−0.039	−0.078	0111	111Ø*
+0.019	+0.039	−2.481	−4.961	−9.922	0000	000Ø*
0.000	0.000	−2.500	−5.000	−10.000	0000	0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V or ±2.5V input ranges, 1LSB for 8 bits = 19.5mV.
4. For 0 to +10V or ±5V input ranges, 1LSB for 8 bits = 39mV.
5. For ±10V input range, 1LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5160 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.961 volts. Subsequently, any input voltage more negative than −9.961 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of −0.039 volts, and the 1111 1111 to 1111 1110 transition should occur at +9.883 volts. An input more positive than +9.883 volts will give all "1's."