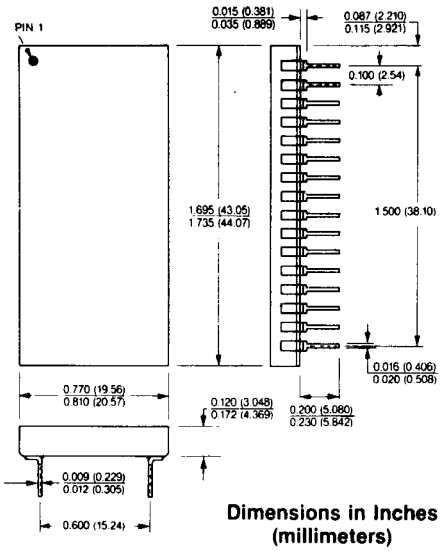
FEATURES

- 16-Bit Resolution
- 17μsec Max Conversion Time
- 14-Bit Performance Guaranteed Over Temperature (MN5295)
- ±0.003% FSR Maximum Linearity Error (MN5295)
- Serial and Parallel Outputs
- 6 User-Selectable Input Ranges
- 1.2 Watts Maximum Power Consumption
- Standard 32-Pin Double DIP
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

High resolution, high speed, small package and the ability to operate over extended temperatures (including −55°C to +125°C) are brought together in the MN5295 and MN5296. These TTL-compatible, 16-bit, DIP-packaged A/D converters guarantee 17μsec maximum conversion time (for 16 bits); 1.2 Watts maximum power consumption; and ±0.003% FSR maximum integral linearity error. Over temperature, MN5295 guarantees 14-bit "no missing codes", and MN5296 guarantees the same for 13-bits. Each device is packaged in a standard, 32-pin, double-wide, hermetic, ceramic DIP—not the triple-wide DIP's of most other 16-bit A/D's.

MN5295 and MN5296 are complete with internal clock and reference, and each has 6 user-selectable input voltage ranges. Output data is straight binary coded for unipolar input ranges and offset binary coded for bipolar input ranges and is available in both serial and parallel formats.

MN5295 and MN5296 16-bit A/D converters were specifically designed for use in military/aerospace and harsh-environment industrial applications that demand fully guaranteed, high-speed, high-resolution performance over extended operating temperature ranges. They are ideal for applications requiring true 14 (MN5295) or 13-bit (MN5296) performance over temperature. Applications will be found in military instrumentation, ATE, servo control systems and industrial robotic position sensing systems. MN5295 and MN5296H/B are available with Environmental Stress Screening while MN5295 H/B CH and MN5296 H/B CH are screened in accordance with MIL-PRF-38534.

Model Number	Temperature Range for Guaranteed No Missing Codes	
MN5295	14 Bits	0°C to +70°C
MN5295H	14 Bits	−55°C to +125°C
MN5295H/B	14 Bits	−55°C to +125°C
MN5295H/B CH	14 Bits	−55°C to +125°C
MN5296	13 Bits	0°C to +70°C
MN5296H	13 Bits	−55°C to +125°C
MN5296H/B	13 Bits	−55°C to +125°C
MN5296H/B CH	13 Bits	−55°C to +125°C

MN5295 MN5296 HIGH-SPEED 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5295, MN5296	0°C to +70°C
MN5295H, H/B, MN5296H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 27)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 23)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pin 29)	0 to +7 Volts
Analog Inputs (Pins 8 and 9)	±22 Volts
Digital Inputs (Pins 30 and 32)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5295 H/B CH

- Select MN5295 or MN5296.
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 10, 20 ±2.5, 5, 10		Volts Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V 0 to +10V, ±5V 0 to +20V, ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+40 −1.6	μA mA
TRANSFER CHARACTERISTICS (Note 3)				
Resolution		16		Bits
Integral Linearity Error (Note 4): Initial (+25°C): MN5295 MN5296 Over Temperature (Note 5): MN5295 MN5296		±0.0015 ±0.003 ±0.003 ±0.006	±0.003 ±0.006 ±0.006 ±0.012	%FSR %FSR %FSR %FSR
Differential Linearity Error (Note 4): MN5295 MN5296		±0.003 ±0.006	±0.006 ±0.012	%FSR %FSR
Temperature Range for Guaranteed No Missing Codes MN5295 (14 bits), MN5296 (13 bits) MN5295H (14 bits), MN5296H (13 bits)	 0 −55		 +70 +125	 °C °C
Full Scale Absolute Accuracy Error (Note 6): Unipolar: Initial (+25°C) Over Temperature (Note 5) Bipolar: Initial (+25°C) Over Temperature (Note 5)		 ±0.075 ±0.15 ±0.1 ±0.2	 ±0.15 ±0.3 ±0.2 ±0.4	 %FSR %FSR %FSR %FSR
Unipolar Offset Error (Notes 7, 8): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 7, 9): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.12 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Gain Error (Notes 7, 10): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±20	% % ppm/°C
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 11): Unipolar Ranges Bipolar Ranges		SB OB		
Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$) Logic "0" ($I_{sink} \leq 3.2mA$)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference: Voltage Accuracy Tempco (Note 2) External Current (Notes 2, 12)		+10.000 ±0.025 ±5	 ±0.1 1	Volts % ppm/°C mA
DYNAMIC CHARACTERISTICS				
Conversion Time (14 Bits/16 Bits) (Note 13)		14/16	15/17	μsec

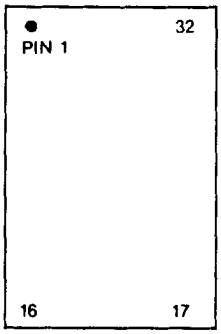
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: ±15V Supplies +5V Logic Supply	±14.55 +4.75	±15 +5	±15.45 +5.25	Volts Volts
Power Supply Rejection (Note 14): +15V Supply −15V Supply +5V Logic Supply		±0.005 ±0.005 ±0.001	±0.02 ±0.02 ±0.01	%FSR/% Supply %FSR/%Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Logic Supply		+35 −24 +12	+42 −32 +18	mA mA mA
Power Consumption		945	1200	mW

SPECIFICATION NOTES:

1. Listed specifications apply for all part numbers unless specifically indicated. Detailed timing specifications appear in the Timing sections of this data sheet.
2. These parameters are listed for reference only and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for 0 to +20V or ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153%FSR. 1 LSB for 14 bits is equivalent to 0.0061%FSR.
4. ±0.003%FSR is equivalent to ±½ LSB for 14 bits. ±0.006%FSR is equivalent to ±½ LSB for 13 bits.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½ LSB's below the nominal positive full scale voltage. The latter ideally occurs ½ LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Initial unipolar offset (bipolar zero) and gain errors are adjustable to zero with the use of external potentiometers.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just chages from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN5295/5296 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN5295/5296 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
10. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 1111 to 1111 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
11. SB = straight binary. OB = offset binary. See table of transition voltages in section labeled Digital Output Coding.
12. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
13. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of the status (end of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14-bit conversions. See Timing Diagram.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

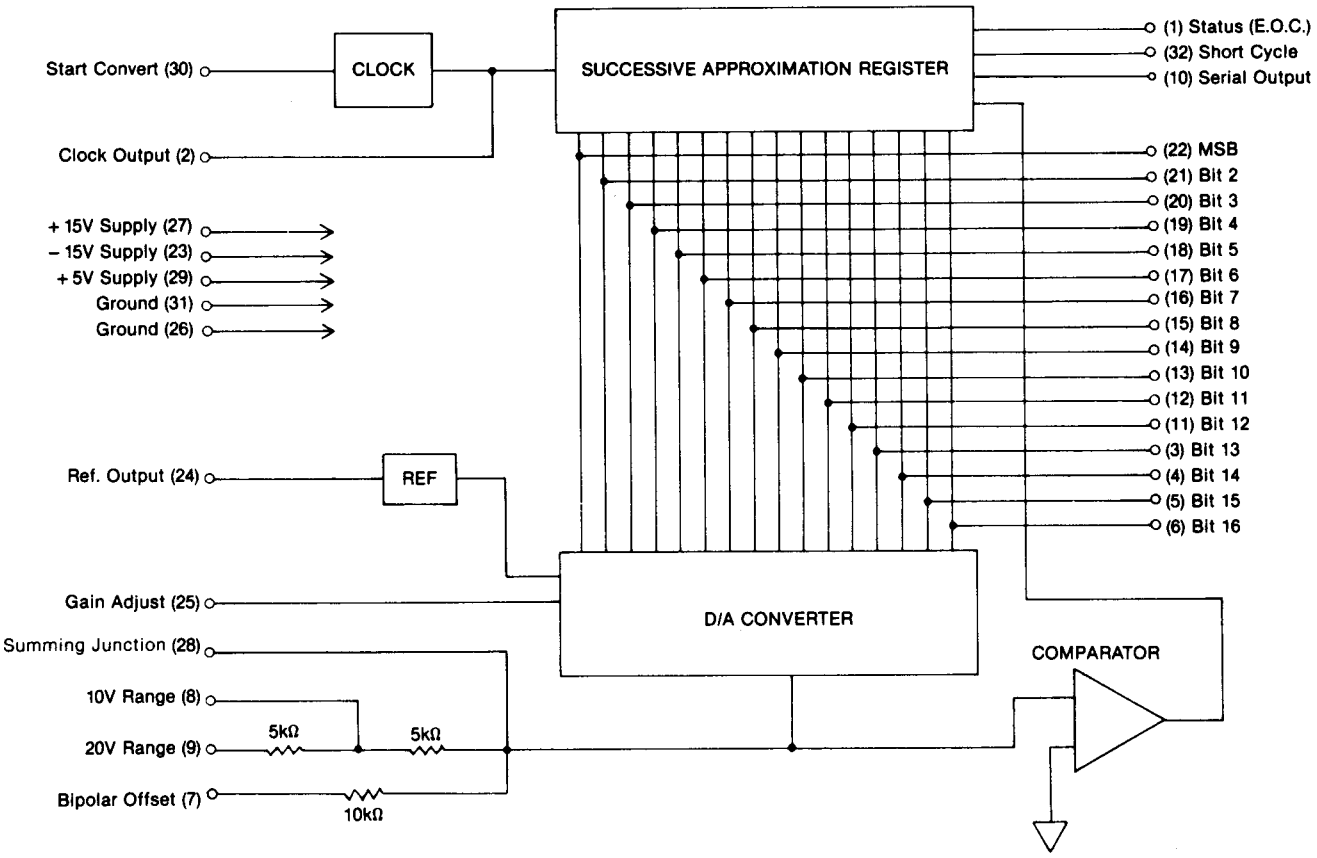
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Status (E.O.C.)	32	Short Cycle
2	Clock Output	31	Ground
3	Bit 13	30	Start Convert
4	Bit 14	29	+5V Supply (+V_{dd})
5	Bit 15	28	Summing Junction
6	Bit 16 (LSB)	27	+15V Supply (+V_{cc})
7	Bipolar Offset	26	Ground
8	10V Input Range	25	Gain Adjust
9	20V Input Range	24	Reference Output (+10V)
10	Serial Output	23	−15V Supply (−V_{cc})
11	Bit 12	22	Bit 1 (MSB)
12	Bit 11	21	Bit 2
13	Bit 10	20	Bit 3
14	Bit 9	19	Bit 4
15	Bit 8	18	Bit 5
16	Bit 7	17	Bit 6

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—See Block Diagram. The successive approximation register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 30 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0"; the outputs of the other bit flip flops are set to a logic "1"; and the Status (pin 1) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after Start Convert has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

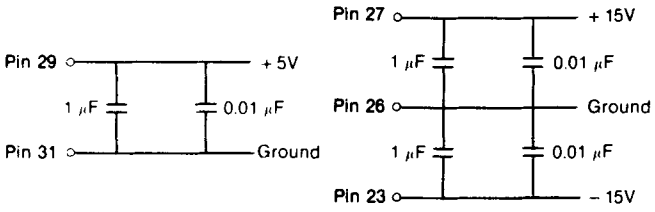
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5295 and MN5296. The units' two ground pins (pins 26 and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 26 and 31 as close to the unit as possible and wide conductor runs employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 7 (Bipolar Offset), 8 and 9 (Analog Inputs), 28 (Summing Junction) and 25 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when using these inputs. Input signal lines should be as short as possible. In bipolar operation, where pin 7 is connected to pin 24, a short jumper should be used. If bipolar offsetting is not used, pin 7 should be grounded to pin 26. For external offset adjustment, the 1.8 megohm resistor should be located as close to pin 28 as possible. A 0.01μF ceramic capacitor should be connected between pin 25 and analog ground as close to the package as possible.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN5295 and MN5296. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

If short cycling is not used, the Short Cycle pin (pin 32) must be connected to +5V (pin 29).

POWER SUPPLY DECOUPLING



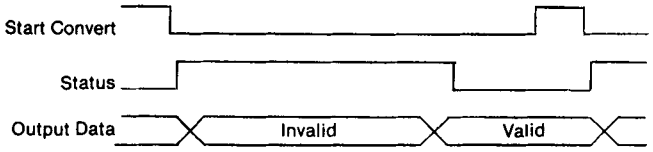
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

SHORT CYCLING—For applications requiring fewer than 16 bits of resolution, the MN5295 and MN5296 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 32). For example, to truncate at 14 bits, connect pin 5 (Bit 15) to pin 32; converting will stop and Status will go low after bit 14 has been set. For any length conversion, the falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs.

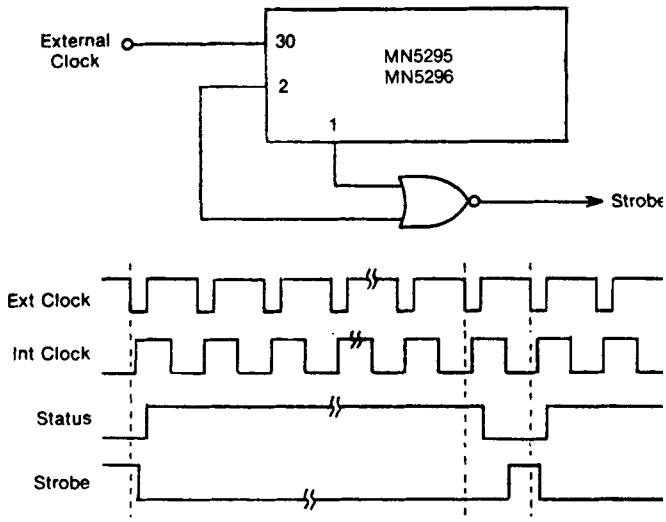
EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever Start Convert is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after Status has gone low signaling the end of the previous conversion. When continuously converting in this manner, Status will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT—Serial data is available only during the conversion process. Format is NRZ with the MSB occurring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the Timing Diagram. Each data bit becomes valid typically 120nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. The falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs. If parallel data is to be latched into external registers, this delay should be long enough to accomodate the set-up time requirements of the latch such that Status can be used to strobe the latch. If the delay is not long enough, the Status can be delayed with gate delays or the latch can be strobed with the leading edge of the next start convert pulse. See diagram below.

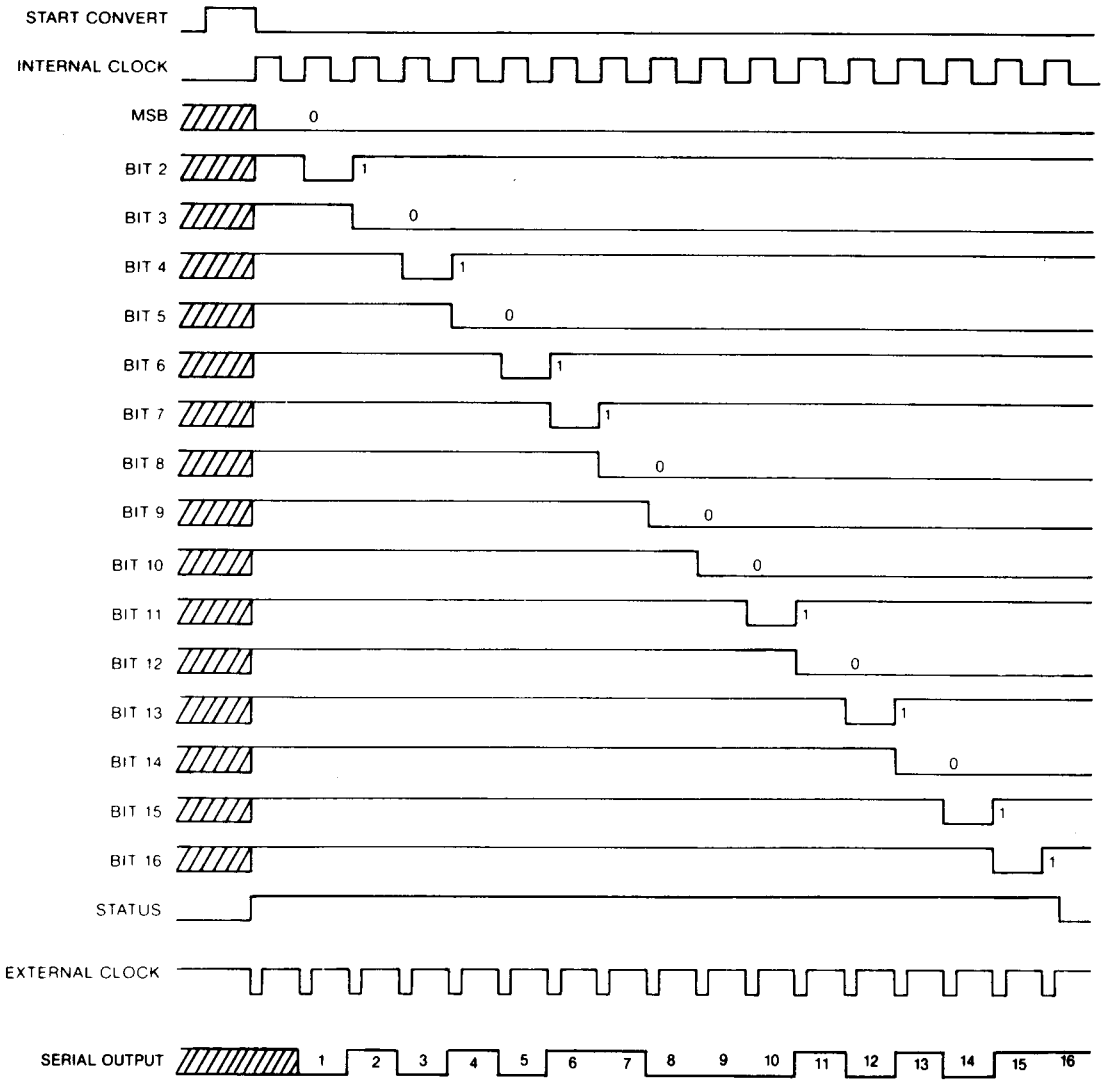


If continuously converting with an external clock, Status can be NORed with the internal clock, as shown below, to produce a positive strobe pulse approximately ½ period wide, approximately ½ period after Status has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 120nsec. See Timing Diagram and the section labeled External Clock.



INTERNAL REFERENCE—The MN5295 and MN5296 contain an internal, low-drift 10V reference that is laser trimmed to an initial accuracy of ±0.1%. The reference is pinned out on pin 24 and can supply up to 1mA beyond the current required for bipolar operation (pin 24 connected to pin 7). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

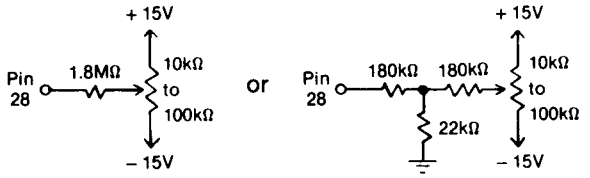
DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (14 Bits/16 Bits)		14/16	15/17	μsec
Internal Clock Frequency (Note 8)		1		MHz
Start Convert Positive Pulse Width (Note 8)	50			nsec
Delay Falling Edge of Start to (Note 8): Status = "1" Clock Output = "1"		50 20	80 50	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20	120	200	nsec
Delay LSB Valid to Falling Edge of Status (Note 8)	20	60		nsec

TIMING DIAGRAM NOTES

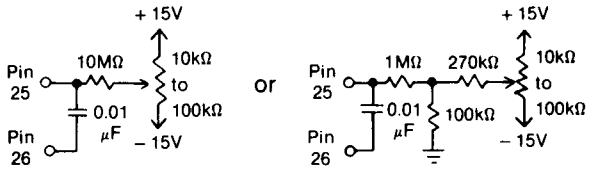
1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Data will be valid 60nsec before the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock.
6. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
7. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14 bit conversions.
8. These parameters are listed for reference only and are not tested.

OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS — Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 28 should be connected as described in the Range Selection section.

ZERO ADJUSTMENT—Connect the zero adjust potentiometer as shown. For unipolar ranges, apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off. For bipolar ranges, apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits "flicker" on and off.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+ F.S.	+ F.S.	1111 1111 1111 1111
+ F.S. – ³/₂ LSB	+ F.S. – ³/₂ LSB	1111 1111 1111 111Ø*
+ ½F.S. + ½ LSB	+ ½ LSB	1000 0000 0000 000Ø*
+ ½F.S. – ½ LSB	– ½ LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+ ½F.S. – ³/₂ LSB	– ³/₂ LSB	0111 1111 1111 111Ø*
+ ½ LSB	– F.S. + ½ LSB	0000 0000 0000 000Ø*
0	– F.S.	0000 0000 0000 0000

CODING NOTES:

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5295/MN5296 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE					
	0 to + 5V	0 to + 10V	0 to + 20V	± 2.5V	±5V	± 10V
Connect Pin 7 to Pin	26	26	26	24	24	24
Connect Pin 9 to Pin	28	Open	Input	28	Open	Input
Connect Pin 28 to Pin	9	Open	Open	9	Open	Open
Connect Input to Pin	8	8	9	8	8	9
Input Impedance (KΩ)	2.5	5	10	2.5	5	10

EXAMPLE: For the ± 10V range, the transition from output code 1111 1111 1111 1111 to output code 1111 1111 1111 1110 (or vice versa) will ideally occur at an input of + 9.999542V (+ F.S. – ³/₂LSB). Subsequently, any voltage greater than + 9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of – 0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at – 9.999847V. An input more negative than this level will give all "0's."

USING TRACK-HOLD AMPLIFIERS WITH MN5295 AND MN5296 A/D CONVERTERS

High-speed, high-resolution, successive approximation type A/D converters, such as MN5295/5296, are severely limited in their ability to accurately convert dynamic input signals. Stated differently, these high-resolution, high-throughput digitizers have limited analog input bandwidth capabilities. In high-speed data-acquisition or digital-signal-processing (DSP) applications in which high resolution, high throughput and high input bandwidth are required, a track-hold (T/H) amplifier must be used to overcome the A/D's inherent bandwidth limitations. The T/H has the ability to follow (track) the high-speed input signal until it is time to convert it. When commanded into the hold mode, the T/H instantaneously "freezes" the input signal and holds it constant while the A/D performs its conversion.

The MN374 High-Speed, High-Resolution T/H Amplifier has been designed specifically as a companion T/H for MN5295/5296 A/D's. A typical application is described below. Please see the MN5290/5291 data sheet for a general discussion of important factors to consider when selecting a T/H for use with higher resolution A/D's.

For slower speed A/D converters, the most popular technique used to control the T/H's operation is to drive the T/H directly with the A/D's status line. For virtually all high-resolution A/D's in use today, including MN5295/5296, this technique does *not* work because the T/H's track-to-hold transients will not reliably settle fast enough. The application described below is a much more cautious way to control the T/H-A/D timing because it uses a timed one-shot to delay the start of the A/D conversion. The circuit allocates a predetermined amount of time for the track-to-hold transient to fully settle before initiating the A/D conversion. After the conversion has been completed, the circuit immediately drives the T/H back into the track mode.

The principles discussed below are general and can be used for virtually any T/H-A/D combination. The system is run by an externally applied clock whose frequency determines the overall sampling/digitizing rate. Please refer to the timing and schematic diagrams below as well as the MN374 T/H data sheet.

The system consists of the A/D, the T/H, a single one-shot and a dual flip-flop. The falling edge of the system clock triggers the 74LS123 one-shot, and the system clock can have any duty cycle as long as it has a minimum positive pulse width of

50nsec to accommodate the setup-time requirement of the one-shot.

The one-shot produces a 500nsec pulse, and both the Q and $\overline{Q}$ outputs are utilized. The Q output becomes the start pulse for the MN5295/5296, and the $\overline{Q}$ output drives the set pin of the first half of the 74LS74 flip-flop. The $\overline{Q1}$ output of the flip-flop controls the operational mode of the MN374 T/H. The falling edge of the $\overline{Q}$ output of the 74LS123 asynchronously sets the flip-flop driving its Q1 output high and its $\overline{Q1}$ output low. The MN374, which has an active-low control line, is immediately driven into its hold mode by the falling edge of $\overline{Q1}$.

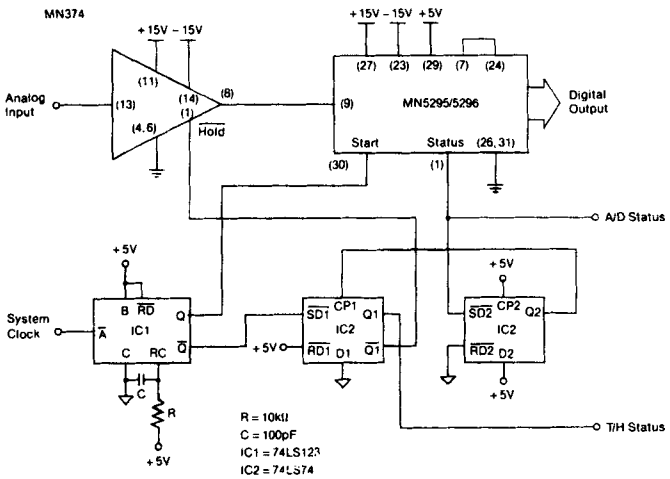
The pulse width of the 74LS123 has been selected so that there is now ample time for the MN374 track-to-hold transient to fully decay before the A/D conversion begins. After 500nsec, the Q output of the one-shot drops to "0" initiating the A/D conversion, and driving the Status output (pin 1) of the A/D to a "1". The T/H remains in hold because the rising edge of the $\overline{Q}$ output of the one-shot does not affect the first flip-flop. The rising edge of Status asynchronously resets the second flip-flop driving the Q2 output low.

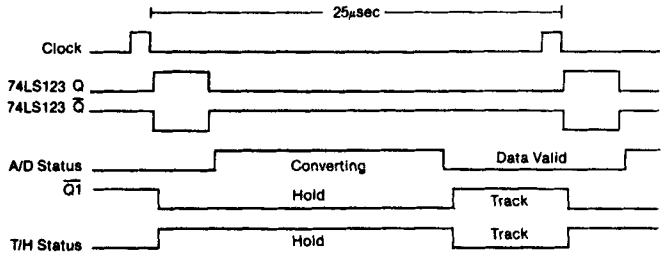
The T/H remains in the hold mode for the next 17μsec as the A/D completes its conversion. At the end of the conversion, the A/D's Status line drops to a "0", and this sets the second flip-flop. The Q2 output goes high clocking the first flip-flop which has a "0" on its D line. This forces the Q1 output low and the $\overline{Q1}$ output high driving the T/H back into the signal-acquisition (track) mode.

The status of this system can be monitored at a number of different points. Whenever pin 1 (Status) of MN5295/5296 is a logic "1", the A/D is performing a conversion, and output data is not valid. The falling edge of this line signals that the conversion is complete and that output data is now valid. The Q1 output of the first flip-flop can be used to monitor the T/H. Whenever this line is a "1", the T/H is in the hold mode. When it is a "0", the T/H is in the track mode. The falling edge here also indicates that a conversion has just been completed and that output data is now valid. If an external latch is to be used to clock data away from MN5295/5296, either of the falling edges described above may be used to strobe the latch.

Remember that the above application does not automatically take care of the T/H acquisition time and that this time must be allowed for in determining the external clock period. If the MN5295/5296 requires 17μsec to make a conversion, and the T/H requires 4μsec for acquisition time, adding 2μsec of overhead time yields a period of 23μsec. That means the system can be clocked at 43kHz and still be guaranteed to meet full accuracy and linearity performance.

It is unnecessary to have the 74LS123 one-shot in the application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 43kHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5295/5296 directly, and it can be inverted to drive the 74LS74.





ORDERING INFORMATION

Part Number	Specified Temperature Range	Conversion Time (μsec, Max.)	Integral Linearity (%FSR, Max.)		No Missing Codes Over Temperature	Power Consumption (mW, Max.)	Package
			+25°C	Temp.			
MN5295	0°C to +70°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5295H	−55°C to +125°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5295H/B	−55°C to +125°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5296	0°C to +70°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP
MN5296H	−55°C to +125°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP
MN5296H/B	−55°C to +125°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP

Contact factory for availability of CH device types.