MICRO NETWORKS

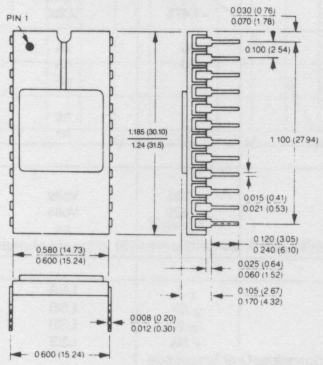
MN5901

8-Bit, 100MHz
FLASH A/D CONVERTER

FEATURES

- **8-Bit Resolution**
- **100MHz Min. Conversion Rate**
- **80MHz Large Signal Bandwidth**
- **5.0 Effective Bits, f_{ain} =35MHz (Guaranteed Over Temp Range)**
- **Balanced Input Range**
- **End Point Error 1LSB Max (Guaranteed Over Temp Range)**
- **.85LSB Max Linearity (Guaranteed Over Temp Range)**
- **100K ECL Compatible Output Data**
- **Operating Temp Range -55°C to +125°C case, (Optional)**

24 PIN SIDE-BRAZED DIP



Dimensions In Inches
(millimeters)

DESCRIPTION

The MN5901 is an ultra-high speed monolithic Analog to Digital converter which has 8-bit resolution and a guaranteed conversion speed (strobe frequency) of 100MHz. The MN5901 utilizes the "flash" or parallel principle, whereby a field of 255 comparators simultaneously determine the precise analog input. The comparators' outputs are converted to ECL compatible outputs through three encoding stages which are activated by two strobe signals. The MN5901's input is easily driven by a 50-ohm source without the burden of a pre-amplifier or level shifter. Reference sense pins $+V_{REF,S}$ and $-V_{REF,S}$ allow compensation for voltage drops at the top and bottom of the reference resistance string which contribute to the MN5901's precise end point accuracy (1LSB max over the full operating temperature range).

Packaged in a small 24-pin hermetically sealed ceramic DIP, the MN5901 offers outstanding differential linearity (.95LSB max over the specified temperature range) and a high signal-to-noise-ratio (SNR) of 38dB min at 35MHz as well as a precise endpoint accuracy of 1LSB max over the full temperature range. Micro Networks provides important dynamic testing of dynamic linearity (effective bits), signal-to-noise-ratio, and total harmonic distortion over the full operating temperature range at a conversion rate of 100MHz for 100% of all military temperature range devices. The MN5901 is specified for operation from −4.5V supplies for output compatibility with 100K ECL logic and is also compatible with 10K ECL logic when operated from −5.2V.

Devices are offered for operation over −25°C to +85°C (case), and −55°C to +125°C (case, H models). Contact factory for availability of fully compliant MIL-STD-883, Method 5008 devices.

APPLICATIONS

Radar Systems
Digital Oscilloscopes
Automatic Test Equipment
ECM Equipment
Analytical Systems

MN5901 8-Bit 100MHz A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (case)	−55°C to +125°C
Specified Temperature Range (case):	
MN5901	−25°C to +85°C
MN5901H, MN5901H-883	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply Voltages ($+V_{CC}$, $+V_{CC,D}$)	−0.3 to +6.0 Volts
Negative Supply Voltages ($-V_{EE}$, $V_{EE,D}$)	+0.3 to −6.0 Volts
Reference Voltages ($+V_{REF}$, $-V_{REF}$)	−2.5 to +1.5 Volts
Analog Input Voltage (V_{AIN})	−2.5 to +1.5 Volts
Digital Input Voltages	−3.5 to +0.0 Volts
Output Current (I_{D0} - I_{D7})	20mA

ORDERING INFORMATION

PART NUMBER — **MN5901H-883**

Add suffix "H" for −55°C to +125°C operation.

Add "-883" suffix to "H" models for MIL-STD-883 compliant devices.

Thermal Information

Thermal resistance:

Junction-to-case (bottom of package)	2.6°C/W
Junction-to-ambient, free air dissipation	44°C/W

SPECIFICATIONS (T_A = +25°C, V_{CC}, $V_{CC,D}$ = +5.0V; V_{EE}, $V_{EE,D}$ = −4.5V; $+V_{REF}$ = +1.00V; $-V_{REF}$ = −1.00V unless otherwise noted)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	−2	±1	+1	Volts
Analog Input Current ($V_{AIN} \geq +V_{REF}$)	150		700	μA
(Note 1) ($V_{AIN} \leq -V_{REF}$)			10	μA
Input Impedance		6		KOhms
Input Capacitance ($V_{AIN} \geq +V_{REF}$)		50		pF
($V_{AIN} \leq -V_{REF}$)		60		pF
Full Power Bandwidth (Note 2)		80		MHz
REFERENCE INPUTS				
Reference Voltages (Note 3) ($+V_{REF}$, $-V_{REF}$)	−2.0		+1.0	Volts
Reference Ladder Resistance	105	150	190	Ohms
Ladder Temperature Coefficient		0.45		Ohms/°C
DIGITAL INPUTS				
Logic Levels: Over Temperature (Note 4)				
Logic "1"	−1.165			Volts
Logic "0"			−1.475	Volts
Logic Currents: Over Temperature (Note 4)				
Logic "1" ($V_{STR} = V_{IH}$)			30	μA
Logic "0" ($V_{STR} = V_{IL}$)			40	nA
Input Capacitance		5		pF
Pulse Width Low:				
STR 1	4			ns
STR 2	3			ns
DIGITAL OUTPUTS				
Logic Levels: Over Temperature (Notes 4 & 5)				
Logic "1"	−1.025		−.880	Volts
Logic "0"	−1.810		−1.620	Volts
Output Rise Time (Note 6)			3	ns
Output Fall Time (Note 6)			3	ns
TRANSFER CHARACTERISTICS				
Integral Nonlinearity Error			±.5	LSB
Over Temperature (Note 4)			±.85	LSB
Differential Linearity Error			±.6	LSB
Over Temperature (Note 4)			±.95	LSB
No Missing Codes		Guaranteed Over Temperature		
End Point Error (Note 7)			±.90	LSB
Over Temperature (Notes 4 & 7)			±1.0	LSB

	MIN.	TYP.	MAX.	UNITS
DYNAMIC PERFORMANCE				
Conversion Rate Over Temperature	100	125		MHz
Aperture Delay		1		ns
Aperture Jitter		25		ps
Conversion Time (Notes 6 & 8)			20	ns
Output Propagation Delay (Notes 6 & 9)		10	15	ns
Output Hold Time (Notes 6 & 15)	5			ns
Transient Response (Note 10)		10		ns
Overvoltage Recovery Time (Note 11)		10		ns
AC LINEARITY (Note 12)				
Dynamic Linearity (Effective Bits)				
f_{AN} = 1.0MHz	7.0	7.5		dB
f_{AN} = 10MHz	6.0	7.0		dB
f_{AN} = 35MHz Over Temperature (Note 4)	5.0	5.4		dB
Signal-to Noise Ratio (SNR)				
f_{AN} = 1.0MHz	42	48		dB
f_{AN} = 10MHz	40	47		dB
f_{AN} = 35MHz Over Temperature (Note 4)	38	44		dB
Total Harmonic Distortion (THD)				
f_{AN} = 1.0MHz		−52	−42	dB
f_{AN} = 10MHz		−47	−40	dB
f_{AN} = 35MHz Over Temperature (Note 4)		−35	−33	dB
POWER SUPPLIES (Note 13)				
Positive Supply Current (I_{CC} + $I_{CC, D}$)		180	200	mA
Over Temperature			210	mA
Negative Supply Current (I_{EE} + $I_{EE, D}$) (Note 14)		83	95	mA
Over Temperature (Note 4)			100	mA
Power Consumption 25°C		1.3	1.43	Watts
Over Temperature (Note 4)			1.5	Watts
Power Supply Rejection				
V_{CC}		35		dB
V_{EE}		35		dB

SPECIFICATION NOTES

1. Analog input current varies linearly as a function of input voltage. See Figure 4, Analog Input Current versus Analog Input Voltage.
2. Full Power Bandwidth is the input frequency at which the output amplitude drops 3dB with respect to the measured output amplitude when driven by a 50-ohm line terminated in 50 ohms.
3. $+V_{REF}$ must always be more positive than $-V_{REF}$.
4. This specification is guaranteed over the applicable temperature range.
5. Digital outputs are measured with an output load of 100 ohms connected to −2 Volts.
6. Measured on the MSB.
7. The positive end point error is measured with the analog input equal to $+V_{REF}$ less 1.5 LSB's. The negative endpoint error is measured with the analog input equal to $-V_{REF}$ plus 0.5 LSB's.
8. Includes one full clock conversion (10 ns) plus output propagation delay time.
9. Measured from falling edge of STR2 to data valid.
10. Full step to 8-bit accuracy.
11. Time to recover to 8-bit accuracy after an overvoltage whose input is equal to 150% of the Full-Scale input voltage.
12. The AC linearity tests are performed at 100MHz sampling rate using the recommended strobe timing. The specified performance characteristics are derived from the FFT of the converter's response to a full scale (2 Vp-p) sinewave input. The analog input source impedance is 25 ohms (50 ohm line with a 50 ohm termination).
13. For normal operation, the power supplies should remain stable within ±5% (V_{CC}, $V_{CC, D}$ = +5.00V ±.25V and V_{EE}, $V_{EE, D}$ = −4.5V ±.22V). The positive supplies, V_{CC} and $V_{CC, D}$, may be operated from separate power supplies with the restriction that voltage differential between the two supplies is no greater than 0.1 Volts. Similarly the negative supplies, V_{EE} and $V_{EE, D}$ may be operated from separate supplies with the restriction that the voltage differential between the two supplies be no greater than 0.1 Volts.
14. The MN5901's digital outputs are compatible with 10K ECL logic when operated from −5.2V rather than −4.5V. Operation from −5.2V will result in an increase in power consumption.
15. Measured from the falling edge of STR2 to previous data invalid.

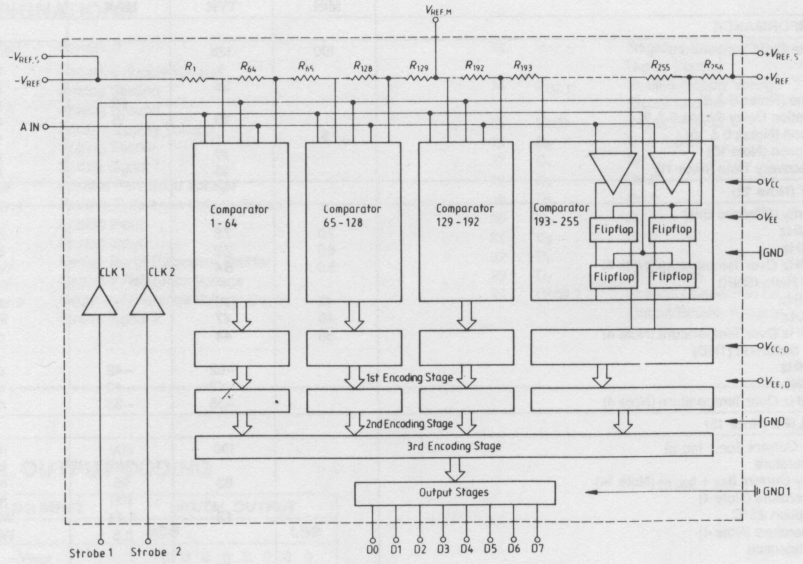


Figure 1.
Block Diagram

APPLICATION INFORMATION

The MN5901 has an input voltage range which is symmetrical about ground and has a low input capacitance. It can be easily driven from either a monolithic amplifier or a 50-ohm system without the burden of pre-amplifiers or level shifters. Lower input impedances will, however, result in improved performance. When driving the input with an amplifier, care should be taken to select one that has a high bandwidth and low output impedance to fully utilize the MN5901's wide input bandwidth. Two analog input pins are provided in order to reduce the losses caused by lead inductance. The user should connect these two pins together close to the package.

Internal reference voltages for the MN5901's 255 comparators are derived from the V_{REF} inputs by means of a reference ladder network. The MN5901 provides both reference input pins and reference sense pins. This allows the user to compensate for voltage errors caused by I-R drops from the reference inputs through the package to the reference ladder. Test circuit, Figure 8 includes circuitry that has been proven to be a simple and effective means of driving the reference inputs. The MN5901 does not include an overflow function. Consequently, the digital output will remain at 11111111 for inputs more positive than $+V_{REF}$ and will stay at 00000000 for inputs more negative than $-V_{REF}$. The pin $V_{REF,M}$ requires no adjustments and is provided for RF decoupling only.

LAYOUT SUGGESTIONS — It is strongly recommended that a substantial ground plane be placed under and around the MN5901. This can serve as the common tie point for both analog and digital grounds. An alternative is to use separate analog and digital ground planes. In this case, the digital ground plane should surround the digital output and clock pins and the analog ground plane should surround the analog input and reference pins. The analog and digital grounds should then be connected together with a 1 uh inductor. A third alternative is to use a single ground plane which is connected to digital ground. Both Analog GND and Digital GND pins on the MN5901 can be connected to this ground plane. The Analog and V_{REF} inputs should be referenced to a separate analog ground which could be RF isolated from digital ground through a 1uh inductor. There is an additional pin, GND1, provided for the collectors of the output emitter followers. This pin may be connected directly at the MN5901 to Digital Gnd or it may be connected to a common system ground external to the MN5901. In the latter case, it is recommended that the connecting wire have a ferrite bead around it. The selection of which grounding scheme is the best one to use is dependent on system configuration and noise levels. Experimentation is recommended.

Interference from digital switching may be minimized by isolating the various supplies. This can be accomplished by connecting 1 uh inductors in series with each of the four power supply pins: V_{CC}, $V_{CC,D}$, V_{EE} and $V_{EE,D}$.

It is recommended that .01uf ceramic decoupling capacitors be connected directly at the MN5901 to reduce the effects of system noise on converter accuracy. The $+V_{REF}$, $+V_{REF,S}$, $-V_{REF}$, $-V_{REF,S}$ and $V_{REF,M}$ pins should be decoupled to analog ground. The $V_{CC,D}$ and $V_{EE,D}$ pins should be decoupled to digital ground. V_{CC} and V_{EE} should be decoupled to whichever ground the Analog GND pin is connected. Low-inductance chip capacitors will provide the best results.

STROBE TIMING

Each of the 255 comparators in the MN5901 consists of a differential amplifier followed by a master/slave register stage. The master and slave sections of the register are controlled independently using strobe signals, STR1 and STR2, respectively.

When STR1 is low, the master section samples the difference between the analog input and the corresponding tap on the reference ladder. The rising edge of STR1 stores the result of this comparison in the master latch.

When STR2 is low, the slave latch samples the output of the master. This value is held in the slave following the rising edge of STR2 and allowed to propagate through the encoding stages to the A/D output.

For sampling frequencies up to 75MHz, the two strobe inputs of the MN5901 can be driven by complementary logic signals having a 50% duty cycle. To optimize performance above this sampling rate, however, requires slightly different timing. For operation at 100 MSPS, STR1 should still have a 50% duty cycle, being high for 5 nsec and low for 5 nsec. In order to provide the largest possible data valid window at the digital outputs (t_{VQ} in Figure 2), the low time of STR2 should be shortened to 3.5 nsec. Also, the sampling of the slave section of the register is optimized by delaying the falling edge of STR2 by 3 nsec after the rising edge of STR1. See Figure 2. Note that this results in the rising edge of STR2 occuring *after* the falling edge of STR1.

While this sounds complicated, implementation is easy and minor variations in this timing will not significantly affect performance. Using just three sections of a 100102 ECL gate, all required timing can be derived from a single-phase, 50% duty cycle clock. See Figure 3. All dynamic testing is done using this clock circuit.

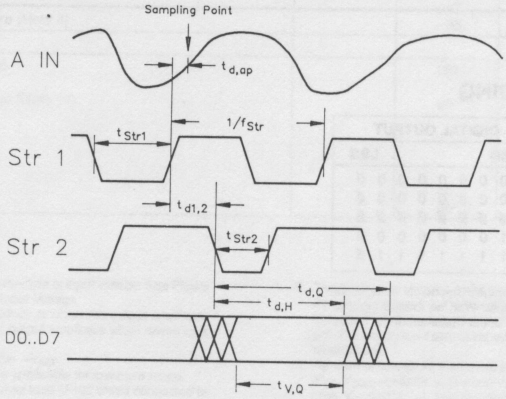


Figure 2.
Strobe Timing

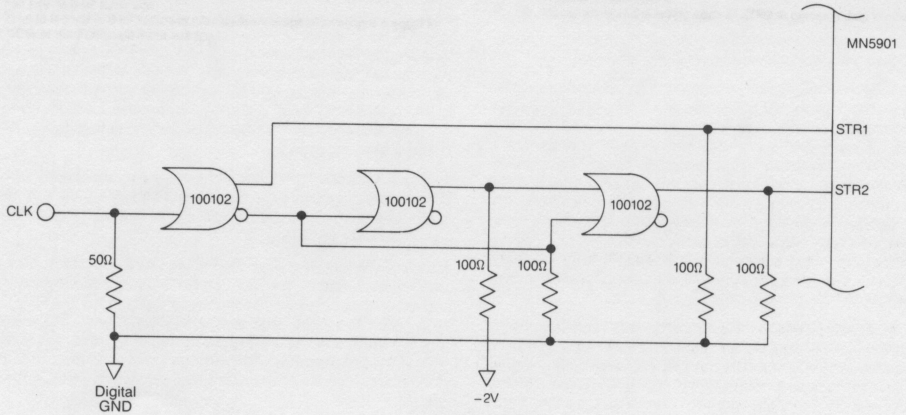


Figure 3.
Clock Circuitry

PIN DESIGNATIONS

Pin	Symbol	Function
1	V_{EE}	Negative Supply Voltage Analog Section
2	GND A	Analog Ground
3	V_{CC}	Positive Supply Voltage Analog Section
4	STR1	Strobe Signal 1
5	$+V_{REF}$	Positive Reference Voltage
6	$+V_{REF, S}$	Positive Reference Voltage Sense
7	A_{IN}	Analog Input
8	A_{IN}	Analog Input
9	$V_{REF, M}$	Center Tap of Reference Divider
10	$-V_{REF}$	Negative Reference Voltage
11	$-V_{REF, S}$	Negative Reference Voltage Sense
12	STR 2	Strobe Signal 2
13	$V_{EE, D}$	Negative Supply Voltage Digital Section
14	$V_{CC, D}$	Positive Supply Voltage Digital Section
15	GND	Digital Ground
16	D_0	Bit 0 (LSB)
17	D_1	Bit 1
18	D_2	Bit 2
19	D_3	Bit 3
20	D_4	Bit 4
21	D_5	Bit 5
22	D_6	Bit 6
23	D_7	Bit 7 (MSB)
24	GND 1	Ground Connection for Output Emitter Follower

DIGITAL OUTPUT CODING

ANALOG INPUT	DIGITAL OUTPUT							
	MSB							LSB
$-V_{REF}$	0	0	0	0	0	0	0	0
$-V_{REF} + ½LSB$	0	0	0	0	0	0	0	Ø
$-½LSB$	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
$+½LSB$	1	0	0	0	0	0	0	Ø
$+V_{REF} - 3/2LSB$	1	1	1	1	1	1	1	Ø

The analog input voltages shown above are the theoretical voltages for the corresponding digital output. Example: With an analog input of $-V_{REF} + ½LSB$, the output code will be at the transition of the codes 00000000 and 00000001.

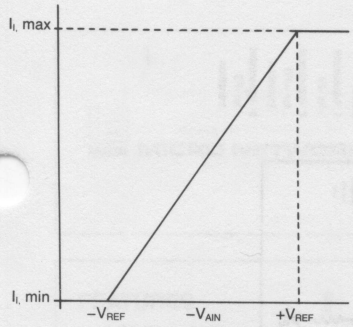


Figure 4.
Analog Input Current vs. Input Voltage

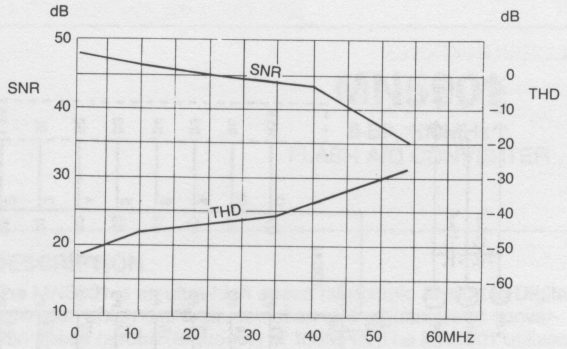


Figure 6.
Signal-to-Noise-Ratio (SNR) and Harmonic (THD) vs. Analog Frequency

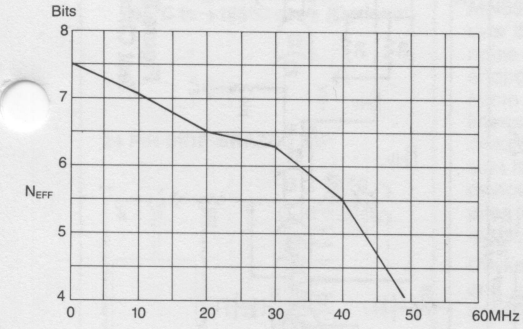


Figure 5.
Dynamic Linearity (Effective Bits) vs. Analog Frequency

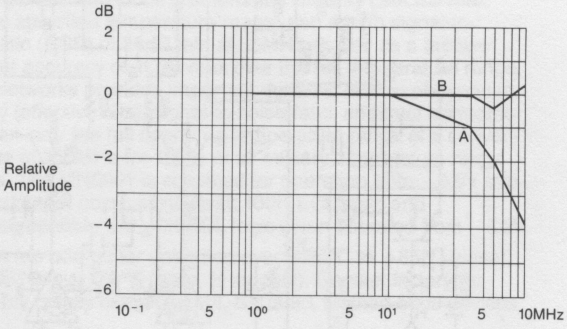


Figure 7.
Amplitude Response vs. Analog Frequency
A) Includes voltage drop across source impedance (25 ohms)
B) Does not include voltage drop across source (25 ohms)

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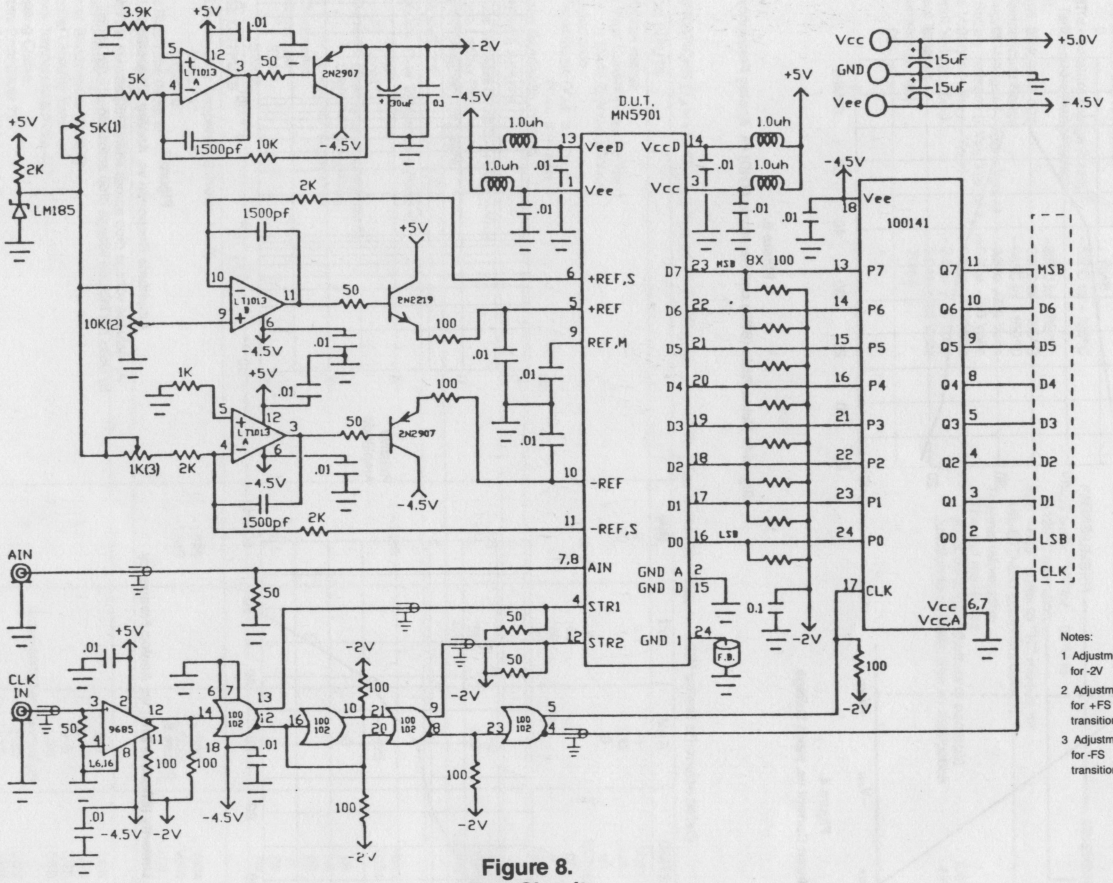

Figure 8.
Test Circuit