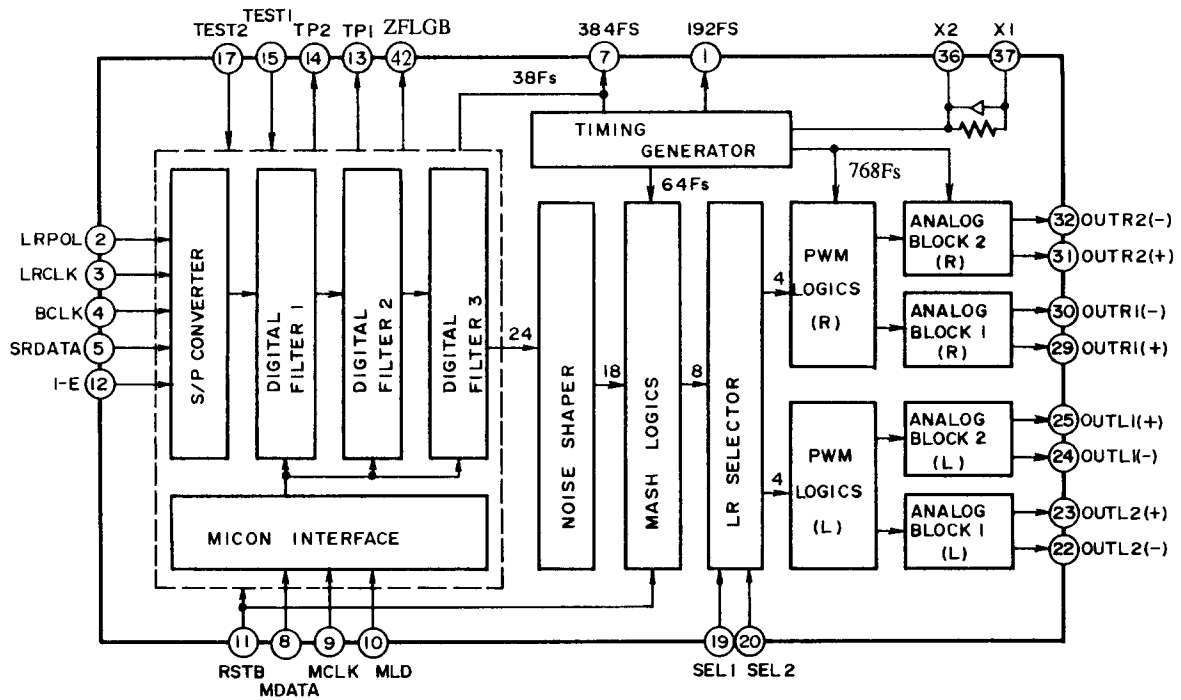


MN6472 (D/A Converter)



Pin No.	Symbol	Description	Pin No.	Symbol	Description															
1	192FS	192FS(=8.4672MHz) output terminal.	21	AVDD1	Power supply terminal 1 for analog system. (+5V)															
2	LRPOL	Polarity switching terminal for LRCLK.L ch at "H",R ch at "L".	22	OUTL2(-)	PWM output terminal for L 2 ch negative phase.															
3	LRCLK	Input terminal for LRCLK. At LR-POL "H":Lch data input at "H",Rch data input at "L". At LR-POL "L":Lch data input at "L",Rch data input at "H".	23	OUTL2(+)	PWM output terminal for L 2 ch positive phase.															
			24	OUTL1(-)	PWM output terminal for L 1 ch negative phase.															
			25	OUTL1(+)	PWM output terminal for L 1 ch positive phase.															
4	BCLK	Serial bit clock input terminal.	26	AVSS1	Ground terminal 1 for analog system.															
5	SRDATA	Input terminal for serial input data.	27	NC																
6	DVSS	Ground terminal for digital system.	28	AVSS2	Ground terminal 2 for analog system.															
7	384FS	384FS=16.9344MHz output terminal.	29	OUTR1(+)	PWM output terminal for R 1 ch positive phase.															
8	MDATA	Microprocessor command data input terminal.	30	OUTR1(-)	PWM output terminal for R 1 ch negative phase.															
9	MCLK	Clock input terminal for microprocessor command.	31	OUTR2(+)	PWM output terminal for R 2 ch positive phase.															
10	MLD	Microprocessor command load input terminal.Load at "L".	32	OUTR2(-)	PWM output terminal for R 2 ch negative phase.															
11	RSTB	Reset terminal.Reset at "L".	33	AVDD2	Power supply terminal 2 for analog system. (+5V)															
12	I-E	Signal processing LSI format at "L",and I ² S format at "H".	34	DVDD1	Power supply terminal 1 for digital system. (+5V) (Power supply for oscillation circuit)															
13	TP1	Output terminal 1 for digital filter portion test.																		
14	TP2	Output terminal 2 for digital filter portion test.																		
15	TEST1	Test signal input terminal 1 for testing digital filter portion. Normally "L".	35	DVSS1	Ground terminal 1 for digital system. (Ground for oscillation circuit)															
16	DVDD	Power supply terminal for digital system. (Terminal for COM potential fixing) (+5V)	36	X2	Crystal oscillation terminal.															
			37	X1	Crystal oscillation terminal.(External clock input terminal)															
17	TEST2	Test signal input terminal 2 for testing digital filter portion. Normally "L".	38	DVSS2	Ground terminal 2 for digital system.															
			39	NSUB	Connect to D-VDD.(Potential fixing terminal for Silicon circuit board)															
18	NC		40	DVDD2	Power supply terminal 2 for digital system. (+5V)															
19 20	SEL1 SEL2	<table><tr><td>SEL1</td><td>SEL2</td><td>Output</td></tr><tr><td>L</td><td>L</td><td>Normal stereo output</td></tr><tr><td>L</td><td>H</td><td>Only Lch output</td></tr><tr><td>H</td><td>L</td><td>Only Rch output</td></tr><tr><td>H</td><td>H</td><td>Both Rch and Lch negative output</td></tr></table>	SEL1	SEL2	Output	L	L	Normal stereo output	L	H	Only Lch output	H	L	Only Rch output	H	H	Both Rch and Lch negative output	41	NC	
		SEL1	SEL2	Output																
		L	L	Normal stereo output																
		L	H	Only Lch output																
		H	L	Only Rch output																
H	H	Both Rch and Lch negative output																		
42	ZFLGB	Output terminal for zero output detector.																		