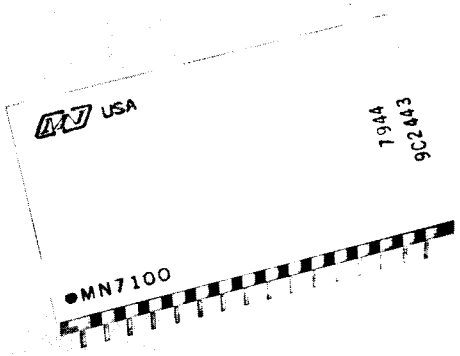


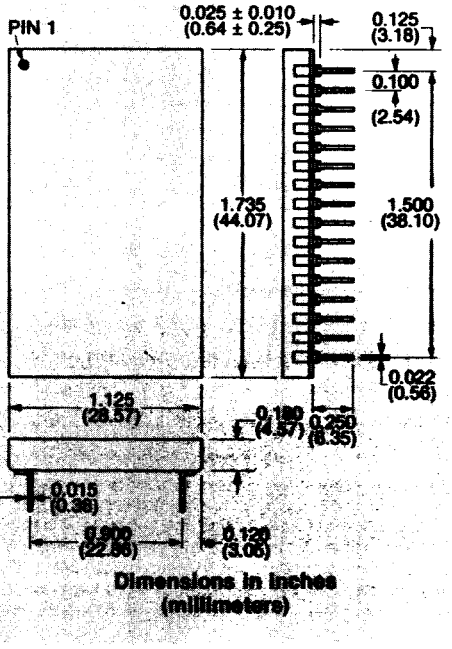
MN7100

8 BIT 8 CHANNEL DATA ACQUISITION SYSTEM

FEATURES

- **Complete System**
  - **Multiplexer**
  - **Sample/Hold**
  - **A/D Converter**
  - **Control Logic**
- **Small 32 Pin DIP**
- **± ½ LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Random or Sequential Addressing**
- **75,000 Channels/Sec Guaranteed**
- **Full Mil Operation −55°C to +125°C Available Fully Screened and Processed to Method 5008 of MIL-STD-883**

32 PIN DIP



DESCRIPTION

The MN7100 was the first complete, 8 Bit Data Acquisition System (DAS) ever offered in a Dual-In-Line package. It is a complete system including input Multiplexer with address register, Sample/Hold Amplifier (S/H), A/D Converter, clock and necessary controlling logic. Its eight input channels are either randomly or sequentially addressable and have an input impedance greater than 10 meg ohms.

The MN7100 is actively laser trimmed as a complete device eliminating normally annoying DAS errors such as S/H pedestal error. The system is adjustment-free. No external gain or offset adjusting potentiometers are required to guarantee an overall system error of better than ±1 LSB at +25°C and better than ±2 LSB's over the entire operating temperature range.

The MN7100's S/H has an acquisition time of 6 μSec and the A/D conversion time of 7 μSec allows an overall throughput rate of over 75,000 channels/sec. Units may be ordered for either 0°C to +70°C or −55°C to +125°C operation and high reliability processing, screening, and qualification to the requirements of MIL-STD-883 Method 5008 are available for military/aerospace applications.

APPLICATIONS

The MN7100 is easily expandable up to 256 channels using MN7110 multiplexer expanders or external multiplexers. Its small size and low power consumption make it ideally suited for industrial control and monitoring systems. Highly reliable thin-film hybrid construction, optional MIL-STD-883 screening, and performance specifications guaranteed from −55°C to +125°C make it the right choice for low resolution military/aerospace data acquisition requirements.

Micro Networks Corporation
324 Clark Street, Worcester, Massachusetts 01606 • (617) 852-5400
A SUBSIDIARY OF UNITRODE CORPORATION

MN7100 8 BIT 8 CHANNEL DATA ACQUISITION SYSTEM

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
Positive Supply (Pin 19)	−0.5 to +18 Volts
Negative Supply (Pin 20)	+0.5 to −18 Volts
Logic Supply (Pin 21)	−0.5 to +7 Volts
Analog Inputs (Pins 8-15)	±20 Volts
Digital Inputs (Pins 1-4, 32)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN7100 H/B

Standard device is specified for 0°C to +70°C operation. Add "H" suffix for −55°C to +125°C operation.

Add "/B" for 100% screening according to Method 5008 of MIL-STD-883.

SPECIFICATIONS (TA = 25°C, Voltage ± 15, +5, Unless Otherwise Noted)

ANALOG INPUT CHARACTERISTICS:			
Number of Channels		8 Single Ended	
Input Voltage Range (Note 2)		−10 to +10 Volts	
Input Impedance		10 meg Ohm	
Direct S/H Input Impedance		10 meg Ohm	
TRANSFER CHARACTERISTICS:			
Resolution		8	Bits
Quantization Error		± ½	LSB
Linearity (0 to 70°C) Note 1		± ½	LSB
Zero Error (0 to 70°C) Note 1		± 1	LSB
Absolute Accuracy		± 1	LSB
Absolute Accuracy (0 to 70°C) Note 1		± 2	LSB
Cross Talk	−65		db
DYNAMIC CHARACTERISTICS:			
Acquisition Time	5	6	μ Sec
Aperature	50		η Sec
A/D Conversion Time	6	7	μ Sec
Throughput Rate	90,000		Conversions/Sec
POWER REQUIREMENTS:			
Current Drain +15V	10	16	mA
Current Drain −15V	12	25	mA
Current Drain +5V	70	110	mA
Supply Rejection +15V	.04		%FS/%PS
Supply Rejection −15V	.001		%FS/%PS
Supply Rejection +5V	.001		%FS/%PS
Power Consumption	680	1165	mW

Note 1. For "H" models, this specification applies over the −55°C to +125°C operating temperature range.

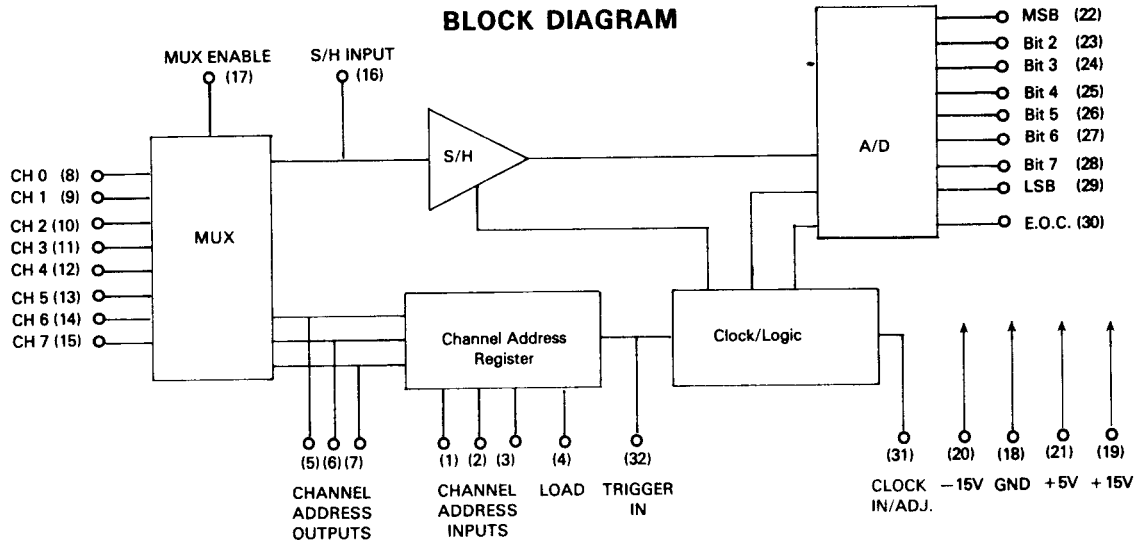
Note 2. Contact factory for other available input voltage ranges.

LOGIC CODING

ANALOG INPUT	DIGITAL OUTPUT
(DC Volts)	MSB LSB
+10.000	1111 1111
+ 9.922	1111 1110*
+ 0.078	1000 0000*
0.000	0000 0000*
− 0.078	0111 1110*
− 9.922	0000 0000*
−10.000	0000 0000

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the system continuously sampling and converting, the output bits indicated as 0 will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. The transition from digital output 0000 0000 to digital output 0000 0001 (or vice versa) will ideally occur at −9.922V. Subsequently, an input voltage more negative than −9.922V will give an output of all "0's". The transition from digital output 0111 1111 to digital output 1000 0000 (or vice versa) will ideally occur at an input of zero volts. The 1111 1110 to 1111 1111 transition should occur at +9.922V. An input greater than +9.922V should give all "1's".

BLOCK DIAGRAM



OPERATION

INPUTS:

The analog input signals are connected to the eight input channels. Input levels should not exceed ±10 volts and it is recommended that unused channel inputs be grounded. Multiplex inputs may be expanded to 256 channels by addition of multiplexers and logic.

ADDRESSING:

Both sequential and random addressing are available in the MN7100. For sequential addressing connect LOAD to logic "1", and the channels will sequence from Channel 0 to Channel 7, advancing one channel on the leading edge of each TRIGGER pulse. For random operation the desired channel address (in 4 2 1 binary coding) is applied to the CHANNEL ADDRESS inputs, and LOAD set to logic "0". The rising edge of the next TRIGGER input will update the channel address. The CHANNEL ADDRESS OUTPUTS provided indicate the last channel selected.

TRIGGERING:

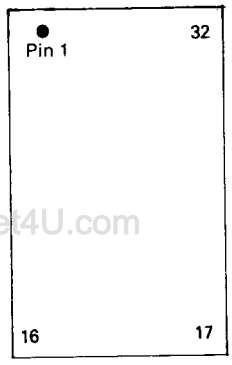
The rising edge of a positive TRIGGER input pulse updates the channel address, the falling edge commands the sample-and-hold amplifier to the track mode and disables the system clock. E.O.C. is low. Turning off the clock reduces noise during signal acquisition. 6 μSec later the S/H goes into the hold mode and A/D conversion begins. E.O.C. now goes high. 7 μSec later the conversion is complete and E.O.C. drops low again.

CLOCK:

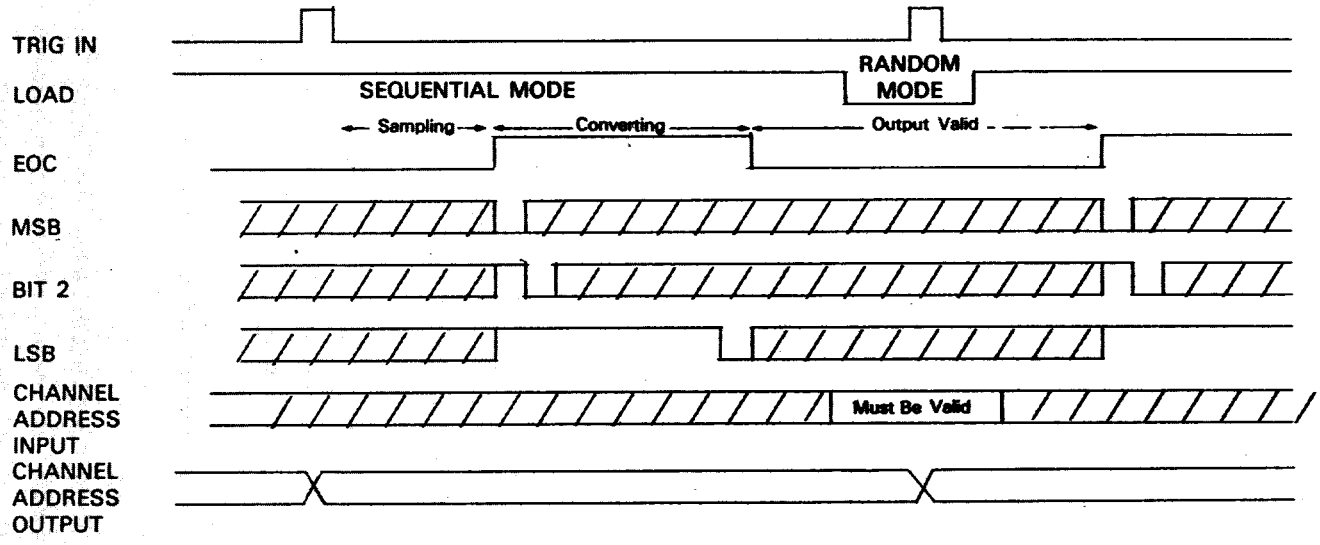
The MN7100 can be operated from its internal clock or from a user clock applied to the clock input. The internal clock is disabled during the analog acquisition time to reduce noise. External clocks should not exceed 400 nSec pulse widths or a 1.5 MHz repetition rate. In addition, the frequency of the internal clock can be varied by connection of one external resistor or capacitor. A resistor (20k Ohms or higher) connected from Pin 31 to the +5V Supply will increase the clock repetition rate inversely with resistance. A capacitor connected from Pin 31 to ground will decrease the clock rate directly with capacitance. The clock rate may be observed on Pin 31 as an RC charging waveform of approximately 0.5Vp. Loading at this point should be greater than 10 meg Ohms to avoid shifting the clock rate.

EXPANSION

The MN7100 Data Aquisition System can be expanded to over 256 analog input channels with Micro Networks MN7110 Multiplexer Expanders. One MN7100 and one MN7110 form a complete 24 channel DAS in two small 32 pin dual-in-line packages, and additional MN7110's and a minimum of TTL Logic may be used for further expansion. Applications diagrams for channel expansion are shown on the MN7110 Data Sheet.



PIN	FUNCTION	PIN	FUNCTION
1	Address Input−1	17	Mux Enable
2	Address Input−2	18	Ground
3	Address Input−4	19	+15 Volts
4	Load	20	−15 Volts
5	Address Output−1	21	+5 Volts
6	Address Output−2	22	MSB Out
7	Address Output−4	23	Bit 2
8	Channel 0	24	Bit 3
9	Channel 1	25	Bit 4
10	Channel 2	26	Bit 5
11	Channel 3	27	Bit 6
12	Channel 4	28	Bit 7
13	Channel 5	29	LSB
14	Channel 6	30	End of Conversion
15	Channel 7	31	Clock In/Adj
16	Sample/Hold Input	32	Trigger Input



Digital Inputs	Logic Signal	Description	Load Presented	Min. Pulse Width	Notes
Mux Enable	"1"	Enables Internal Mux	1 uA	Level	Tie to Logic "1" unless additional external MUX's are used for expansion.
	"0"	Disables Internal MUX	1 uA		Logic "0" $<$ 0.4V Logic "1" $>$ 4.0V
Channel Address Inputs	3 Lines 421 Binary	Selects desired channel in random address mode	TTL	125 nSec.	Must be set up 100 nSec before clocking trigger and be valid through rising edge of trigger.
Load	"1" "0"	Sequential Address Mode Random Address Mode	TTL	Level	Data will be loaded on the first rising edge of trigger.
Trigger	"0" to "1"	Starts Data Acquisition Process	TTL	100 nSec.	
Clock		System Clock	20 pf Parallel 30k	100 nSec Min. 400 nSec Max.	1.5 MHz Max. Clock rate can be varied or an external clock used.

Digital Outputs	Logic Signal	Description	Max. Load	Notes
Data Outputs	True Binary	Parallel digital data outputs 8 lines MSB thru LSB	6 TTL	Output data is valid after E.O.C. goes low.
Channel Address Outputs	421 Binary	Channel address outputs 3 lines	3 TTL	Indicates channel being converted.
E.O.C.	"0"	Conversion process complete output data valid	6 TTL	E.O.C. goes to logic "1" 5 uSec after trigger returns low and returns to logic "0" when conversion is complete.

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