MICRO NETWORKS

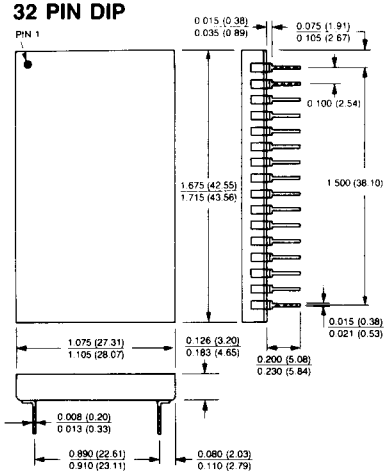
MN7120

8-Bit, 8-CHANNEL
DATA ACQUISITION SYSTEM
with 3-STATE OUTPUTS

FEATURES

- **Complete System:**
  Input Multiplexer
  Track-Hold Amplifier
  8-Bit A/D Converter
  3-State Output Buffer
  Control Logic
- **Small 32-Pin DIP**
- **±1/2 LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Random or Sequential Addressing**
- **75,000 Channels/sec Guaranteed Throughput**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN7120 is a complete, 8-bit, 8-channel data acquisition system with 3-state outputs in a single, 32-pin, hermetically sealed dual-in-line package. Contained in the single package are input multiplexer with address register, track-hold (T/H) amplifier, A/D converter, 3-state output buffer, clock and all the necessary controlling logic. The basic system's 8 input channels can be either randomly or sequentially addressed, and input impedance is greater than 10 megohms. The number of input channels is easily expanded with external multiplexers.

MN7120 is actively laser trimmed as a complete device eliminating the normally annoying DAS errors such as T/H pedestal error. The system is adjustment-free. No external gain or offset adjusting potentiometers are required to guarantee an overall system error of better than ±1 LSB at +25°C and better than ±2 LSB's over the entire operating temperature range.

The MN7120's T/H has an acquisition time of 6μsec, and the A/D's conversion time of 7μsec allows an overall throughput rate of over 75,000 channels/sec. The standard device is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. The MN7120H/B is available with Environmental Stress Screening while the MN7120H/B CH is fully screened in accordance with MIL-H-38534.

MN7120's output buffer facilitate interfacing to microprocessor and microcomputer buses. Normally, simple address decoding is all that has to be added to give data acquisition capability to your microprocessor-based system. MN7120 is ideally suited for industrial control and monitoring systems. Highly reliable thin-film hybrid construction, optional MIL-H-38534 screening, and performance specifications guaranteed from −55°C to +125°C make it the right choice for low-resolution military/aerospace data acquisition requirements.

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7120 8-Bit 8-CHANNEL DAS with 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7120	0°C to +70°C
MN7120H, MN7120H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (Pin 19)	−0.5 to +18 Volts
−15V Supply (Pin 20)	+0.5 to −18 Volts
Logic Supply (Pin 21)	−0.5 to +7 Volts
Analog Inputs (Pins 8-15)	±15 Volts
Digital Inputs (Pins 1-4, 32)	-0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **MN7120H/B CH**

Standard Part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels (Note 1)		8		
Input Voltage Range		±10		Volts
Input Impedance		10		Mohm
Direct T/H Input Impedance (Pin 16)		10		Mohm
TRANSFER CHARACTERISTICS (Note 2)				
Resolution		8		Bits
Quantization Error		±½		LSB
Integral Linearity Error: Initial (+25°C)		±⅛	±½	LSB
Over Temperature (Note 3)		±¼	±½	LSB
Zero Error (Note 4): Initial (+25°C)		±¼	±1	LSB
Over Temperature (Note 3)		±½	±1	LSB
Full Scale Absolute Accuracy (Note 5): Initial (+25°C)		±½	±1	LSB
Over Temperature (Note 3)		±1	±2	LSB
DYNAMIC CHARACTERISTICS				
T/H Acquisition Time (Note 6)		5	6	μsec
T/H Aperture Delay Time		50		nsec
A/D Conversion Time		6	7	μsec
Throughput Rate (Channels/sec)	75	90		kHz
Crosstalk Attenuation	65			dB
POWER SUPPLIES				
Power Supply Range: ±15V Supply		±5		%
+5V Supply		±5		%
Power Supply Rejection: +15V Supply		±0.04		%FSR/%Vs
−15V Supply		±0.001		%FSR/%Vs
+5V Supply		±0.001		%FSR/%Vs
Current Drains: +15V Supply		+10	+16	mA
−15V Supply		−12	−25	mA
+5V Supply		+70	+110	mA
Power Consumption		680	1165	mW

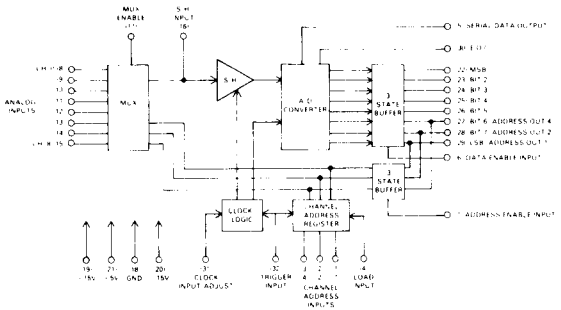
SPECIFICATION NOTES:

1. Eight single-ended input channels can be increased with external multiplexers.
2. For an 8-bit system with a 20V FSR (full scale range), 1 LSB is equal to 78.1mV.
3. MN7120 is fully specified for 0°C to +70°C operation. MN7120H and MN7120H/B are fully specified for −55°C to +125°C operation.
4. Zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000. The ideal value at which this transition should occur is 0 Volts.
5. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors and is specified without adjustment. The full scale accuracy specification applies at both positive and negative full scale. It is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1110 to 1111 1111 or from 0000 0000 to 0000 0001. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
6. Specified for a 20V step acquired to ±½LSB.

Analog Input (DC Volts)	Digital Output MSB LSB
+10.000	1111 1111
+9.922	1111 111Ø*
+0.078	1000 000Ø*
0.000	ØØØØ ØØØØ*
−0.078	0111 111Ø*
−9.922	0000 000Ø*
−10.000	0000 0000

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the system continuously sampling and converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. The transition from digital output 0000 0000 to digital output 0000 0001 (or vice versa) will ideally occur at −9.922V. Subsequently, an input voltage more negative than −9.922V will give an output of all "0's". The transition from digital output 0111 1111 to digital output 1000 0000 (or vice versa) will ideally occur at an input of zero volts. The 1111 1110 to 1111 1111 transition should occur at +9.922V. An input greater than +9.922V should give all "1's".

BLOCK DIAGRAM



DIGITAL INPUTS AND OUTPUTS

Digital Inputs	Logic Signal	Description	Load Presented	Min. Pulse Width	Notes
Mux Enable	"1"	Enables Internal Mux	1 uA	Level	Tie to Logic "1" unless additional external MUX's are used for expansion. Logic "0" <0.4V Logic "1" >4.0V
	"0"	Disables Internal Mux	1uA		
Channel Address Inputs	3 Lines 421 Binary	Selects desired channel in random address mode	TTL	125 nSec	Must be set up 100 nSec before clocking trigger and be valid through rising edge of trigger.
Load	"1"	Sequential Address Mode	TTL	Level	Data will be loaded on the first rising edge of trigger.
	"0"	Random Address Mode			
Trigger	"0" to "1"	Starts Data Acquisition Process	TTL	100 nSec	
Clock		System Clock	20 pf Parallel 30k	100 nSec Min. 400 nSec Max.	1.5 MHz Max. Clock rate can be varied or an external clock used.
Address Enable	"0"	Enables Address Output Three State Buffers	1 uA	Level	Tie to logic "1" if Address Output is not needed.
Data Enable	"0"	Enables Data Output Three State Buffers	1 uA	Level	Tie to logic "0" if 3-State Outputs are not required.

Digital Outputs	Logic Signal	Description	Max. Load	Notes
Data Outputs	True Binary	Parallel digital data outputs 8 lines MSB thru LSB	1 TTL	Output data is valid after E.O.C. goes low.
Channel Address Outputs	421 Binary	Channel address outputs 3 lines	1 TTL	Indicates channel being converted.
E.O.C.	"0"	Conversion process complete output data valid	6 TTL	E.O.C. goes to logic "1" 5 uSec after trigger returns low and returns to logic "0" when conversion is complete.
Serial Data	NRZ	Serial Data Output	3 TTL	Output occurs during the A/D conversion period.

PIN	FUNCTION	PIN	FUNCTION
1	Address Input — 1	17	Mux Enable
2	Address Input — 2	18	Ground
3	Address Input — 4	19	+15 Volts
4	Load	20	−15 Volts
5	Serial Data Output	21	+5 Volts
6	Data Enable Input	22	MSB Out
7	Address Enable Input	23	Bit 2
8	Channel 0	24	Bit 3
9	Channel 1	25	Bit 4
10	Channel 2	26	Bit 5
11	Channel 3	27	Bit 6/Address Output — 4
12	Channel 4	28	Bit 7/Address Output — 2
13	Channel 5	29	LSB/Address Output — 1
14	Channel 6	30	End of Conversion
15	Channel 7	31	Clock In/Adj
16	Sample/Hold Input	32	Trigger Input

INPUTS

It is recommended that unused analog inputs be grounded.

ADDRESSING

Both sequential and random addressing are available in the MN7120. For sequential addressing connect LOAD to logic "1". Channels will sequence from 0 thru 7, advancing one channel on the leading edge of each TRIGGER pulse. For random channel addressing the channel address (421 binary code) is applied to the CHANNEL ADDRESS INPUTS with LOAD at logic "0". The rising edge of the next TRIGGER pulse will update the channel address. The CHANNEL ADDRESS OUTPUTS, when enabled, indicate the last channel selected.

TRIGGERING

The rising edge of a positive TRIGGER pulse updates the channel address, the falling edge commands the sample/hold to the sample mode.

CLOCK

The MN7120 can be operated from it's internal clock or an external clock applied to the CLOCK INPUT. The internal clock is disabled during analog signal acquisition to reduce noise. A resistor (20k ohms or higher) connected from the CLOCK INPUT to +5V will increase the clock rate inversly with resistance. If the resistor is connected to ground the clock frequency will decrease inversly with resistance. The clock rate can be observed as an RC charging waveform of 0.5Vp at the CLOCK INPUT. Loading at this point should be greater than 10M ohms to avoid shifting the clock rate.

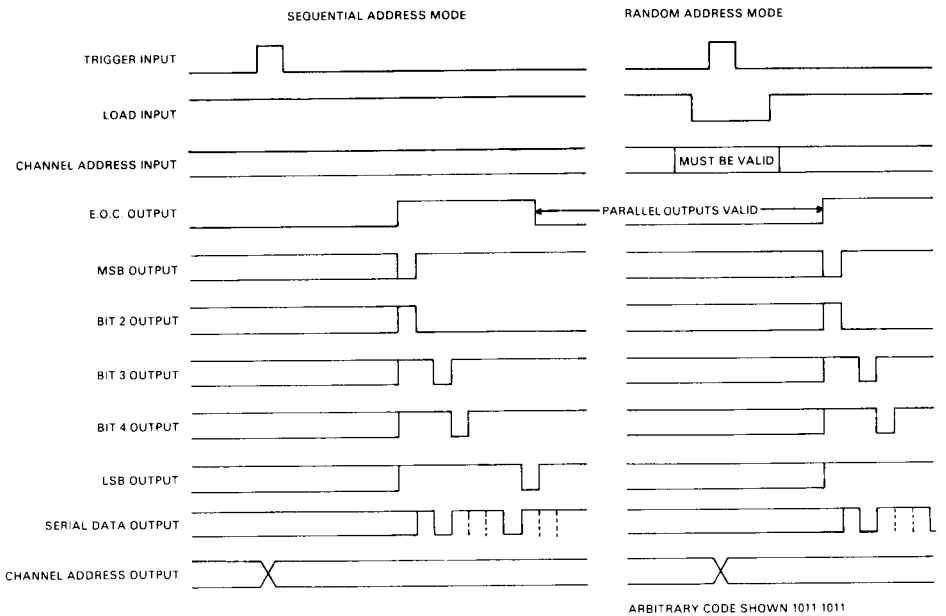
THREE STATE OUTPUTS

Three state buffers are employed on the data and channel address outputs. Channel address or data outputs are selected by a logic "0" on the corresponding ENABLE INPUT. If neither ENABLE is selected the 8 output lines will assume a high impedance state. The CHANNEL ADDRESS and DATA outputs should not be enabled simultaneously. Parallel data will be valid in 95 nsec after the Enable pulse goes Low.

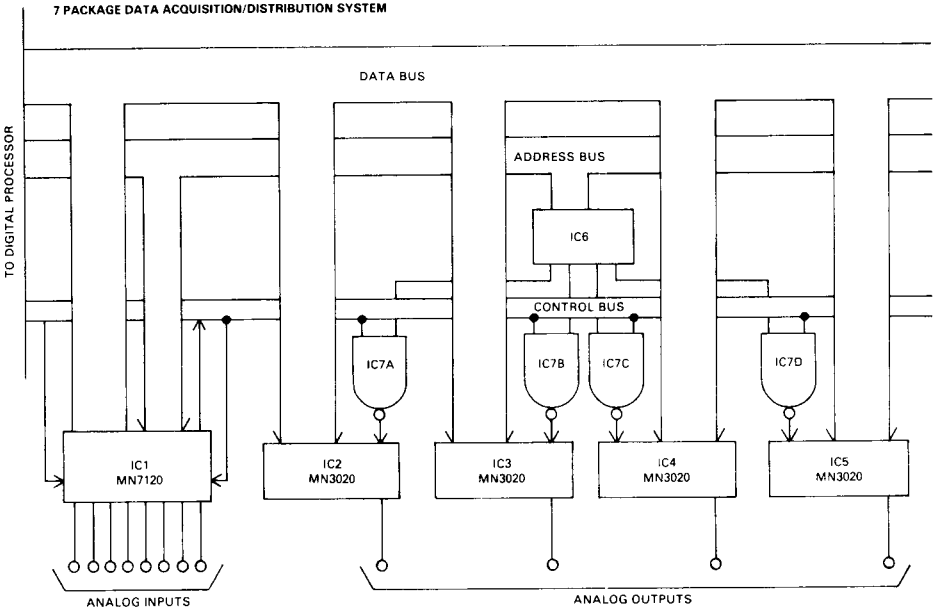
SERIAL DATA OUTPUT

The MN7120 provides serial as well as parallel data output. The first falling edge of the Bit 2 output can be used to indicate the start of the serial output data.

TIMING DIAGRAM



7 PACKAGE DATA ACQUISITION/DISTRIBUTION SYSTEM



IC1 Micro Networks MN7120 Data Acquisition System with Three State Outputs
IC2-5 Micro Networks MN3020 D/A with Input Buffers
IC6 Signetics 8223 Field Programmable ROM