MICRO NETWORKS

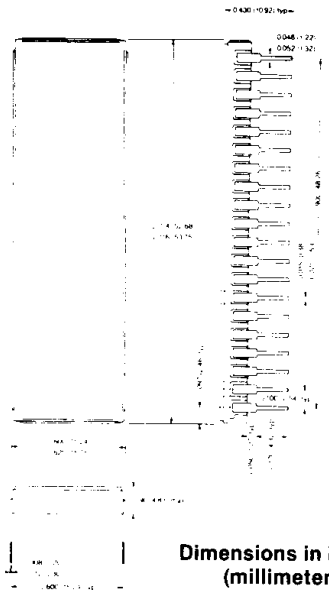
MN7140

12-Bit, 8-CHANNEL
DATA ACQUISITION SYSTEM

FEATURES

- **Complete DAS:**
  Input Multiplexer
  Address Register
  Instrumentation Amp
  Track-Hold Amp
  12-Bit A/D Converter
  Clock, Control Logic
- **Industry Standard 40-Pin Double-Wide DIP**
- **Random or Sequential Addressing**
- **±0.1%FSR Maximum Overall System Accuracy**
- **Adjustment-Free: No Gain or Offset Adjustments Necessary**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

40 PIN DIP



Dimensions in inches (millimeters)

DESCRIPTION

MN7140 is a complete 12-bit data acquisition system in an industry-standard, 40-pin, double-wide dual-in-line package. This unit contains an 8-channel input multiplexer (with latch and counter for either random or sequential addressing), a true instrumentation amplifier (G=1, Z_{in} =100MΩ), a track-hold amplifier (with internal hold capacitor), a 12-bit successive approximation A/D converter (with internal clock and reference), and all the timing and control logic necessary to operate the system with a single trigger pulse. The standard MN7140 has 8 single-ended inputs and can easily be expanded to 16 single-ended or 8 differential inputs with the addition of a single external multiplexer.

Active laser trimming of fully assembled units enables us to produce adjustment-free devices that guarantee performance equal to or exceeding all other modular and hybrid systems. Overall system linearity (±1/2LSB) and absolute accuracy (±0.1%FSR) are fully specified and guaranteed at all temperatures. The standard device is fully specified for either 0°C to +70°C or −55 C to +125°C ("H" model) operation. The MN7140H/B and MN7143H/B are available with Environmental Stress Screening while MN7140H/B CH and MN7143H/B CH are screened in accordance with MIL-H-38534. Contact factory for availability of "CH" devices.

For years, MN7140 was the only DIP-packaged 12-bit DAS to fully specify and guarantee linearity and overall system accuracy, without adjustment, over its entire operating temperature range. This feature, coupled with hermetic packaging and optional MIL-H-38534 screening make it the established choice for high-resolution military/aerospace and severe-environment industrial data acquisition applications. Its thin-film hybrid construction and low chip count ensure the highest reliability.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7140 12-Bit 8-CHANNEL DATA ACQUISITION SYSTEM

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Specified Temperature	0°C to +70°C (Standard)
	−25°C to +85°C ("E" Model)
	−55°C to +125°C ("H" Model)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 20)	−0.5 to +18 Volts
−15V Supply (Pin 21)	+0.5 to −18 Volts
Logic Supply (Pin 23)	−0.5 to +16 Volts
Analog Inputs (Pins 1-4, 37-40)	±15 Volts
Digital Inputs (Pins 31-36, 11)	−0.5 to +Logic Supply

ORDERING INFORMATION

PART NUMBER — MN714X H/B CH

Select MN7140 (±10V) or MN7143 (0 to +10V).

Standard Part is specified for 0°C to +70°C operation. Add "E" suffix for specified −25°C to +85°C operation. Add "H" suffix for specified −55°C to+125°C operation.

Add "/B" to "H" devices for Environmental Stress Screening.

Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V, unless otherwise specified)

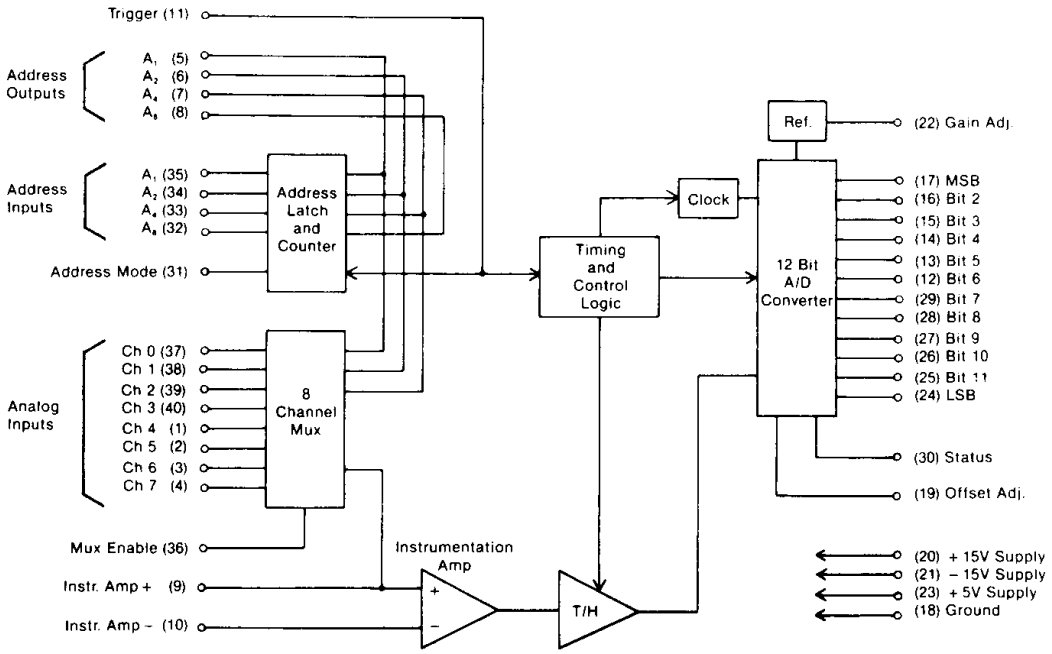
ANALOG INPUTS	MIN.	TYP.	MAX	UNITS
Number of Input Channels (Note 1)		8		Channels
Input Voltage Range (Note 2)		0 to +10V, ±10V		Volts
Input Impedance	100			Mohm
Input Capacitance		10		pF
Input Bias Current (Note 3): +25°C		10	25	nA
−55°C to +125°C			250	nA
CMRR (Note 4)		80		dB
DIGITAL INPUTS				
Logic Levels: Logic "1"				
Mux Enable	4			Volts
Other Inputs (Note 5)	3.5			Volts
Logic "0"				
Mux Enable			0.8	Volts
Other Inputs (Note 5)			1.5	Volts
Loading: Logic "1"				
Mux Enable		0.005	10	μA
Other Inputs (Note 5)		0.005	1.3	μA
Logic "0"				
Mux Enable		−0.005	−10	μA
Other Inputs (Note 5)		−0.005	−1.3	μA
Trigger Pulse Width	240			nSec
Setup Time, Address Mode and Address Inputs to Trigger (Note 6)	300			nSec
TRANSFER CHARACTERISTICS				
Linearity Error (Notes 7, 8):				
+25°C		±¼	±½	LSB
0°C to +70°C		±½	±1	LSB
−25°C to +85°C ("E" Model)		±½	±1	LSB
−55°C to +125°C ("H" Model)		±½	±1	LSB
Differential Linearity Error		±½		LSB
No Missing Codes		Guaranteed		
Absolute Accuracy Error (Notes 9, 10):				
+25°C		±0.05	±0.1	%FSR
0°C to +70°C		±0.15	±0.4	%FSR
−25°C to +85°C ("E" Model)		±0.15	±0.4	%FSR
−55°C to +125°C ("H" Model)		±0.2	±0.4	%FSR
Gain Error (Note 10)		±0.025		%
Gain Drift		±20		ppm/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time (20V Step to ±0.01%) (Note 11)		8	10	μSec
A/D Conversion Time		20	25	μSec
Throughput Rate (Channels/Sec.)	28.5	35		KHz
Full Power Bandwidth (Note 12)		250		KHz
Crosstalk (1KHz, 1KΩ Source Impedance)		−80		dB
Feedthrough (1KHz, 20Vp-p) (Note 13)		±0.01		%
DIGITAL OUTPUTS				
Digital Output Coding		Complementary Offset Binary		
Logic Levels (All Outputs): Logic "1" I_o = −10 μA	4			Volts
I_o = −360 μA	2.4			Volts
Logic "0" I_o = 10 μA			0.5	Volts
I_o = 360 μA			0.4	Volts

POWER SUPPLY REQUIREMENTS				
Power Supply Range: + 15V Supply	+ 14.55	+ 15.00	+ 15.45	Volts
− 15V Supply	− 14.55	− 15.00	− 15.45	Volts
+ 5V Supply	+ 4.75	+ 5.00	+ 5.25	Volts
Power Supply Rejection: + 15V Supply		± 0.003		%FSR/%Vs
− 15V Supply		± 0.003		%FSR/%Vs
+ 5V Supply		± 0.001		%FSR/%Vs
Current Drains: + 15V Supply		30	50	mA
− 15V Supply		− 50	− 75	mA
+ 5V Supply		10	16	mA
Power Consumption		1250	1955	mW

SPECIFICATION NOTES:

1. The standard MN7140 has 8 single-ended input channels. See page 6 for expanded single-ended and differential operation using additional external multiplexers.
2. Contact factory for other available input voltage ranges.
3. Input bias current specification is for the "on" multiplexer channel. "Off" channel leakage current is ±50 nA maximum at all temperatures.
4. CMRR specification is for full differential operation using an external multiplexer. See page 6.
5. Other Digital Inputs include: ADDRESS INPUTS A_1, A_2, A_4, and A_8, and the ADDRESS MODE INPUT.
6. If using random addressing or if changing from one addressing mode to the other, ADDRESS INPUT or ADDRESS MODE information must be present a minimum of 300 nSec prior to the rising edge of TRIGGER.
7. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range. See Ordering Information.
8. One LSB for a 12 bit system corresponds to 0.024%FSR. See note 9.
9. FSR stands for Full Scale Range and is equivalent to the peak to peak voltage of the system's input range. For the MN7140, FSR = 20 volts, and 1 LSB = 4.88 mV.
10. See sections on Absolute Accuracy and Gain Errors for an explanation of how Micro Networks tests and specifies these parameters. the tutorial section of the Micro Networks Product Guide and Applications Manual for a complete discussion of DAS specifications.
11. The MN7140's internal timing control logic allows 10 μSec for channel switching, amplifier settling, and signal acquisition. See Summary of Operation.
12. This spec applies from analog input to the output of the internal S/H amplifier and it applies when the S/H is acquiring and tracking an analog input signal. It is the frequency at which a 20V-pp input/output sine wave becomes slew rate limited.
13. This spec also applies from the analog input to the output of the internal S/H amplifier and it applies when the S/H is holding an analog signal i.e., when the A/D converter is converting.

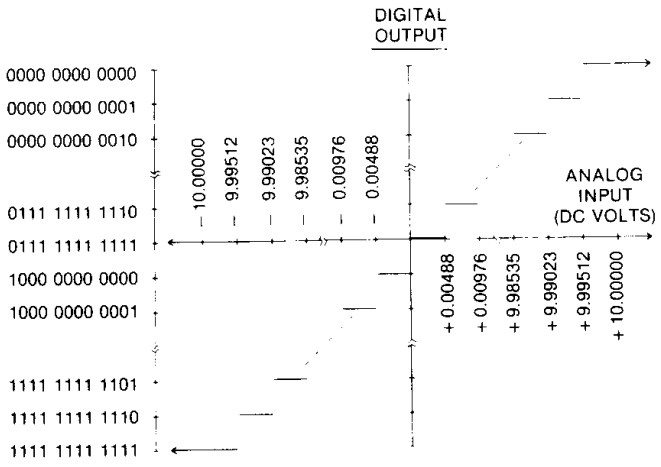
BLOCK DIAGRAM



ABSOLUTE ACCURACY ERROR

The MN7140 is a complete Data Acquisition System (DAS) including input multiplexer, instrumentation amplifier, track/hold amplifier (T/H), A/D converter, and control logic. Accuracy and linearity are specified for the complete system from analog input to digital output, eliminating the need for ordinarily important DAS component specifications such as instrumentation amp linearity, instrumentation amp gain accuracy, and T/H pedestal error.

Specifying the accuracy of the MN7140 as a system is similar to specifying the accuracy of an A/D converter. Portions of the MN7140's analog input/digital output transfer function are sketched below. Notice the quantization effect. A given digital output code is valid for a "band" or "range" of analog input voltages that theoretically, is 1 LSB wide. For the MN7140 (± 10V input range, 12 bit resolution), 1 LSB equals 4.88 mV. Ideally, any analog input between 4.88 mV and 9.76 mV should give a digital output of 0111 1111 1110. If we assign this code to the nominal midpoint of the band of input voltage for which it is valid, we can say that the 0111 1111 1110 digital output corresponds to analog inputs of +7.32 mV ±2.44 mV which can be written as +7.32 mV ± ½ LSB. The ± ½ LSB is an irreducible quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error, and its magnitude can be reduced only by going to higher resolution converters, i.e., ones that have smaller LSB's.



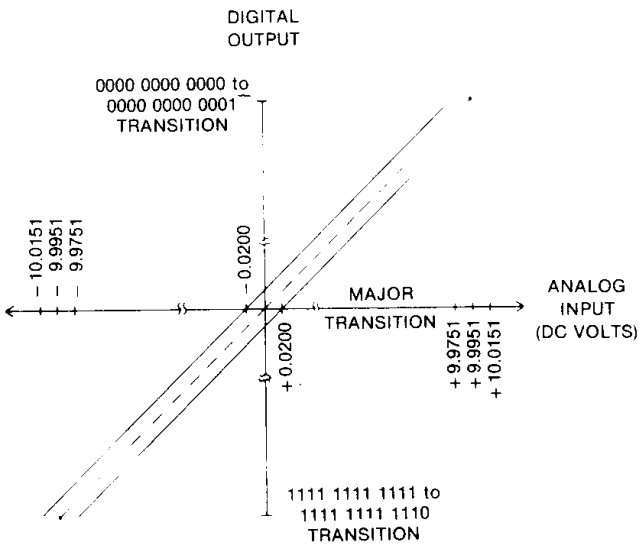
MN7140 INPUT/OUTPUT TRANSFER FUNCTION

It is difficult and time consuming to measure the center of a quantization band (the +7.32 mV in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the analog input voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted,* analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR. Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors. For the MN7140, Micro Networks tests Absolute Accuracy Error at both endpoints and the midpoint of the system transfer function.

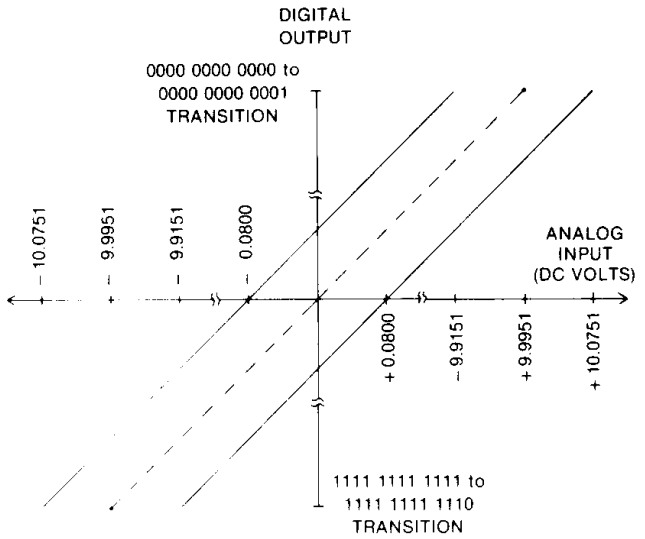
Return to the ideal analog input/digital output transfer function at the beginning of this discussion. Notice that the digital output data is supposed to change from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from −10.000V to −9.9951V. It should change from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to −9.9951V. This voltage, −9.9951V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The 1000 0000 0000 to 0111 1111 1111 transition (called the major transition because all the output bits change) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V.

For the MN7140, Micro Networks measures the three transition voltages just discussed. We perform these tests at +25°C and at 0°C and +70°C for commercial models and at −55°C and +125°C for "H" models (see Ordering Information). This testing, coupled with our linearity testing, allows us to guarantee that at +25°C, the analog input voltage at which any given digital output transition occurs will be within ±0.1%FSR (±20 mV) of its ideal value and that over the specified operating temperature range (−55°C to +125°C for "H" models), the analog input voltage at which any given digital output transition occurs will be within ±0.4%FSR (±80 mV) of its ideal value.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is represented by the broken line and the absolute accuracy limits by the solid lines. We guarantee that at +25°C, the MN7140's actual transfer function will be better than ± ½ LSB linear and that all the transition voltages will fall within the boundaries indicated. We also guarantee that at 0°C and +70°C for commercial models and at −55°C and +125°C for "H" models, the actual transfer function will be better than ±1 LSB linear, and the transition voltages will fall within the boundaries indicated.



MN7140 ABSOLUTE ACCURACY +25°C



MN7140H ABSOLUTE ACCURACY −55°C, +125°C

For temperatures intermediate to +25°C and the extremes of the specified operating temperature range, maximum Absolute Accuracy Errors can be found through interpolation. At +75°C, for example, the maximum Absolute Accuracy Error of the MN7140H will be ±0.25%FSR.

OFFSET ERROR—We have not specified an Offset Error for the MN7140. Offset Error is an Absolute Accuracy Error, and it would be redundant and potentially confusing to specify Offset Error after giving an Absolute Accuracy Error that applies over the converter's full input range.

GAIN ERROR—Gain Error is the difference between the ideal and the measured values of the DAS's Full Scale Range (minus 2 LSB's); it is a measure of the slope of the DAS's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 0000 0000 0000 to 0000 0000 0001 transition minus that measured for the 1111 1111 1111 to 1111 1111 1110 transition.

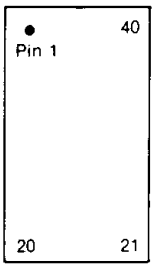
DIGITAL OUTPUT CODING

ANALOG INPUT (DC VOLTS)		DIGITAL OUTPUT
MN7143	MN7140	MSB LSB
0.0000	+10.0000	0000 0000 0000
+ 0.0024	+ 9.9951	0000 0000 000Φ*
+ 0.0049	+ 0.0098	0111 1111 11ΦΦ*
+ 4.9976	+ 0.0049	0111 1111 111Φ*
+ 5.0000	0.0000	ΦΦΦΦ ΦΦΦΦ ΦΦΦΦ*
+ 5.0024	− 0.0049	1000 0000 000Φ*
+ 9.9951	− 0.0098	1000 0000 00ΦΦ*
+ 9.9976	− 9.9951	1111 1111 111Φ*
+10.0000	−10.0000	1111 1111 1111

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the DAS continuously acquiring and converting data, the output bits indicated as Φ will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages and a sketch of the MN7140's transfer function.

The transition from output code 0000 0000 0000 to code 0000 0000 0001 will ideally occur at an input voltage of +9.9951V. Subsequently, any input voltage greater than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1110 to 1111 1111 1111 transition should occur at −9.9951 volts. An input more negative than 9.9951 volts will give all "1's".

PIN DESIGNATIONS



1	Channel 4 Input	40	Channel 3 Input
2	Channel 5 Input	39	Channel 2 Input
3	Channel 6 Input	38	Channel 1 Input
4	Channel 7 Input	37	Channel 0 Input
5	Address Output (A_1)	36	Mux Enable
6	Address Output (A_2)	35	Address Input (A_1)
7	Address Output (A_4)	34	Address Input (A_2)
8	Address Output (A_8)	33	Address Input (A_4)
9	Mux Output, Amp In (+)	32	Address Input (A_8)
10	Instr. Amp Input (−)	31	Address Mode
11	Trigger Input	30	Status Output (E.O.C.)
12	Bit 6	29	Bit 7
13	Bit 5	28	Bit 8
14	Bit 4	27	Bit 9
15	Bit 3	26	Bit 10
16	Bit 2	25	Bit 11
17	Bit 1 (MSB)	24	Bit 12 (LSB)
18	Ground	23	Logic Supply ($\pm$Vdd)
19	Offset Adjust	22	Gain Adjust
20	+15V Supply (+Vcc)	21	−15V Supply (−Vcc)

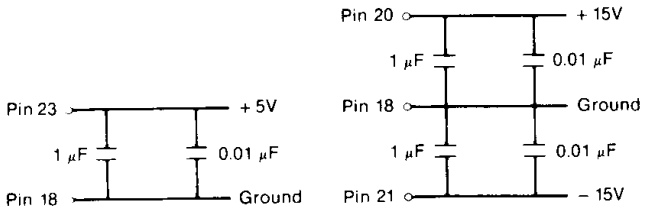
APPLICATIONS INFORMATION

The digital circuitry used in the MN7140 is CMOS. The standard precautionary measures for handling CMOS should be followed. For standard single-ended operation, Pin 10 (the minus input to the internal instrumentation amplifier) should be grounded, and Pin 36 (multiplexer enable) should be tied to a logic "1".

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN7140. The unit's GROUND (Pin 18) should be connected to system analog ground, preferably through a large ground plane underneath the package. Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Analog input runs should be well separated from digital clock lines and other noise sources. The OFFSET ADJUST point (Pin 19) is particularly noise susceptible. Care should be taken to avoid long analog runs or runs close to digital lines when utilizing this input.

When external offset adjustment is employed (see page 7), the 3.3 megohm resistor and trimpot should be located as close to the package as possible. Whether or not external gain adjustment is used (see page 7), a 0.01 μF ceramic bypass capacitor should be located close to the package connecting the GAIN ADJUST point (Pin 22) to analog ground.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the MN7140. For optimum performance and noise rejection, 1 μF capacitors paralleled with 0.01 μF ceramic capacitors should be used as shown in the diagram below.



POWER SUPPLY DECOUPLING

SUMMARY OF OPERATION—The rising edge of a TRIGGER pulse loads the multiplexer (Mux) channel address and initiates a data acquisition and conversion cycle. If sequential addressing is being used (see below), the next channel will be accessed. If random addressing is being used, the channel whose address has been applied to the CHANNEL ADDRESS INPUTS will be accessed. The rising edge of the TRIGGER pulse simultaneously fires an internal one-shot (10 μSec pulse duration) whose output disables the internal clock. 10 μSec later, the falling edge of the one-shot drives the track/hold amp (T/H) into the hold mode, gates on the clock, generates a start convert signal for the 12 bit A/D converter, and drives the STATUS OUTPUT to a logic "1". Gating off the clock during the time the Mux is settling into its new channel and the T/H is acquiring a new signal reduces noise errors. When the conversion is complete (approximately 20 μSec later), the STATUS output returns to a logic "0" indicating that the conversion is complete, that the digital output is valid, and that the T/H amplifier has returned to the tracking mode. The unit is now ready to be triggered for the acquisition and conversion of the next channel.

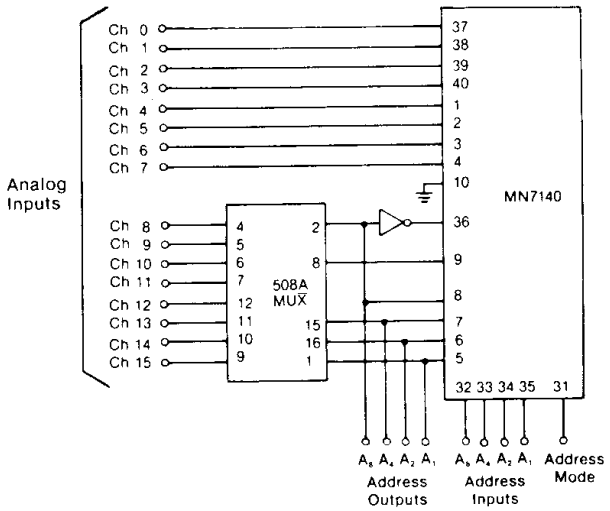
ADDRESSING—The MN7140's input channels may be randomly or sequentially addressed. For random addressing, the ADDRESS MODE input (Pin 31) must be tied to a logic "0" and the desired channel address (in 8421 binary) applied to the CHANNEL ADDRESS INPUTS (Pins 32-35). In this addressing mode, the MN7140's internal address latch/counter acts as a 4 bit parallel register. The rising edge of the TRIGGER pulse latches the new channel address and initiates the data acquisition and conversion cycle. If the MN7140 is not being expanded (see below) and only its 8 internal channels are being used, the A_8 address bit (Pin 32) is unnecessary, and this input can be tied either high or low but should not be left open.

For sequential addressing, the ADDRESS MODE input (Pin 31) must be tied to a logic "1". In this mode, the internal address latch/counter acts as a 4 bit binary counter. Each rising edge of the TRIGGER input will increment the channel address and initiate the data acquisition and conversion cycle. Channel 0000 will be accessed after channel 1111. As one changes from random to sequential addressing, the next channel accessed will be one higher than the channel last randomly addressed. Changing digital data appearing at the ADDRESS INPUTS will not affect the MN7140 when it is in the sequential addressing mode.

SEQUENTIAL ADDRESSING CONTINUOUS CONVERSIONS—The MN7140 can be made to continuously sequence through channels acquiring and converting data by applying a logic "1" to the ADDRESS MODE input (Pin 31) and inverting the STATUS output (Pin 30) and tying it back to the TRIGGER INPUT (Pin 11). In this mode, the STATUS OUTPUT going low at the end of a conversion becomes the rising TRIGGER edge that addresses the next channel and initiates the next data acquisition and conversion cycle. After each channel has been converted and the STATUS has dropped to a "0", the output data will be valid for approximately the next 10 μSec while the multiplexer is switching channels and the T/H is acquiring the new signal. The falling edge of STATUS may be used to latch output data into an external receiving register (please read the section describing the STATUS output). When continuously converting, an external TRIGGER signal should be provided at power-on to avoid possible latch-up.

CHANNEL ADDRESS OUTPUTS—The MN7140's CHANNEL ADDRESS OUTPUTS (Pins 5-8) are tied directly to the unit's internal address counter/latch. They indicate, in 8421 binary, the multiplexer channel presently being accessed. When using external multiplexers for differential or expanded single-ended operation (see below), these outputs can be used to address the external multiplexers, eliminating the need for any additional address decoding circuitry. When using sequential addressing, the appropriate CHANNEL ADDRESS OUTPUTS can be NORed together to generate a frame sync pulse each time channel 7 (8 channel systems) or channel 15 (16 channel systems) is being addressed. In microprocessor-based systems, the ADDRESS OUTPUTS can be 3-state buffered to add channel read-back capability.

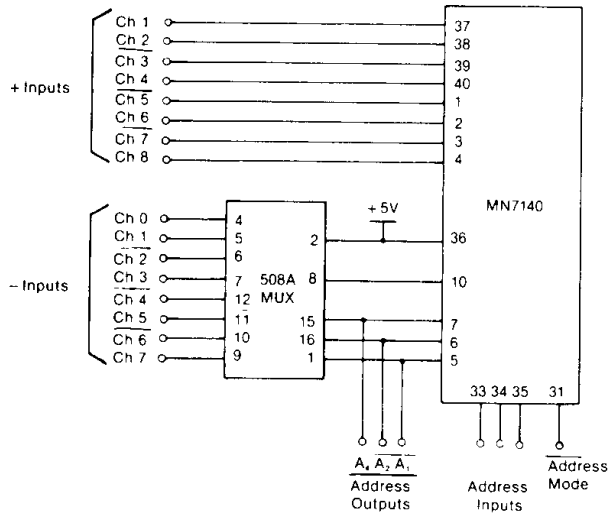
CHANNEL EXPANSION—The MN7140's input capabilities can be expanded beyond the 8 basic channels with the addition of external analog multiplexers. The diagram below shows a 16 channel single-ended system using an external 508A type multiplexer. Note that no additional address



16 SINGLE-ENDED INPUT CHANNELS

decoding circuitry is necessary. The MN7140's internal address latch/counter (see above) is a 4 bit unit that can be used to either randomly or sequentially address up to 16 channels. For further expansion, additional mux's can be tied to Pin 9 (the noninverting input to the internal instrumentation amplifier) or cascaded in front of the MN7140's internal mux. Remember that for single-ended operation, Pin 10 (the minus input to the internal instrumentation amplifier) has to be grounded.

DIFFERENTIAL INPUT OPERATION—The MN7140 can be configured for 8 differential input channels with the addition of a single external multiplexer. A system using a 508A type multiplexer is shown below. No additional address decoding circuitry is necessary. Further expansion is possible with additional mux's tied to Pins 9 and 10 (the inputs to the internal instrumentation amplifier).



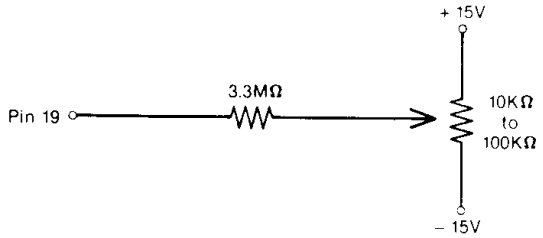
8 DIFFERENTIAL INPUT CHANNELS

PIN 36 MULTIPLEXER ENABLE—When Pin 36 has a logic "0" applied, the MN7140's internal mux is disabled. When Pin 36 has a logic "1" applied, the internal mux is enabled and can be accessed through ADDRESS INPUTS A_1, A_2, and A_4 (Pins 33-35).

STATUS OUTPUT (E.O.C.)—The STATUS or END OF CONVERSION (E.O.C.) output (Pin 30) indicates whether the MN7140 is tracking or converting an input signal. When STATUS is a logic "0", the MN7140's internal T/H amplifier is in the tracking mode and digital output data from the previous conversion is still valid. When the STATUS is a logic "1", the T/H is in the hold mode, and the internal A/D is converting. The output data is not valid. The falling edge of STATUS indicates that the conversion is complete, that the output data is valid, and that the T/H has returned to the tracking mode. Output data will be valid and enabled a minimum of 300 nsec before STATUS returns low.

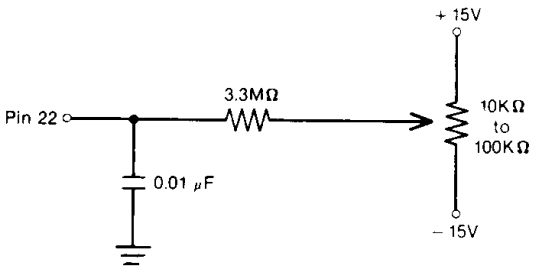
OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The MN7140 will operate as specified without additional adjustments. If desired, however, Absolute Accuracy Error can be reduced to ± 1 LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the Offset Adjustment must be made before the Gain Adjustment. Multiturn potentiometers with TCR'S of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ± 20% carbon composition or better. If these adjustments are not used, Pins 19 and 22 should be left open. Do not ground.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown, and apply an analog input voltage of −9.9951V. With the MN7140 performing repeated conversions, adjust the offset potentiometer down until all the output bits are "1". Then adjust up until the LSB just turns to a "0".



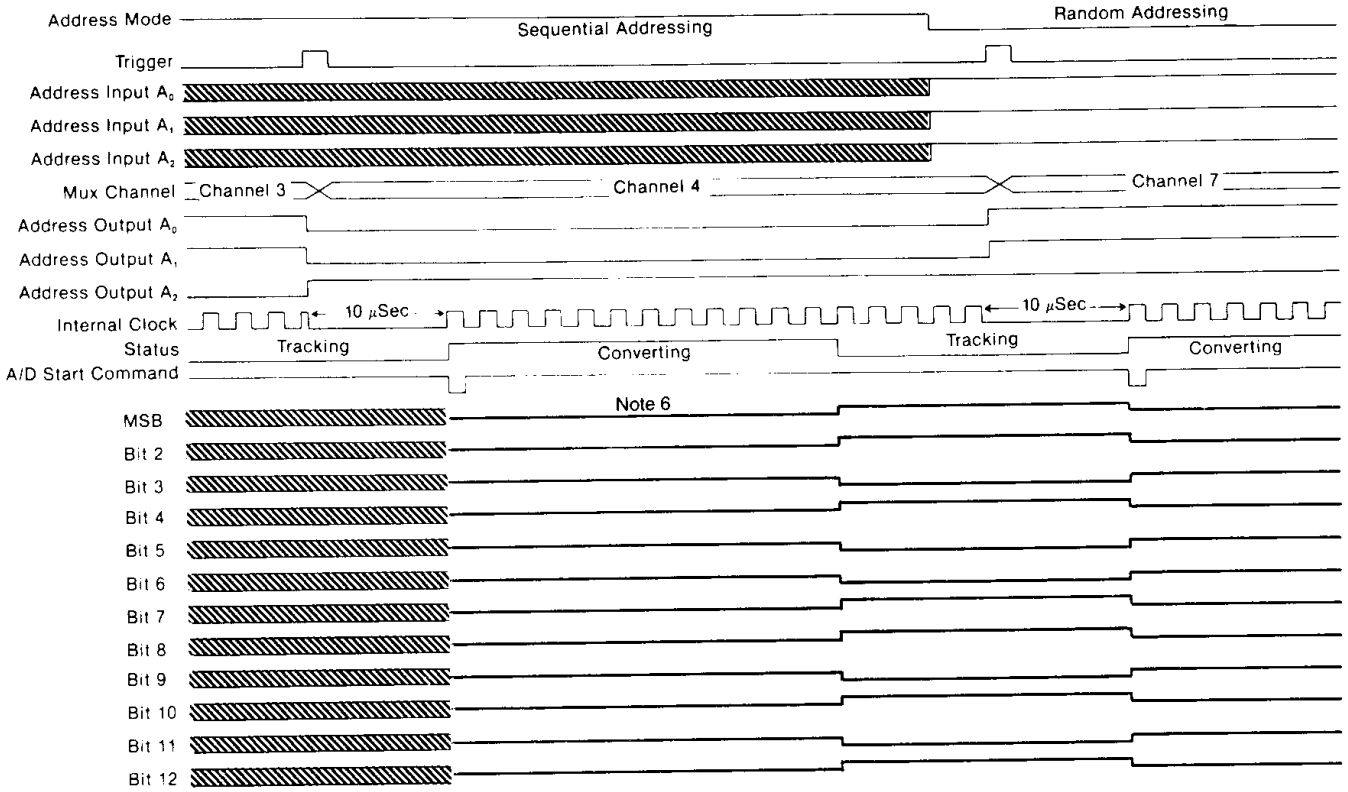
OFFSET ADJUSTMENT

GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply an analog input voltage of + 9.9951V. With the MN7140 performing repeated conversions, adjust the gain potentiometer up until all the output bits are "0". Then adjust down until the LSB just turns to a "1".



GAIN ADJUSTMENT

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. For sequential addressing, set ADDRESS MODE = "1". For random addressing, set ADDRESS MODE = "0".
2. The minimum TRIGGER pulse width is 240 nSec, but the TRIGGER does not have to be brought back down for the acquisition and conversion cycle to continue.
3. In the random addressing mode, ADDRESS INPUT data must be valid at least 300 nSec prior to TRIGGER.
4. The rising edge of TRIGGER disables the internal clock for 10 μSec during signal acquisition.
5. When STATUS = "1" the internal T/H is in the hold mode, and the A/D converter is performing a conversion. When STATUS = "0", the conversion is complete; output data is valid; and the T/H has returned to the track mode.
6. All output bits are 3-stated during the A/D conversion. They become valid and enabled a minimum of 300nsec before STATUS returns low.
7. Operation shown is for the digital word 1101 0011 0101 which corresponds to an analog input of −6.5137V.
8. Conversion time is defined as the time the STATUS output is high.
9. Once an acquisition and conversion cycle has begun, it cannot be stopped by applying another TRIGGER pulse.
10. When the system is initially "powered up", it may come on at any point in the cycle.