MN838898

1. Type

CMOS LSI source driver for color TFT LCD panels

2. Overview

This LSI converts the digital display data from a personal computer, portable device, or other source into analog signals for driving a color TFT LCD panel.

3. Features

(1) Power saving driver
(2) Built in DA converter accepting 6-bit digital input (for 262,144 colors)
(3) Choice of 360 and 324 drive outputs
(4) Input data bus at pixel level
(5) Choice of output data format: gray scale or binary
(6) Eleven reference voltage inputs for producing 10 segment gamma adjustment graph.
(7) Set output voltage inflection points at data values 00, 01, 07, 0F, 17, 1F, 27, 2F, 37, 3E, and 3F.
(8) Prechargeless drive circuits
(9) Support for serial cascade connections
(10) Automatic internal clock stop after fixed number of data inputs
(11) Choice of shift register shift direction: right or left
(12) Gray scale data inversion available every clock cycle
(13) Low voltage operation: 2.5 V (typ.) for logic circuits; 3.5 V (typ.) for analog circuits
(14) Maximum operating clock frequency: 15 MHz
(15) Power save function for cutting off current to outputs, fixing them at high impedance

4. Internal Block Diagram

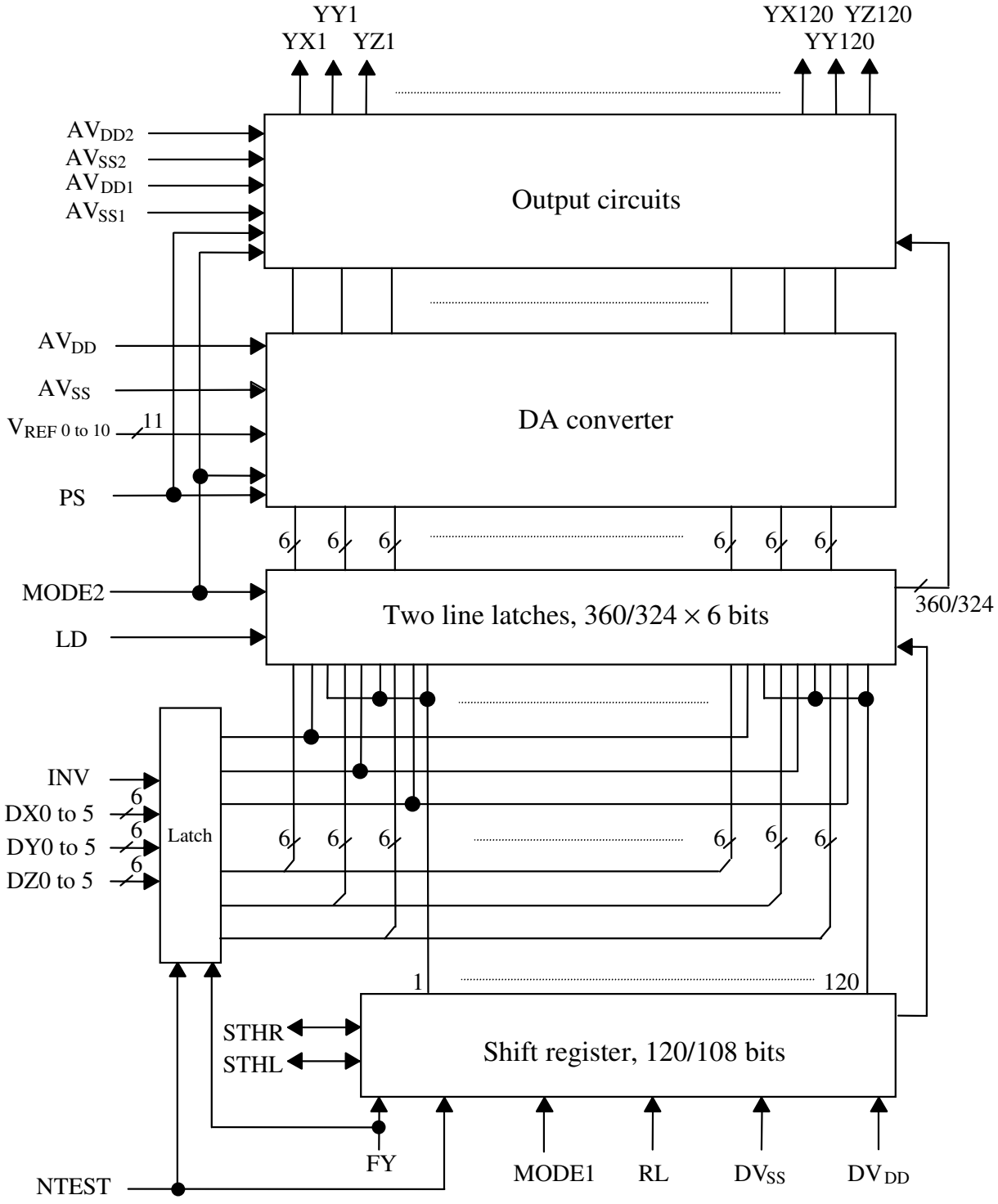


Figure 4.1 Block Diagram

5. Pin Descriptions

Table 5.1 Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O Direction</th><th>Pin Function</th><th>Description</th></tr>
<tr><td rowspan="2">DX0 to 5,
DY0 to 5,
DZ0 to 5</td><td rowspan="2">Input</td><td>Gray scale digital data input pins</td><td>Input pins for gray scale (MODE2 = Low) digital data, 6 bits each for R, G, and B.
DX5, DY5, and DZ5 represent the MSB;
DX0, DY0, and DZ0, the LSB.</td></tr>
<tr><td>Binary digital data input pins
(DX5, DY5, and DZ5)</td><td>Input pins for binary (MODE2 = High) digital data, 1 bit each for R, G, and B.
Always drive the unused pins
(DX4 to DX0, DY4 to DY0, and DZ4 to DZ0)
at either High or Low level.</td></tr>
<tr><td>YX1 to 120,
YY1 to 120,
YZ1 to 120</td><td>Output</td><td>Analog image output pins</td><td>These signals drive the LCD panel.</td></tr>
<tr><td>STH R, STHL</td><td>I/O</td><td>Start pulse I/O pins</td><td>These I/O pins are for the internal shift register's start pulses.
The following table indicates data shift direction by start pulses during face up.
<table>
<tr><th></th><th>RL=H</th><th>RL=L</th></tr>
<tr><td>STHR</td><td>Right shift input</td><td>Left shift output</td></tr>
<tr><td>STHL</td><td>Right shift output</td><td>Left shift input</td></tr>
</table></td></tr>
<tr><td>RL</td><td>Input</td><td>Shift direction input pin</td><td>This specifies the shift direction: High level for right;
Low level for left.
H: Right shift input (YX,YY,YZ1 → 120)
L: Left shift input (YX,YY,YZ120 → 1)</td></tr>
<tr><td>FY</td><td>Input</td><td>Shift clock input pin</td><td>This accepts the transfer clock for the shift register</td></tr>
<tr><td>LD</td><td>Input</td><td>Data load input pin</td><td>High level input enables transfer, synchronized with rising edges in the FY signal, of the LCD drive data from the built-in DA converter.</td></tr>
<tr><td>INV</td><td>Input</td><td>Data inversion control input pin</td><td>The data logic when the INV input is at Low level is AVDD for Low level and AVSS for High level. Driving INV at High level reverses the data logic.</td></tr>
<tr><td>MODE1</td><td>Input</td><td>Number of drive outputs select pin</td><td>This specifies the number of LCD panel drive outputs:
High level for 360, Low level for 324, disabling
YX55 to YX66, YY55 to YY66, and YZ55 to YZ66.
(For further details, see Section 6.1 "Functional Description.")</td></tr>
<tr><td>MODE2</td><td>Input</td><td>Input format select pin</td><td>This specifies the data input format: gray scale or binary.
High level: Binary. DX5, DY5, and DZ5 only. The DA converter is off.
Low level: Gray scale. DX, DY, and DZ5 to DZ0. The DA converter is on.</td></tr>
<tr><td>PS</td><td>Input</td><td>Power save function select pin</td><td>High level input at a rising edge in the FY signal cuts off current to outputs, fixing them at high-impedance.
High level: High-impedance outputs. No current to operational amplifier or other components.
Low level: Normal operation</td></tr>
<tr><td>NTEST</td><td>Input</td><td>Test input pin
(with built-in pull-up resistance)</td><td>Normally fix this input at High level.
High level: Normal operation
Low level: Test mode</td></tr>
<tr><td>$VREF_{0\ to\ 10}$</td><td>Input</td><td>Gamma adjustment potential input pin</td><td>This input is the gamma adjustment potential input pin for the DA converter.</td></tr>
<tr><td>AV_{DD}, AV_{SS}</td><td>Input</td><td>Analog power supply</td><td>This is the power supply for the DA converter's analog circuits.</td></tr>
<tr><td>AV_{DD1}, AV_{SS1}</td><td>Input</td><td>Analog power supply</td><td>This is the power supply for the output analog circuits.</td></tr>
<tr><td>AV_{DD2}, AV_{SS2}</td><td>Input</td><td>Analog power supply</td><td>This is the power supply for the circuits protecting the output circuits.</td></tr>
<tr><td>DV_{DD}, DV_{SS}</td><td>Input</td><td>Digital power supply</td><td>This is the power supply for the digital circuits.</td></tr>
</table>

6. Description of Operation

6.1 Functional Description

The MODE2 pin offers a choice of 6-bit gray scale data or 1-bit binary data. The MODE1 pin specifies the number of outputs.

The following Table summarizes the effects of MODE1 and MODE2, and RL input levels on I/O.

Table 6.1 MODE1 and MODE2, and RL Settings

MODE1	MODE2	RL	Input pins	Data transfer direction	Data Output format
				FX : 1 - 2 - 3 - ··· - 54 - 55 - ··· - 118 - 119 - 120	
High level (360 Outputs)	Low level (gray scale input)	H	DX0 - 5	YX1 - YX2 - YX3 - ··· - YX54 - YX55 - ··· - YX118 - YX119 - YX120	64-level analog outputs
			DY0 - 5	YY1 - YY2 - YY3 - ··· - YY54 - YY55 - ··· - YY118 - YY119 - YY120	
			DZ0 - 5	YZ1 - YZ2 - YZ3 - ··· - YZ54 - YZ55 - ··· - YZ118 - YZ119 - YZ120	
		L	DX0 - 5	YX120 - YX119 - YX118 - ··· - YX67 - YX66 - ··· - YX1 - YX2 - YX3	
			DY0 - 5	YY120 - YY119 - YY118 - ··· - YY67 - YY66 - ··· - YY1 - YY2 - YY3	
			DZ0 - 5	YZ120 - YZ119 - YZ118 - ··· - YZ67 - YZ66 - ··· - YZ1 - YZ2 - YZ3	
	High level (binary input)	H	DX5	YX1 - YX2 - YX3 - ··· - YX54 - YX55 - ··· - YX118 - YX119 - YX120	Binary digital outputs
			DY5	YY1 - YY2 - YY3 - ··· - YY54 - YY55 - ··· - YY118 - YY119 - YY120	
			DZ5	YZ1 - YZ2 - YZ3 - ··· - YZ54 - YZ55 - ··· - YZ118 - YZ119 - YZ120	
		L	DX5	YX120 - YX119 - YX118 - ··· - YX67 - YX66 - ··· - YX1 - YX2 - YX3	
			DY5	YY120 - YY119 - YY118 - ··· - YY67 - YY66 - ··· - YY1 - YY2 - YY3	
			DZ5	YZ120 - YZ119 - YZ118 - ··· - YZ67 - YZ66 - ··· - YZ1 - YZ2 - YZ3	
				FX : 1 - 2 - 3 - ··· - 54 - 55 - ··· - 106 - 107 - 108	
Low level (324 Outputs)	Low level (gray scale input)	H	DX0 - 5	YX1 - YX2 - YX3 - ··· - YX54 - YX67 - ··· - YX118 - YX119 - YX120	64-level analog outputs
			DY0 - 5	YY1 - YY2 - YY3 - ··· - YY54 - YY67 - ··· - YY118 - YY119 - YY120	
			DZ0 - 5	YZ1 - YZ2 - YZ3 - ··· - YZ54 - YZ67 - ··· - YZ118 - YZ119 - YZ120	
		L	DX0 - 5	YX120 - YX119 - YX118 - ··· - YX67 - YX54 - ··· - YX1 - YX2 - YX3	
			DY0 - 5	YY120 - YY119 - YY118 - ··· - YY67 - YY54 - ··· - YY1 - YY2 - YY3	
			DZ0 - 5	YZ120 - YZ119 - YZ118 - ··· - YZ67 - YZ54 - ··· - YZ1 - YZ2 - YZ3	
	High level (binary input)	H	DX5	YX1 - YX2 - YX3 - ··· - YX54 - YX67 - ··· - YX118 - YX119 - YX120	Binary digital outputs
			DY5	YY1 - YY2 - YY3 - ··· - YY54 - YY67 - ··· - YY118 - YY119 - YY120	
			DZ5	YZ1 - YZ2 - YZ3 - ··· - YZ54 - YZ67 - ··· - YZ118 - YZ119 - YZ120	
		L	DX5	YX120 - YX119 - YX118 - ··· - YX67 - YX54 - ··· - YX1 - YX2 - YX3	
			DY5	YY120 - YY119 - YY118 - ··· - YY67 - YY54 - ··· - YY1 - YY2 - YY3	
			DZ5	YZ120 - YZ119 - YZ118 - ··· - YZ67 - YZ54 - ··· - YZ1 - YZ2 - YZ3	

MODE1 = Low (324 outputs) produces invalid output from YX55 - YX66, YY55 - YY66, and YZ55 - YZ66.

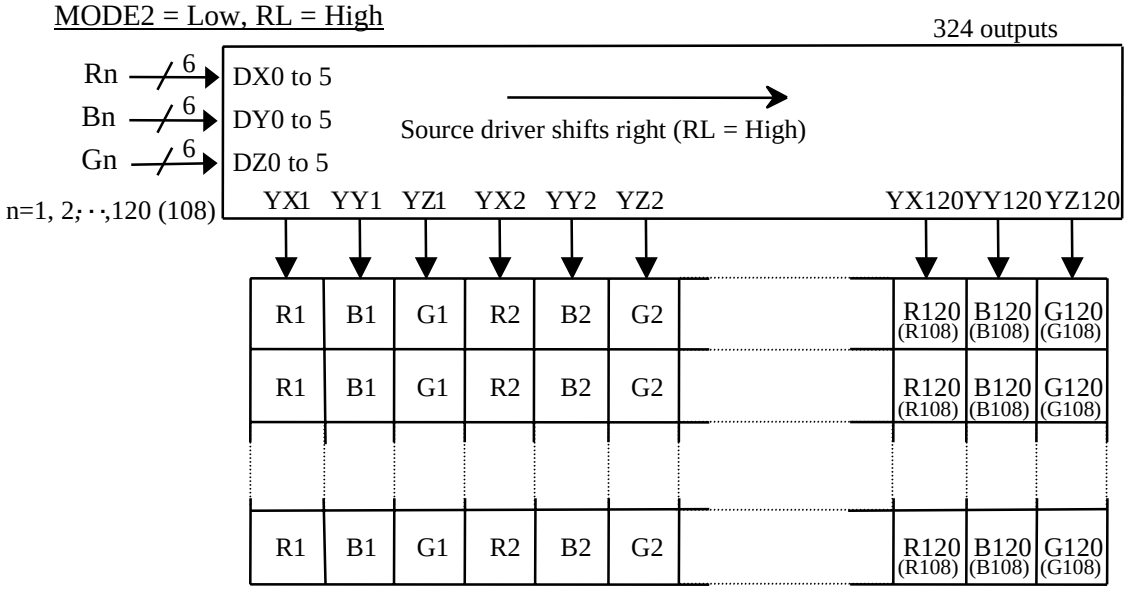
6.2 Relationships Between Data Input and Output Pins

(1) Gray scale data input (MODE2 = Low)

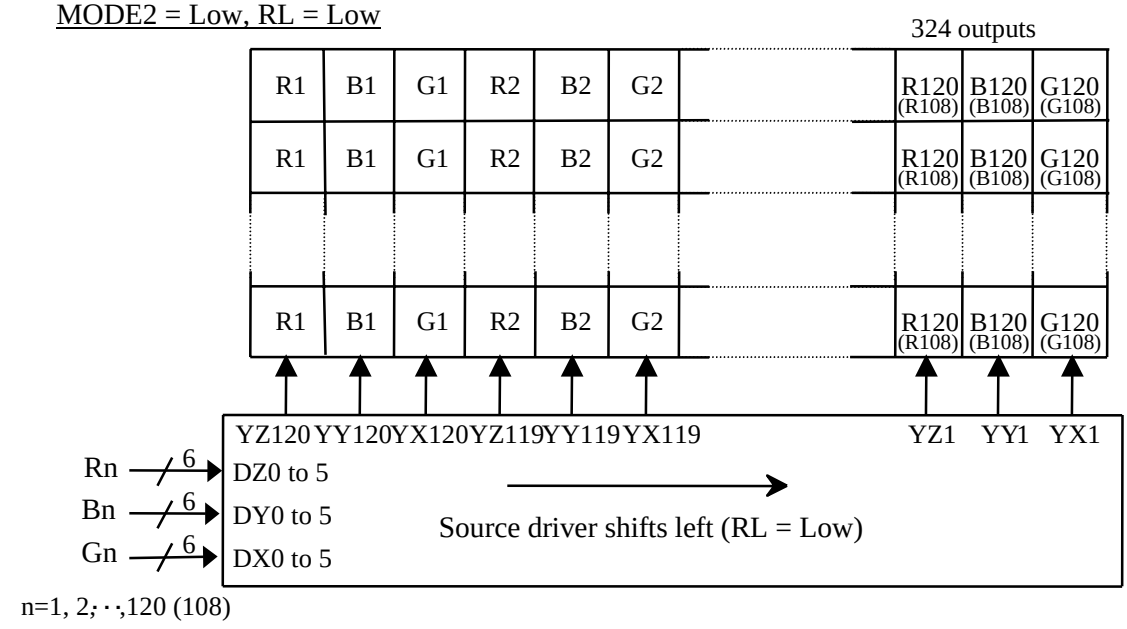
The following summarizes the relationships between data input and output pins for gray scale data input (MODE2 = Low).

So, binary data input is naturally ignored during gray scale data input.

MODE2 = Low, RL = High



MODE2 = Low, RL = Low



(2) Binary input (MODE2 = High)

Binary input uses only the pins DX5, DY5, and DZ5. The relationships between data input and output pins are otherwise the same.

So, binary data input is naturally ignored during gray scale data input.

6.3 Power Save Function

This signal can be switched anywhere except the latch signal, rising edges in the FY signal.

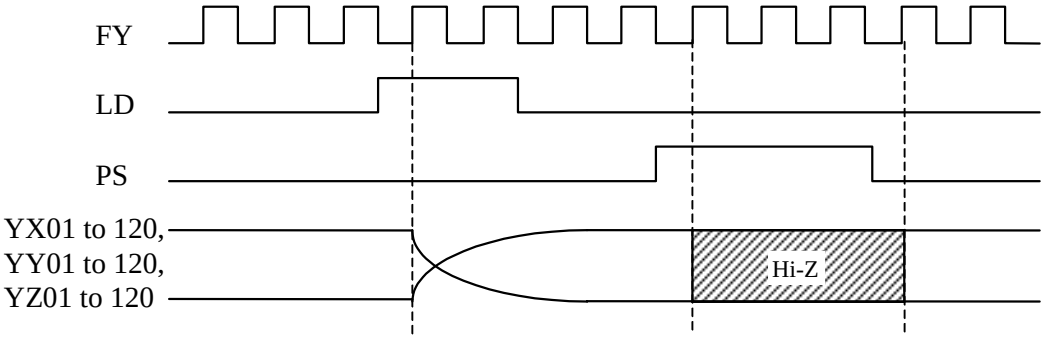


Figure 6.3 High-Impedance Output Interval

6.4 Blanking Interval

The following timing chart summarizes the relationships between the load data (LD) and start pulse (STHR and STHL) inputs and the blanking interval.

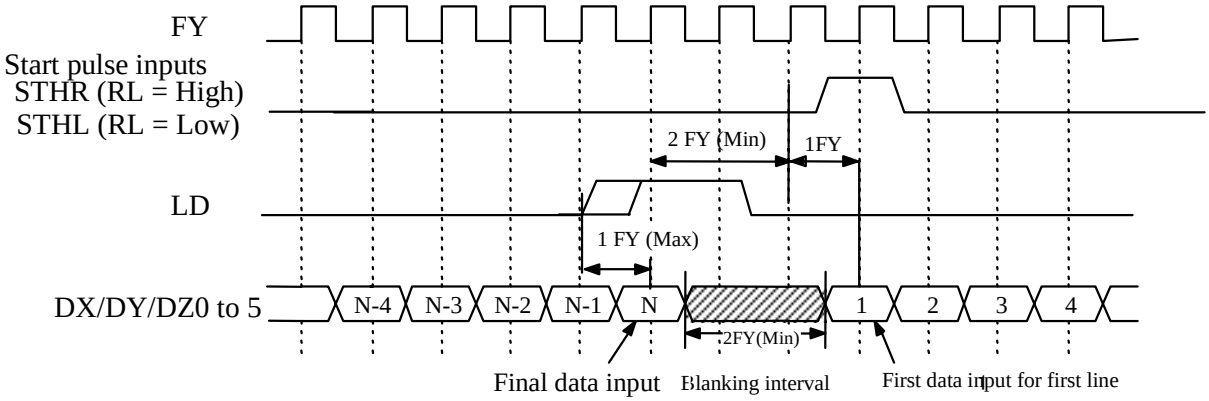


Figure 6.4 Blanking Interval

6.5 Data Inverse Function

Driving the INV input at High level inverts all bits in the data input.

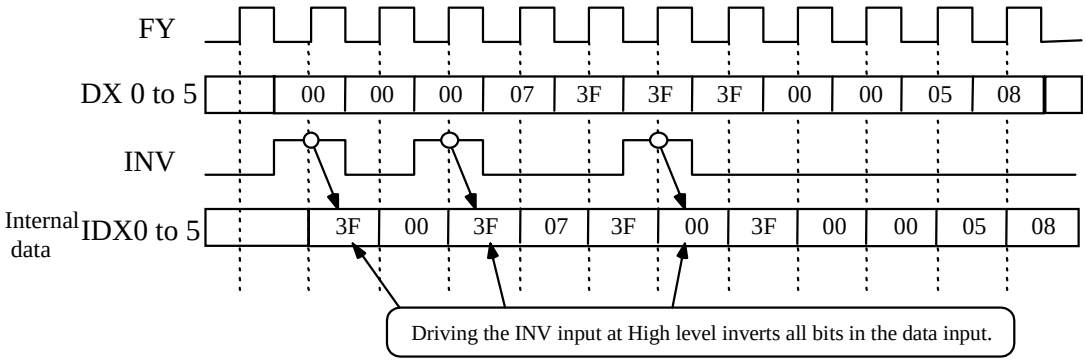


Figure 6.5 Data Inverse Function

6.6 Switching Input Formats

The following timing chart summarizes the relationships between changes in input format and the subsequent changes in output.

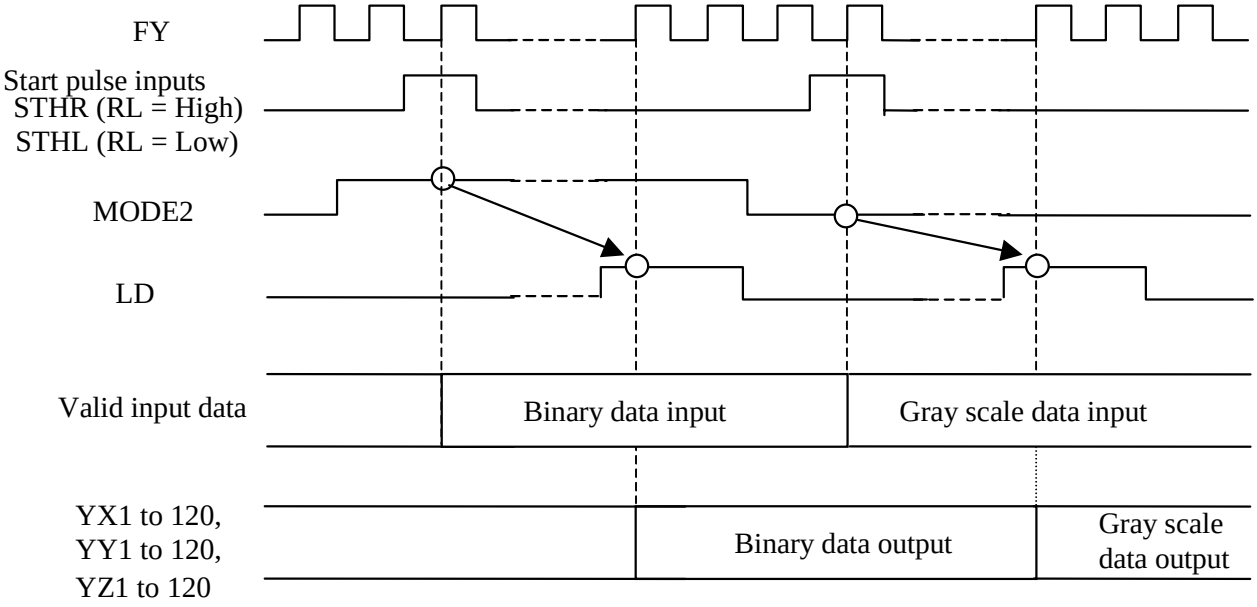


Figure 6.6.1 Switching Formats (1/2)

The LSI drives the output pins at high-impedance for one FY cycle when changing output formats.

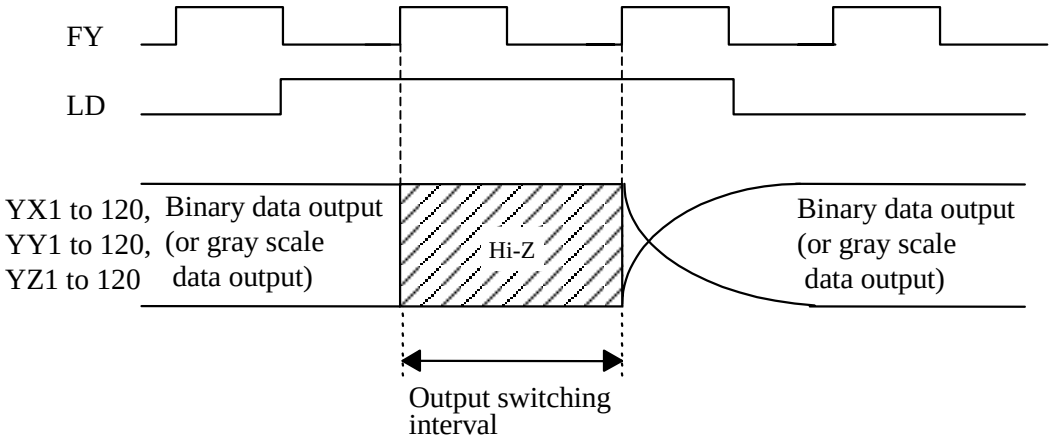


Figure 6.6.2 Switching Formats (2/2)

6.7 Cascade Connection

(1) RL = High

Driver A starts latching data one FY cycle after receiving a start pulse (STHR).
It asserts the carry signal (STHL) one FY cycle before latching the last data and then stopping.

MODE1 = High (360 outputs): 119 FY cycles
MODE1 = Low (324 outputs): 107 FY cycles

Cascade Connection

Driver B starts latching data one FY cycle after receiving the carry signal (STHL) from driver A.

Note: Although the carry signal (STHL) pulses are two FY cycles long, only the first cycle counts. The next driver treats the two cycles as a single pulse.

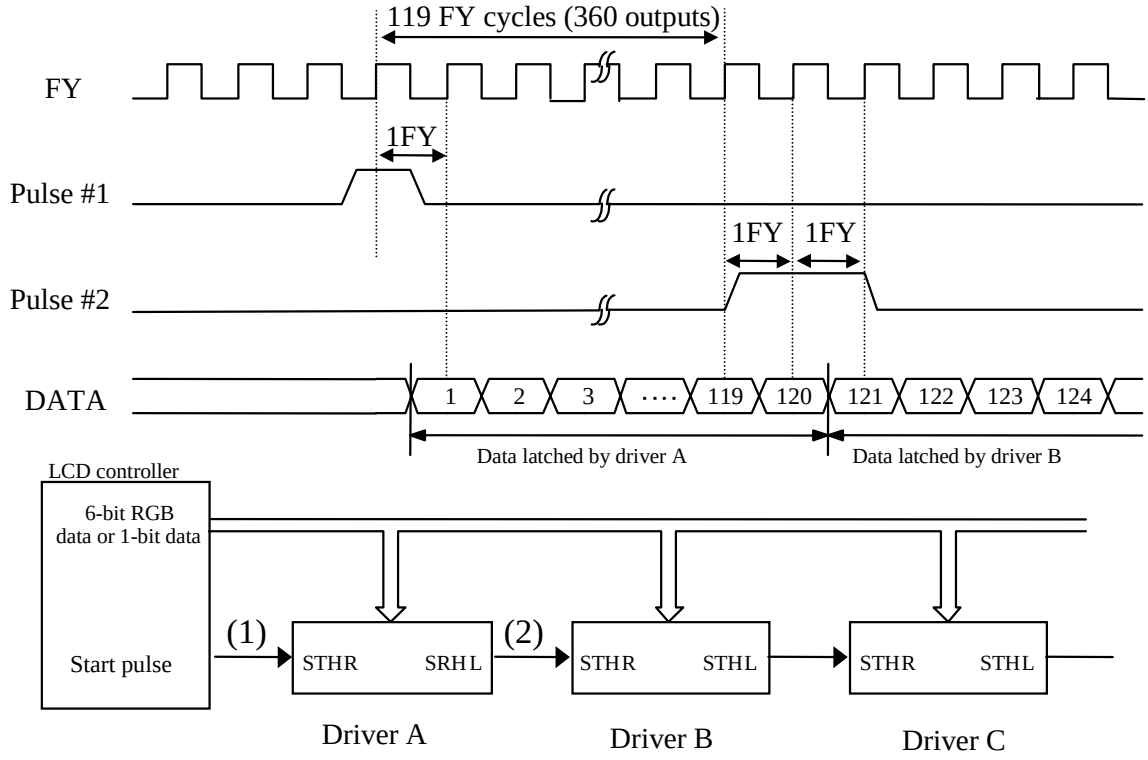


Figure 6.7 Serial Cascade Connection

(2) RL = Low

The start pulse input is from STHL; the carry output, from STHR. Apart from that, operation is the same as for RL = High.

6.8 Relationship between Input Data and Output Voltage

6.8.1 Built-In Gamma Adjustment Resistors

The output voltage depends on the input data and thirteen gamma adjustment voltages ($V_{REF\,x}$, x = H, 0 to 10, L). See graph and conversion table on the next two pages.

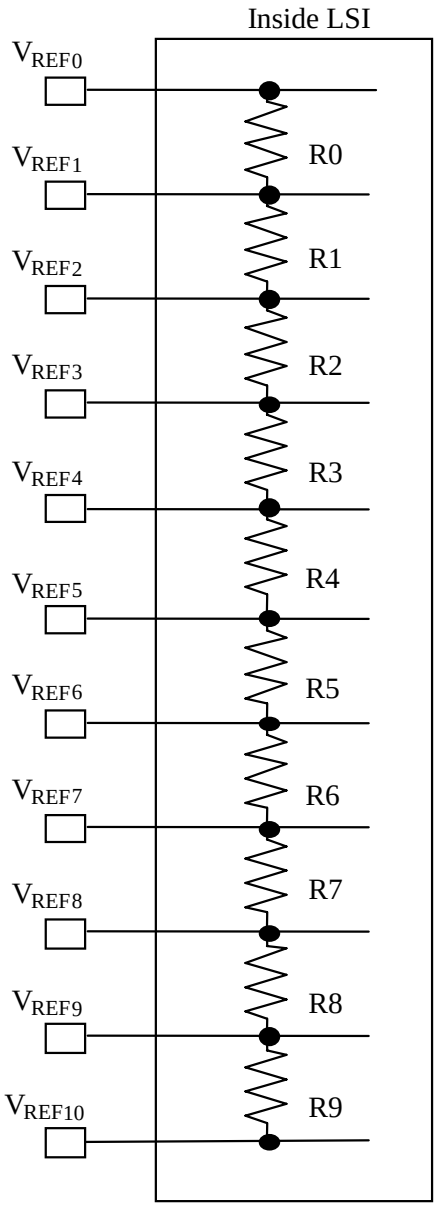


Figure 6.8.1
Built-In Gamma Adjustment Resistors

The LSI contains ten divider resistances and two switches between V_{REGF0} and V_{REGF10}. Table 6.8 summarizes the formulas for calculating the output voltages from the voltages applied to pins $V_{REF\,x}$, x = 0 to 10. Applying voltages only to V_{REF0} and V_{REF10} produces the default graph shown in Figure 6.8.2.

Note that we recommend the use of an operational amplifier or similar means to guarantee low-impedance input to the V_{REF} pins.

Direct input sometimes fails to produce the desired output voltages.

(Note 1)

The adjustment voltages ($V_{REF\,x}$, x = H, 0 to 10) must satisfy one of the following two relationships.

$$AV_{DD} > V_{REF0} \geq V_{REF1} \geq V_{REF2} \geq \cdots\cdots \geq V_{REF9} \geq V_{REFL10} > AV_{SS}$$

or

$$AV_{DD} > V_{REF10} \geq V_{REF9} \geq V_{REF8} \geq \cdots\cdots \geq V_{REF1} \geq V_{REF0} > AV_{SS}$$

Do not change these voltages while the chip is in operation.

The following are the values for the internal resistances R0 to R9 for R2=1.0.

Gamma Adjustment Resistances

R0	1.15
R1	1.09
R2	1.00
R3	1.00
R4	1.00
R5	1.00
R6	1.00
R7	1.00
R8	1.09
R9	1.15

6.8.2 Relationship between Input Data and Output Voltage

The following Figure gives the gamma adjustment curve for INV = Low.

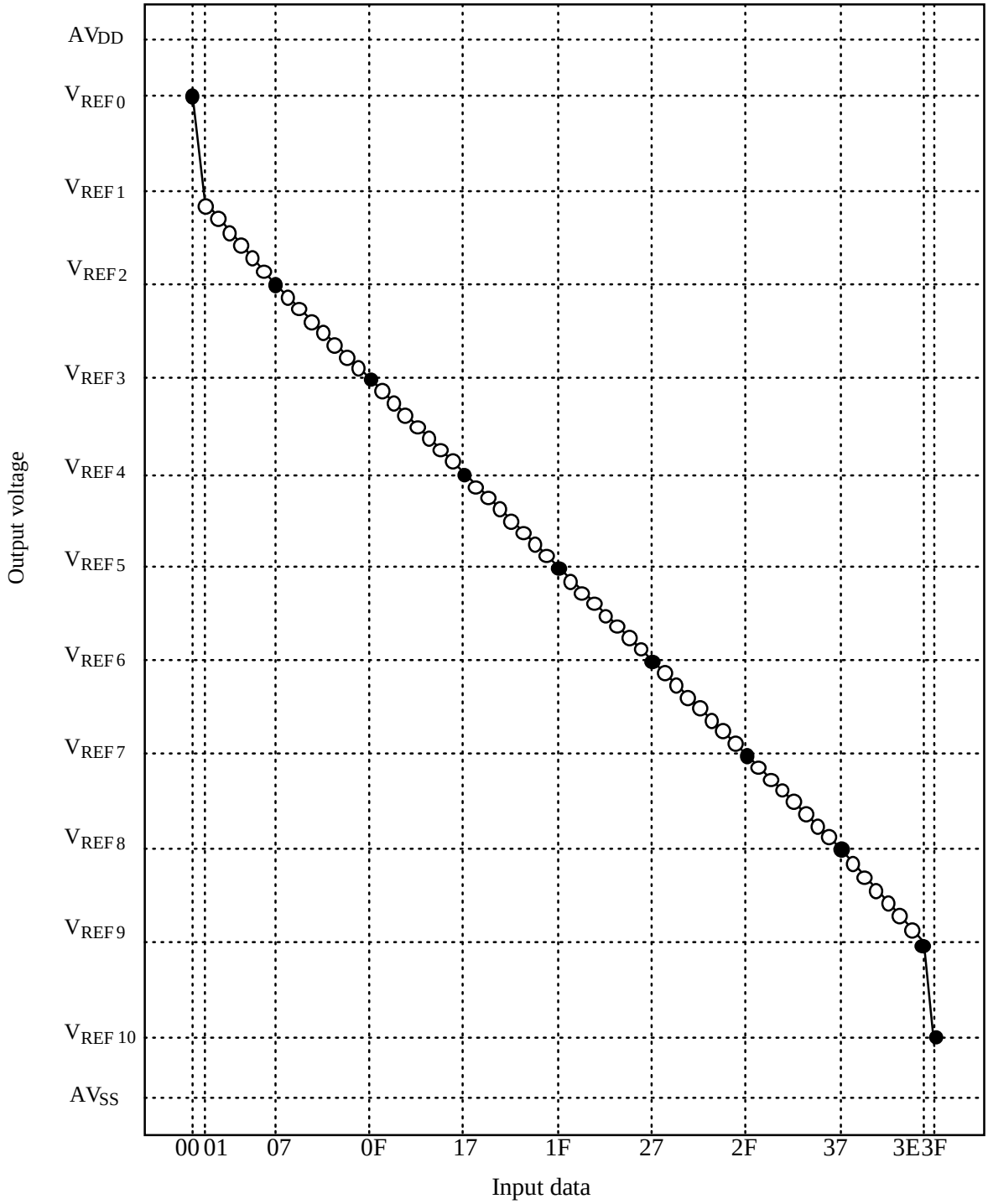


Figure 6.8.2 Relationship between Input Data and Output Voltage

($AV_{DD} > V_{REF0} \geq V_{REF1} \geq V_{REF2} \geq \ldots\ldots \geq V_{REF9} \geq V_{REF10} > AV_{SS}$)

6.8.3 Relationship between Reference Voltages and Output Voltages

The following Table gives the formulas for converting input data for INV = Low.

Table 6.8 Relationship between Reference Voltages and Output Voltages

($AV_{DD} > V_{REF0} \geq V_{REF1} \geq V_{REF2} \geq \ldots \ldots \geq V_{REF9} \geq V_{REF10} > AV_{SS}$)

Input data	Formula for calculating output voltage	Input data	Formula for calculating output voltage
00h	V_{REF0}	20h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 7/8$
01h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 6/7$	21h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 6/8$
02h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 5/7$	22h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 5/8$
03h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 4/7$	23h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 4/8$
04h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 3/7$	24h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 3/8$
05h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 2/7$	25h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 2/8$
06h	$V_{REF2} + (V_{REF1}$ to $V_{REF2}) \times 1/7$	26h	$V_{REF6} + (V_{REF5}$ to $V_{REF6}) \times 1/8$
07h	V_{REF2}	27h	V_{REF6}
08h	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 7/8$	28h	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 7/8$
09h	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 6/8$	29h	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 6/8$
0Ah	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 5/8$	2Ah	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 5/8$
0Bh	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 4/8$	2Bh	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 4/8$
0Ch	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 3/8$	2Ch	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 3/8$
0Dh	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 2/8$	2Dh	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 2/8$
0Eh	$V_{REF3} + (V_{REF2}$ to $V_{REF3}) \times 1/8$	2Eh	$V_{REF7} + (V_{REF6}$ to $V_{REF7}) \times 1/8$
0Fh	V_{REF3}	2Fh	V_{REF7}
10h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 7/8$	30h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 7/8$
11h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 6/8$	31h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 6/8$
12h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 5/8$	32h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 5/8$
13h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 4/8$	33h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 4/8$
14h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 3/8$	34h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 3/8$
15h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 2/8$	35h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 2/8$
16h	$V_{REF4} + (V_{REF3}$ to $V_{REF4}) \times 1/8$	36h	$V_{REF8} + (V_{REF7}$ to $V_{REF8}) \times 1/8$
17h	V_{REF4}	37h	V_{REF8}
18h	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 7/8$	38h	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 6/7$
19h	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 6/8$	39h	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 5/7$
1Ah	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 5/8$	3Ah	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 4/7$
1Bh	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 4/8$	3Bh	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 3/7$
1Ch	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 3/8$	3Ch	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 2/7$
1Dh	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 2/8$	3Dh	$V_{REF9} + (V_{REF8}$ to $V_{REF9}) \times 1/7$
1Eh	$V_{REF5} + (V_{REF4}$ to $V_{REF5}) \times 1/8$	3Eh	V_{REF9}
1Fh	V_{REF5}	3Fh	V_{REF10}

7. Product Standards

A. Absolute Maximum Ratings

$AV_{SS} = DV_{SS} = 0V$

	Item	Symbol	Rating	Unit
A1	Digital power supply voltage	DV_{DD}	- 0.3 to 6.5	V
A2	Analog power supply voltage	AV_{DD}	- 0.3 to 6.5	V
A3	Digital input voltage	V_{I1}	- 0.3 to DV_{DD} +0.3	V
A4	Analog input voltage	V_{I2}	- 0.3 to AV_{DD} +0.3	V
A5	Digital output voltage	V_{O1}	- 0.3 to DV_{DD} +0.3	V
A6	Analog output voltage	V_{O2}	- 0.3 to AV_{DD} +0.3	V
A7	Operating storage temperature	T_{opr}	- 30 to +85	°C
A8	Operating ambient temperature	T_a	- 20 to +75	°C
A9	Storage temperature	T_{stg}	- 40 to +125	°C

Note: The above absolute maximum ratings represent limits for avoiding damage to the product. They do not guarantee operation.

· The above standards apply only to our standard package for the product.

B. Operating Conditions

Ta = - 20 °C to +75 °C $AV_{SS} = DV_{SS} = 0V$

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
B1	Digital power supply voltage	DV_{DD}		1.65	2.5	3.6	V
B2	Analog power supply voltage	AV_{DD}		3.0	3.3	5.5	V
B3	Gamma adjustment reference voltages	$V_{REF X}$		0.1		AV_{DD} - 0.1	V
B4	Operating frequency	f_{FY}				15	MHz
B5	Drive load capacity	C_Y				50	pF
B6	Digital signal input capacity	C_{IN}	1 MHz		7	15	pF

Notes

(1) Use only direct connections to power supply pins sharing the same symbol (AV_{DD}, DV_{DD}).

(2) Use only direct connections to ground pins sharing the same symbol (AV_{SS} and DV_{SS}).

(3) Apply voltages in the following order: DV_{DD} pins, logic input pins, AV_{DD} pins, and $V_{REF X}$. Remove them in the reverse order.

· The above standards apply only to our standard package for the product.

C. Electrical Characteristics

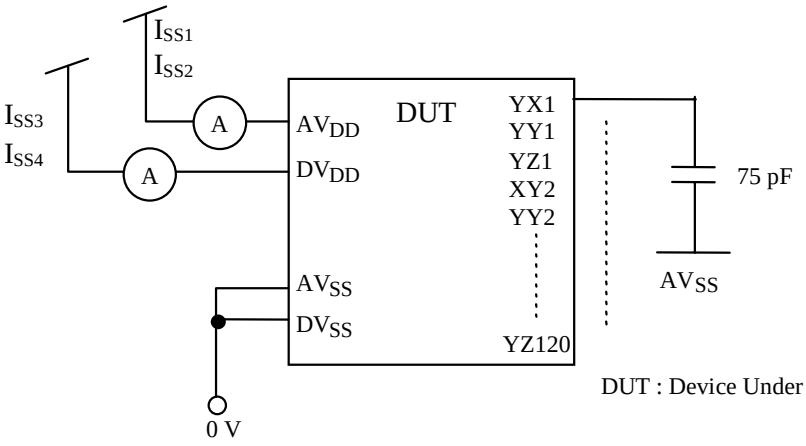
(1) DC Characteristics

DV_{DD} = 2.5V, AV_{DD} = 3.3V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C1	Analog operation power supply current (1)	I_{SS1}	Notes 5 and 6		1.5	3.0	mA
C2	Analog operation power supply current (2)	I_{SS2}	CL = 15pF, R = 2kΩ Notes 5, 6 and 8		1.2		mA
C3	Analog standby power supply current	I_{SS3}	PS = High			10	μA
C4	Digital operation power supply voltage	I_{SS4}	Notes 4 and 5		0.5	1.0	mA
C5	Digital standby power supply current	I_{SS5}	Clock signal off			10	μA

(4) Typical conditions
FY frequency of 15 MHz, raster period of 15 kHz, data pattern alternating between 00 and 3F every raster period, fixed $V_{REF\,x}$

(5) Maximum conditions
FY frequency of 15 MHz, raster period of 15 kHz, data pattern alternating between 00 and 3F every raster period, fixed $V_{REF\,x}$



(6) The loads on the analog output pins are as shown. Note that the numbers for those load circuits sometimes change.

(7) The following is the formula for calculating the power consumption with the loads described in note 5 above.

$I_{SS1} \times AV_{DD} + I_{SS4} \times DV_{DD}$

(8) When C = 15pF, R = 2kΩ, this value is for reference only. It is not guaranteed.

· The above standards apply only to our standard package for the product.

DV_{DD} = 2.5V, AV_{DD} = 3.3V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

Item		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1) Input pins (RL, LD, DX0 to 5, DY0 to 5, DZ0 to 5, FY, INV, PS, MODE1 , MODE2)							
C6	High level input	V_{IH1}	1.65 V ≤ DV_{DD} < 2.5 V	0.8 × DV_{DD}		DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0.7 × DV_{DD}		DV_{DD}	V
C7	Low level input	V_{IL1}	1.65 V ≤ DV_{DD} < 2.5 V	0		0.2 × DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0		0.3 × DV_{DD}	V
C8	Input leak current	I_{LI1}		- 10		10	µA
2) I/O pins (STHR, STHL)							
C9	High level input	V_{IH2}	1.65 V ≤ DV_{DD} < 2.5 V	0.8 × DV_{DD}		DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0.7 × DV_{DD}		DV_{DD}	V
C10	Low level input	V_{IL2}	1.65 V ≤ DV_{DD} < 2.5 V	0		0.2 × DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0		0.3 × DV_{DD}	V
C11	High level output	V_{OH1}	DV_{DD} = 2.5 V, I_O = -1.0 m A	DV_{DD} – 0.5			V
C12	Low level output	V_{OL1}	DV_{DD} = 2.5 V, I_O = 1.0 m A			0.5	V
C13	Input leak current	I_{LI2}		- 10		10	µA
3) Pull down pins (NTEST)							
C14	High level input	V_{IH3}	1.65 V ≤ DV_{DD} < 2.5 V	0.8 × DV_{DD}		DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0.7 × DV_{DD}		DV_{DD}	V
C15	Low level input	V_{IL3}	1.65 V ≤ DV_{DD} < 2.5 V	0		0.2 × DV_{DD}	V
			2.5 V ≤ DV_{DD} ≤ 3.6 V	0		0.3 × DV_{DD}	V
C16	Pull down resistances	R_{PD}			160		k Ω

· The above standards apply only to our standard package for the product.

DV_{DD} = 2.5V, AV_{DD} = 3.3V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
(3) Gamma adjustment resistances							
C17	Resistance	Rγ	Between $V_{REF\,0}$ and $V_{REF\,10}$	23	36	49	kΩ
(4) Analog output pins (YX1 to 120, YY1 to 120, YZ1 to 120)							
C18	High level output current (gray scale output)	I_{OH1}	V_x = 3.2 V V_{OUT} = 2.2 V Note 9			- 0.05	mA
C19	Low level output current (gray scale output)	I_{OL1}	V_x = 0.1 V V_{OUT} = 1.1 V Note 9	0.05			mA
C20	Average output voltage deviation	Δ V_O	2.5 V ≤ V_x		± 15	± 30	mV
			0.8 V < V_x < 2.5 V		± 10	± 20	
			V_x ≤ 0.8 V		± 15	± 30	
C21	Output voltage range	V_O		AV_{SS} +0.1		AV_{DD} - 0.1	V
C22	High level output current (binary output)	I_{OH2}	V_x = 3.3 V V_{OUT} = 2.3V Note 9			- 0.1	mA
C23	Low level output current (binary output)	I_{OL2}	V_x = 0.0 V V_{OUT} = 1.0 V Note 9	0.1			mA

9) V_X is the output voltage for the analog output pin;
V_{OUT}, the voltage applied to the pin.

· The above standards apply only to our standard package for the product.

(2) AC Characteristics

DV_{DD} = 3.3V, AV_{DD} = 3.3V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C24	FY period	t_p	Duty = 50 %	66.6			ns
C25	FY High level pulse width	t_{wcH}		27			ns
C26	FY Low level pulse width	t_{wcL}		27			ns
C27	Data/INV setup time	t_{st1}		15			ns
C28	Data/INV hold time	t_{hd1}		15			ns
C29	Start pulse setup time	t_{st2}		15			ns
C30	Start pulse hold time	t_{hd2}		15			ns
C31	Start pulse Low level pulse width	t_{wsL}		2			FY period
C32	Carry output delay time	t_{d1}	C_L = 15 pF			40	ns
C33	LD signal High level pulse width	t_{wldH}		2			FY period
C34	LD signal Low level pulse width	t_{wldL}		2			FY period
C35	LD signal-start pulse setup time	t_{st3}		2			FY period
C36	LD-FY setup time	t_{st4}		15			ns
C37	LD-FY hold time	t_{sd5}		15			ns
C38	MODE2 setup time	t_{st5}	Note 10)	15			ns
C39	MODE2 hold time	t_{hd5}	Note 10)	15			ns
C40	PS setup time	t_{st6}		15			ns
C41	PS hold time	t_{hd6}		15			ns
C42	Data input invalid interval	t_{ng1}		1			FY period
C43	Final data timing	t_{ng2}				1	FY period
C44	LCD drive signal delay 1	t_{d2}	C_L = 15 pF, R=2KΩ, Note 10)			20	µs
C45	LCD drive signal delay 2	t_{d3}	C_L = 15 pF, R = 2KΩ, Note 11), Note 12)			20	µs
C46	LCD drive signal stop time	t_{d4}	C_L = 15 pF, R = 2KΩ			5	µs

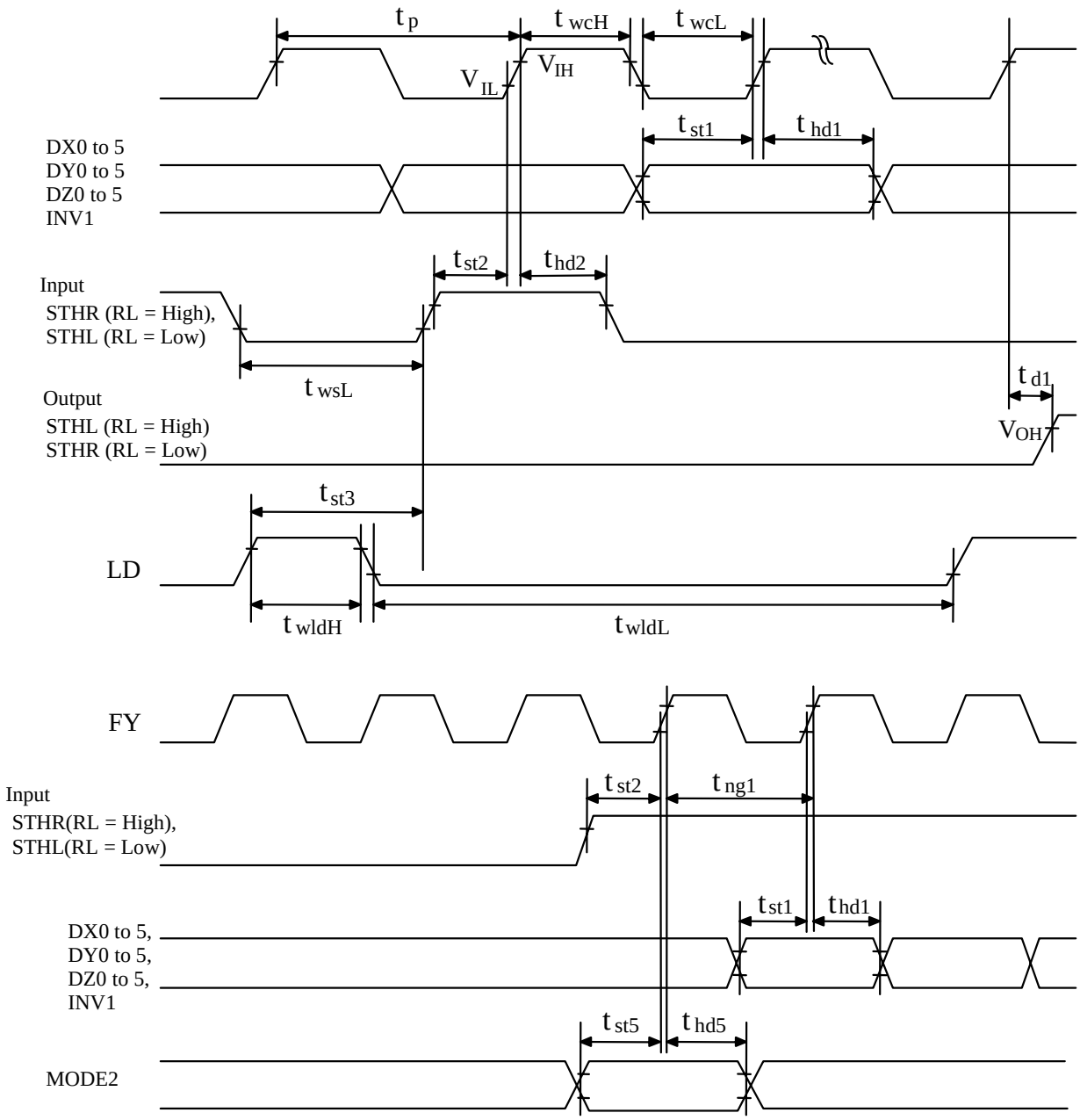
10) The reference point is the first FY rising edge after the rising edge in the start signal (STHR or STHL).

11) This time is defined as that taken for the driver output voltage to reach, within 6-bit precision, the target voltage.

12) The target output voltage shall be the output voltage just before the power save function takes effect—that is, the latter shall be assumed to have reached the target.

· The above standards apply only to our standard package for the product.

AC Characteristics Timing Chart 1

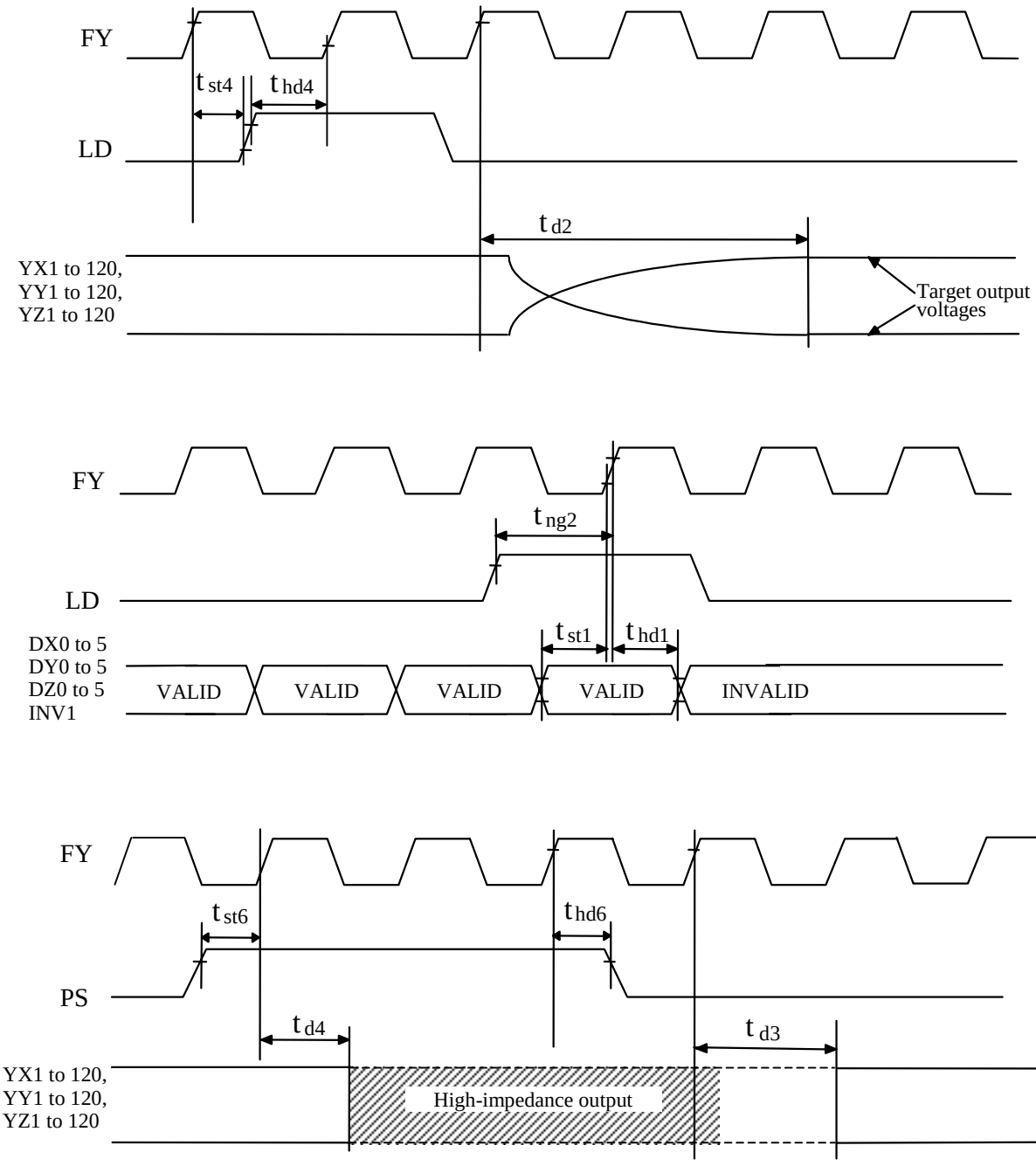


Note
In the absence of any indication to the contrary, the following levels are assumed.

$V_{IH} = V_{OH} = 0.8 \times DV_{DD}$

$V_{IL} = V_{OL} = 0.2 \times DV_{DD}$

AC Characteristics Timing Chart 2



Note
In the absence of any indication to the contrary, the following levels are assumed.

$V_{IH} = V_{OH} = 0.8 \times DV_{DD}$

$V_{IL} = V_{OL} = 0.2 \times DV_{DD}$

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