MN86063

High-Speed CODEC LSI for Facsimile Images

■ Overview

The MN86063 is a high-speed LSI codec for compressing and decompressing facsimile images. Features include real-time printing to laser printers, built-in line memory, enlargement and reduction, and code conversion.

■ Features

- Pixels per line:
  between 16 and 4864 bits, in word (16-bit) increments.
- Processing time per line:
  Individual pixels are processed within two system clock cycles. For a machine cycle of 10 MHz, processing the worst-case pattern for a 4096-bit line takes no more than 1 ms.
- Time-shared, multiplex processing
  Support for time-shared, multiplex processing allows image I/O, enlargement/reduction processing, and coding/decoding to proceed concurrently for a group of lines. Image bus DMA transfers can also proceed concurrently with command processing.
- Multiple channels
  If lines consist of 2432 bits or fewer, commands can be processed simultaneously on two channels using time-sharing. These commands may be issued asynchronously.
- Bus configuration
  There are separate system and image buses. The latter features two independent master DMA channels; the former, four slave DMA channel pins.
- Image data I/O
  Image data I/O can use either the image or system bus.
- Byte conversion
  When the system bus is 16 bits wide, the chip can swap the upper and lower bytes of image or coded data. It can also swap the MSB and LSB.
- Memory management
  The chip includes pointer management for the image buffer connected to the image bus.
- Machine cycle
  The limit is 10 MHz. This means that the maximum input clock is twice this, or 20 MHz.

■ Function

- Message coding:
  MH, MR, MMR, and MG3. The chip also supports data transfers on the image and system buses and DMA transfers on the image bus alone.
- Coding conversion
  The chip converts between all supported message coding systems: MH, MR, MMR, and MG3.
- Enlargement/reduction
  These may be added to coding, decoding, code conversion, and data transfer operations.

(1) In the primary scan direction, the chip uses multiplication on the change point address. The scaling factor can be anywhere between approximately 0.1% and 200% in increments of approximately 0.1%. Integral multiplication is also available beyond this

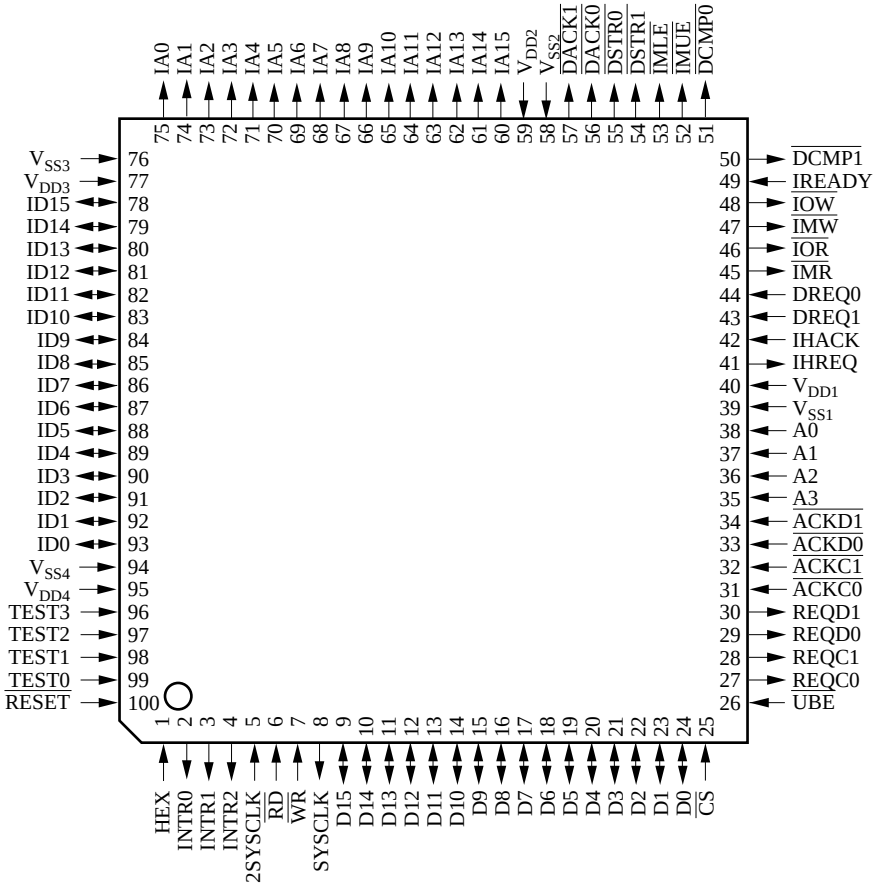
(2) In the subscanning direction, the chip uses decimation and replication. The scaling factor can be anywhere between approximately 0.0015% and 200% in increments of approximately 0.0015%. Integral multiplication is also available from 2 to 65,535.

- White masks for both edges
  These may be added to coding, decoding, code conversion, and data transfer operations. They change all pixels within the margins, specified in bit increments, to white.
- Decoding error processing
  The chip offers a choice of replacing with the previous line or a white line.

■ Applications

- Facsimile equipment

■ Pin Assignment



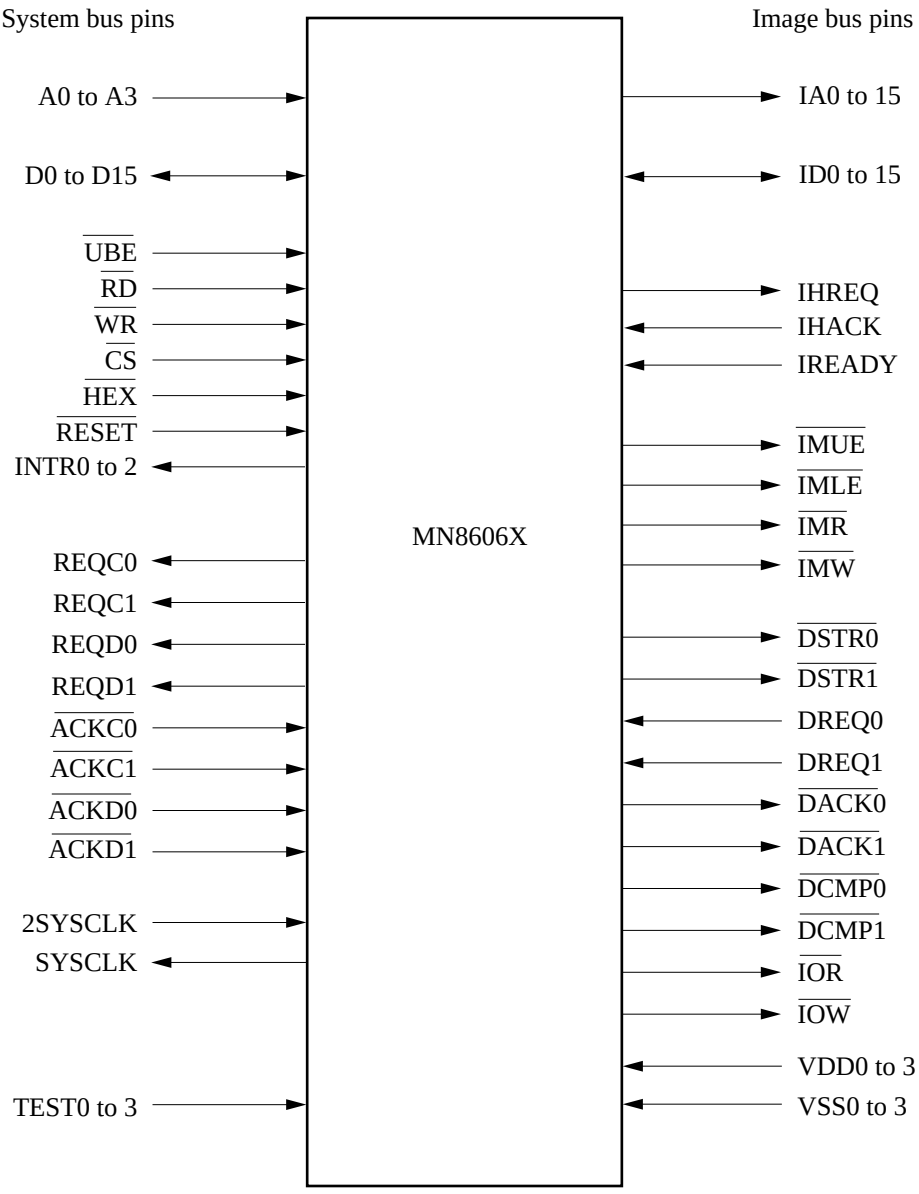
QFP100-P-1818

■ Pin Configuration

The MN86063 features two buses: the system bus, which is primarily used for transferring coded data to and from a microprocessor and other components and the image bus, which is used for transferring image data to or from a scanner, printer, or the like.

■ Pin Function Chart

The chip has a total of 100 pins: 39 for the system bus, 49 for the image bus, and 12 for testing, power supply, and other purposes.



■ Pin Descriptions

● System Bus

Pin No.	Symbol	I/O	Function Description
35	A3	I	Address. Address bus for accessing internal registers
36	A2		
37	A1		
38	A0		
9	D15	I/O	Data. Data bus for bidirectional transfers over system bus
10	D14	Tristate	
11	D13		
12	D12		
13	D11		
14	D10		
15	D9		
16	D8		
17	D7		
18	D6		
19	D5		
20	D4		
21	D3		
22	D2		
23	D1		
24	D0		
26	$\overline{\text{UBE}}$	I	Upper byte enable. This input pin specifies whether the data from pins D15–D8 is effective.
6	$\overline{\text{RD}}$	I	Read. This input pin specifies a read from the specified register.
7	$\overline{\text{WR}}$	I	Write. This input pin specifies a write to the specified register.
25	$\overline{\text{CS}}$	I	Chip select. This input pin specifies access to a register.
1	$\overline{\text{HEX}}$	I	Data bus width selection. This input pin specifies the width of the system data bus: "0" for 16 bits; "1" for 8 bits.
100	$\overline{\text{RESET}}$	I	Reset. This input pin resets the internal circuitry, clearing all registers.
2	INTR0	O Open corrector	Interrupt request 0. This output pin indicates an interrupt request triggered by the cause given in interrupt register 0 (STIR0)
3	INTR1	O Open corrector	Interrupt request 1. This output pin indicates an interrupt request triggered by the cause given in interrupt register 1 (STIR1)
4	INTR2	O Open corrector	Interrupt request 2. This output pin indicates an interrupt request triggered by the cause given in DMA transfer interrupt register (DMIR).
27	REQC0	O	DMA transfer output request 0. This output pin indicates a request for data output on DMA channel 0.
28	REQC1	O	DMA transfer output request 1. This output pin indicates a request for data output on DMA channel 1.

■ Pin Descriptions (continued)

● System Bus (continued)

Pin No.	Symbol	I/O	Function Description
29	REQD0	O	DMA transfer input request 0. This output pin indicates a request for data input on DMA channel 0.
30	REQD1	O	DMA transfer input request 1. This output pin indicates a request for data input on DMA channel 1.
31	$\overline{\text{ACKC0}}$	I	DMA transfer output acknowledge 0. This input pin accepts the response to a DMA transfer request with REQC0.
32	$\overline{\text{ACKC1}}$	I	DMA transfer output acknowledge 0. This input pin accepts the response to a DMA transfer request with REQC1.
33	$\overline{\text{ACKD0}}$	I	DMA transfer input acknowledge 0. This input pin accepts the response to a DMA transfer request with REQD0.
34	$\overline{\text{ACKD1}}$	I	DMA transfer input acknowledge 0. This input pin accepts the response to a DMA transfer request with REQD1.
5	2SYSCLK	I	2 system clock. This input pin accepts a clock signal with a frequency twice that of the system clock.
8	SYSCLK	O	System clock. This output pin provides a clock signal with half the frequency of 2SYSCLK.

● Image Bus

Pin No.	Symbol	I/O	Function Description
60	IA15	O	Image address bus. These pins provide an address on the image data bus.
61	1A14	Tristate	
62	IA13		
63	IA12		
64	IA11		
65	IA10		
66	IA9		
67	IA8		
68	IA7		
69	IA6		
70	IA5		
71	IA4		
72	IA3		
73	IA2		
74	IA1		
75	IA0		

■ Pin Descriptions (continued)

● Image Bus (continued)

Pin No.	Symbol	I/O	Function Description
78	ID15	I/O	Image data. These pins form a bus for bidirectional transfers of image data.
79	ID14	Tristate	
80	ID13		
81	ID12		
82	ID11		
83	ID10		
84	ID9		
85	ID8		
86	ID7		
87	ID6		
88	ID5		
89	ID4		
90	ID3		
91	ID2		
92	ID1		
93	ID0		
41	IHREQ	O	Image bus request. This output pin indicates a request for control of the image bus.
42	IHACK	I	Image bus acknowledge. This input pin indicates when the chip can seize control of the image bus.
49	IREADY	I	Image data acknowledge. This input pin indicates the end of the read/ write operation.
52	$\overline{\text{IMUE}}$	O Tristate	Image memory upper byte enable. This output pin specifies whether the data from pins ID15–ID8 is effective.
53	$\overline{\text{IMLE}}$	O Tristate	Image memory lower byte enable. This output pin specifies whether the data from pins ID7–ID0 is effective.
45	$\overline{\text{IMR}}$	O Tristate	Image memory read. This output pin indicates a read from the address on the image address bus.
47	$\overline{\text{IMW}}$	O Tristate	Image memory write. This output pin indicates a write to the address on the image address bus.
55	$\overline{\text{DSTR0}}$	O	DMA start 0. This output indicates that the chip is ready for a DMA transfer from an I/O device to memory.
54	$\overline{\text{DSTR1}}$	O	DMA start 1. This output indicates that the chip is ready for a DMA transfer from memory to an I/O device.
44	DREQ0	I	DMA request 0. This input pin indicates a request for a DMA transfer from an I/O device to memory.
43	DREQ1	I	DMA request 1. This input pin indicates a request for a DMA transfer from memory to an I/O device.
56	$\overline{\text{DACK0}}$	O	DMA acknowledge 0. This output pin gives the response to the DREQ0 signal, initiating a DMA transfer from an I/O device to memory.
57	$\overline{\text{DACK1}}$	O	DMA acknowledge 1. This output pin gives the response to the DREQ1 signal, initiating a DMA transfer from memory to an I/O device.

■ Pin Descriptions (continued)

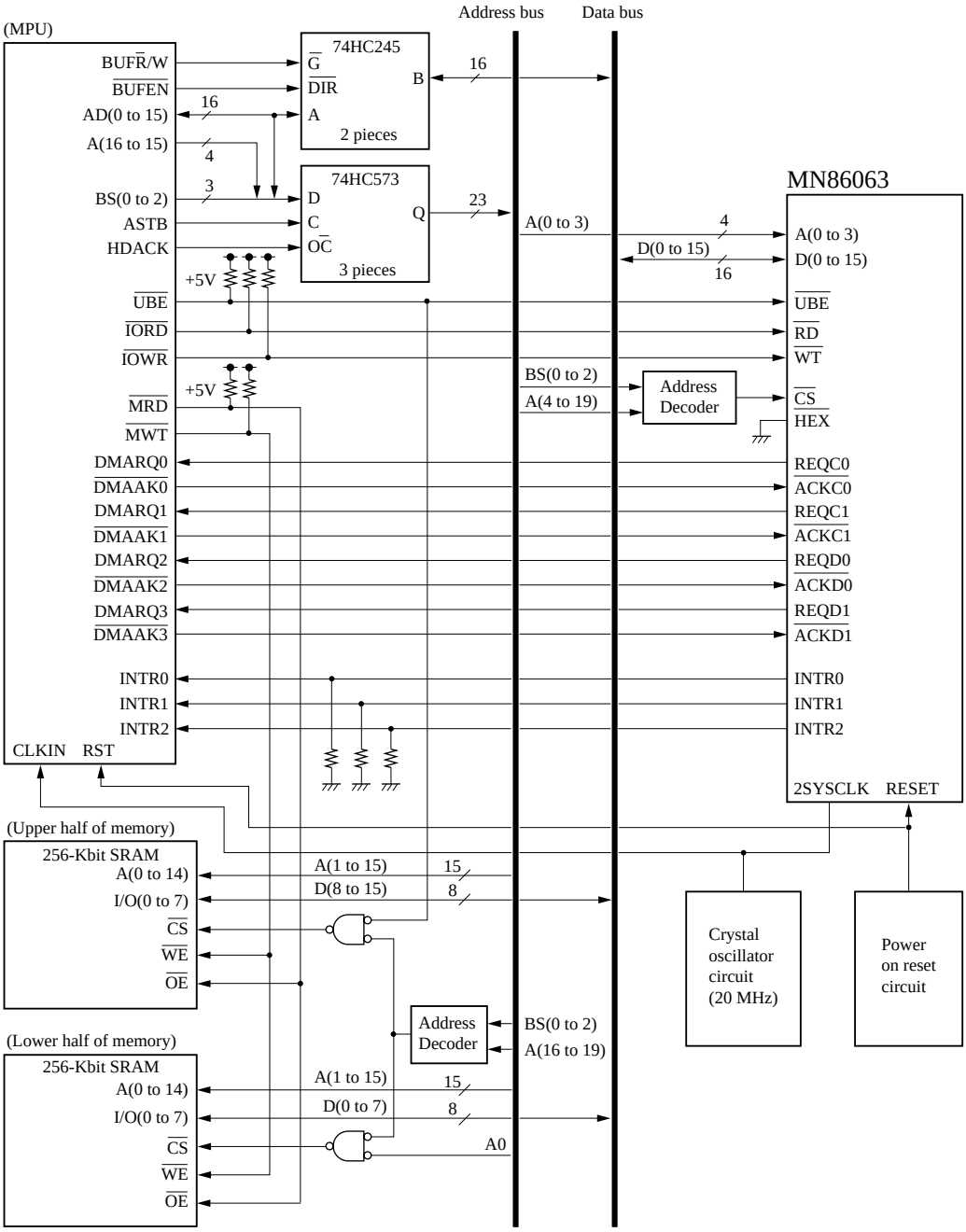
● Image Bus (continued)

Pin No.	Symbol	I/O	Function Description
51	$\overline{DCMP0}$	O	DMA complete 0. This output pin indicates the successful completion of the DMA transfer of 1 line of data from an I/O device to memory.
50	$\overline{DCMP1}$	O	DMA complete 1. This output pin indicates the successful completion of the DMA transfer of 1 line of data from memory to an I/O device.
46	$\overline{IOR}$	O Tristate	I/O device read. This output pin indicates a read from an I/O device connected to the image address bus.
48	$\overline{IOW}$	O Tristate	I/O device write. This output pin indicates a write to an I/O device connected to the image address bus.

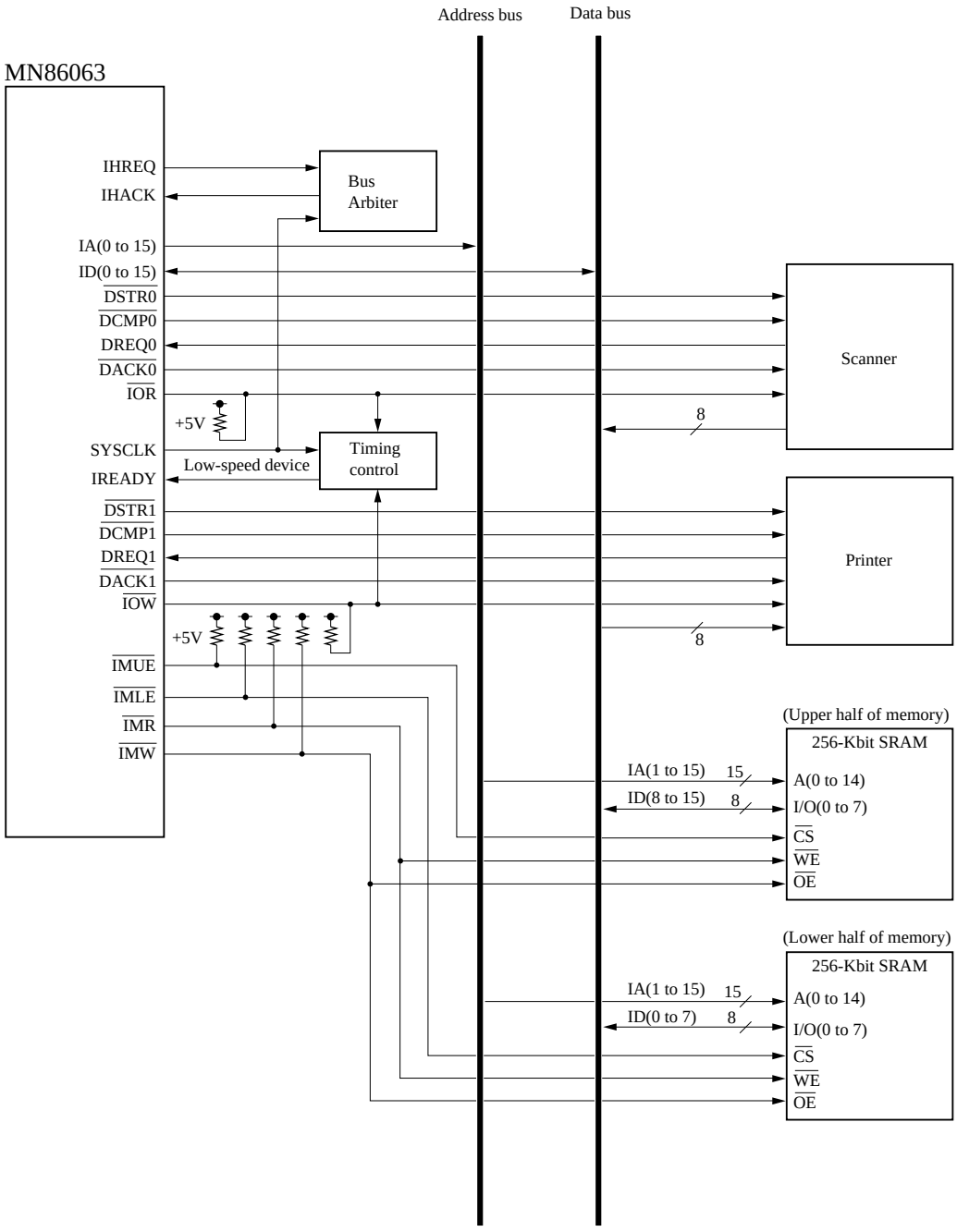
● Power on Reset Circuit

Pin No.	Symbol	I/O	Function Description
96	TEST3	I	Test mode. Connect all these pins to the ground.
97	TEST2		
98	TEST1		
99	TEST0		
40	V_{DD1}	I	5 volt power supply. Connect all these pins to a 5 volt power supply.
59	V_{DD2}		
77	V_{DD3}		
95	V_{DD4}		
39	V_{SS1}	I	Ground. Connect all these pins to the ground.
58	V_{SS2}		
76	V_{SS3}		
94	V_{SS4}		

■ Application Circuit Example #1. Sample Connections to System Bus



■ Application Circuit Example #2. Sample Connections to Image Bus



■ Package Dimensions (Unit: mm)

QFP100-P-1818