National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC501A-X REV 0A0

Original Creation Date: 08/06/98
Last Update Date: 03/09/99
Last Major Revision Date: 02/26/99

HIGH-SPEED OUTPUT CLAMPING OP AMP

General Description

The CLC501 is a high-speed current-feedback op amp with the unique feature of output voltage clamping. This feature allows both the maximum positive (Vhigh) and negative (Vlow) output voltage levels to be established. This is useful in a number of applications in which "downstream" circuitry must be protected from overdriving input signals. Not only can this prevent damage to downstream circuitry, but can also reduce time delays since saturation is avoided. The CLC501's very fast 1ns overload/clamping recovery time is useful in applications in which information-containing signals follow overdriving signals.

Engineers designing high-resolution, subranging A/D systems have long sought an amplifier capable of meeting the demanding requirements of the residue amplifier function. Amplifiers providing the residue function must not only settle quickly, but recover from overdrive quickly, protect the second stage A/D, and provide high fidelity at relatively high gain settings. The CLC501, which excels in these areas, is the ideal design solution in this onerous application. To further support this application, the CLC501 is both characterized and tested at a gain setting of +32, the most common gain setting for residue amplifier applications.

The CLC501's other features provide a quick, high-performance design solution. Since the CLC501's current feedback design requires no external compensation, designers need not spend their time designing compensation networks. The small 8-pin package and low, 180mW power consumption make the CLC501 ideal in numerous applications having small power and size budgets.

Industry Part Number

CLC501A

NS Part Numbers

CLC501AJ-MLS
CLC501AJ-QML*
CLC501AWG-MLS
CLC501AWG-QML**

Prime Die

UB1148C

Controlling Document

5962-8997401PA*,MXA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Output clamping (Vhigh and Vlow)
- 1ns recovery from clamping/overdrive
- 0.05% settling in 12ns
- Characterized and guaranteed at Av = +32
- Low power, 180mW

Applications

- Residue amplifier in high-accuracy, subranging A/D systems
- High-speed communications
- Output clamping applications
- Pulse amplitude modulation systems

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	70mA
Junction Temperature (Tj)	+175 C
Storage Temperature	-65 C to +150 C
Lead Temperature (soldering, 10 seconds)	+300 C
Power Dissipation (Pd) (Note 2)	TBD
Common Mode Input Voltage (Vcm)	Vs
Thermal Resistance	
ThetaJA (Junction to Ambient)	
CERAMIC DIP (Still Air)	TBD
(500LFPM)	TBD
SOIC (Still Air)	TBD
(500LFPM)	TBD
ThetaJC (Juntion to Case)	
CERAMIC DIP	TBD
SOIC	TBD
Package Weight (Typical)	
CERAMIC DIP	TBD
SOIC	TBD
ESD Tolerance (Note 3)	
ESD Rating	<1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Gain Range (Av)	+7 to +50 and -1 to -50
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, feedback resistance (Rf) = 1.5kOhms, and gain setting resistance (Rg) = 48.3Ohms. -55 C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)	Rs = 50Ohms				±25	uA	1
						±35	uA	2
						±37	uA	3
-Iin	Input Bias Current (inverting)	Rs = 50Ohms				±30	uA	1
						±40	uA	2
						±46	uA	3
Vio	Input Offset Voltage	Rs = 50Ohms				±3.0	mV	1
						±5.0	mV	2
						±4.6	mV	3
Tc (+Iin)	Average +Input Bias Current Drift	Rs = 50Ohms	1			±100	nA/C	2
			1			±150	nA/C	3
Tc (-Iin)	Average -Input Bias Current Drift	Rs = 50Ohms	1			±100	nA/C	2
			1			±200	nA/C	3
Tc (Vio)	Average Offset Voltage Drift	Rs = 50Ohms	1			±20	uV/C	1, 2, 3
Is	Supply Current	No Load				24	mA	1, 2
						25	mA	3
PSRR	Power Supply Rejection Ratio	+Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V			60		dB	1, 2
					55		dB	3
CMRR	Common Mode Rejection Ratio	Vcm = ±1V	1		60		dB	1, 2
		Vcm = ±1V	1		55		dB	3
±Iout	Output Current	Rl = 100Ohms	1		±50		mA	1, 2
±Iout	Output Current	Rl = 100Ohms	1		±30		mA	3
Rout	Output Impedance at dc	Rl = 100Ohms	1			0.3	Ohms	1, 2, 3
+Rin	Input Resistance		1		100		kOhms	1, 2
			1		50		kOhms	3
Cin	Input Capacitance	Ta = +25 C	1			7	pF	4
±Vout	Output Voltage Swing	Rl = 100Ohms			±2.4		V	4, 5, 6

Electrical Characteristics

DC PARAMETERS: CLAMPING CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, feedback resistance (Rf) = 1.5kOhms, and gain setting resistance (Rg) = 48.3Ohms. -55 C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voc	Clamp Accuracy					±0.2	V	1, 2, 3
ICL	Input Bias Current on Vhigh and Vlow		1			±50	uA	1, 2
			1			±100	uA	3
CDR	Input Offset Voltage Drift After Recovery		1			200	uV	1, 2, 3
OVC	Overshoot in Clamp		1			15	%	4
CMC	Clamping Range	At Vhigh or Vlow	1		±3.3		V	4, 5
			1		±3.0		V	6
TSO	Overload Recovery from Clamp		1			3	ns	9, 10, 11

AC PARAMETERS: FREQUENCY DOMAIN CHARCTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, feedback resistance (Rf) = 1.5kOhms, and gain setting resistance (Rg) = 48.3Ohms. -55 C ≤ Ta ≤ +125 C (note 3)

SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 5Vpp			60		MHz	4
			2		45		MHz	5
			2		60		MHz	6
		-3dB bandwidth, Av = +20, Vout < 2Vpp	1		85		MHz	4
			1		55		MHz	5
			1		85		MHz	6
GFPL	Gain Flatness, Peaking Low	0.1MHz to 15MHz, Vout < 5Vpp				0.1	dB	4
			2			0.1	dB	5, 6
GFPH	Gain Flatness, Peaking High	> 15MHz, Vout < 5Vpp				0.2	dB	4
			2			0.2	dB	5, 6
GFR	Gain Flatness, Rolloff	0.1MHz to 30MHz, Vout < 5Vpp				1.0	dB	4
			2			1.3	dB	5
			2			1.0	dB	6
LPD	Linear Phase Deviation	0.1MHz to 30MHz, Vout < 5Vpp	1			1.0	Deg	4, 5, 6

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, feedback resistance (Rf) = 1.5kOhms, and gain setting resistance (Rg) = 48.3Ohms. -55 C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2Vpp at 20MHz			-33		dBc	4
			2		-30		dBc	5, 6
HD3	3rd Harmonic Distortion	2Vpp at 20MHz			-50		dBc	4
			2		-50		dBc	5
			2		-45		dBc	6
SNF	Noise Floor	> 1MHz	1			-156	dBm 1Hz	4, 6
			1			-155	dBm 1Hz	5
INV	Integrated Noise	1MHz to 100MHz	1			35	uV	4, 6
			1			40	uV	5

AC PARAMETERS: Timing Domain Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, feedback resistance (Rf) = 1.5kOhms, and gain setting resistance (Rg) = 48.3Ohms. -55 C ≤ Ta ≤ +125 C (note 3)

SR	Slew Rate	Cl < 10pF, measured at ±1V with 3V step	1		800		V/uS	4, 6
		Cl < 10pF, measured at ±1V with 3V step	1		700		V/uS	5
Tr	Rise and Fall Time	2V step, Cl < 10pF	1			5.8	nS	9, 11
			1			7.8	nS	10
Tf	Rise and Fall Time	5V step, Cl < 10pF	1			6.5	nS	9, 11
			1			8	nS	10
Ts	Settling Time	2V step at ±0.05% of the fixed value, Cl < 10pF	1			18	nS	9, 11
		2V step at ±0.05% of the fixed value, Cl < 10pF	1			24	nS	10
OS	Overshoot	2V step, Cl < 10pF	1			5	%	9, 10, 11

Electrical Characteristics

DC PARAMETERS: DRIFT LIMITS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100Ohms, Vs = ±5V dc, Vhigh = +3V, Vlow = -3V, Av = +32, (Rf) = 1.5kOhms, (Rg) = 48.3Ohms.
"Deltas not required on B-level product. Deltas required for S-level (-MLS) product as specified on Internal Processing Instructions (IPI)." (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)	Rs = 50 Ohms				±2.5	uA	1
-Iin	Input Bias Current (inverting)	Rs = 50 Ohms				±3.0	uA	1
Vio	Input Offset Voltage	Rs = 50 Ohms				±0.3	mV	1
Is	Supply Current	No Load				±2.4	mA	1

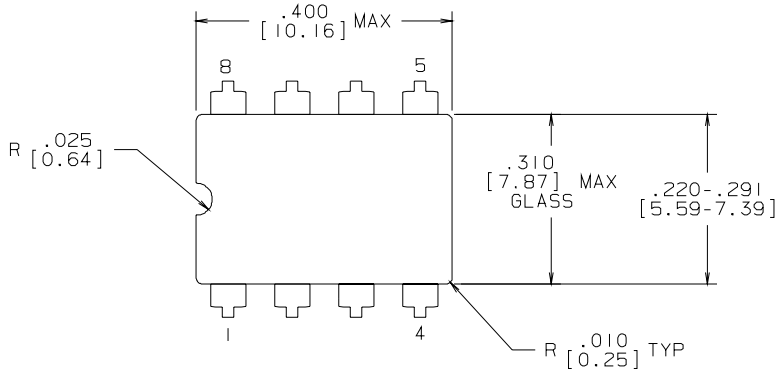
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The limiting terms, "Min" (minimum) and "Max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

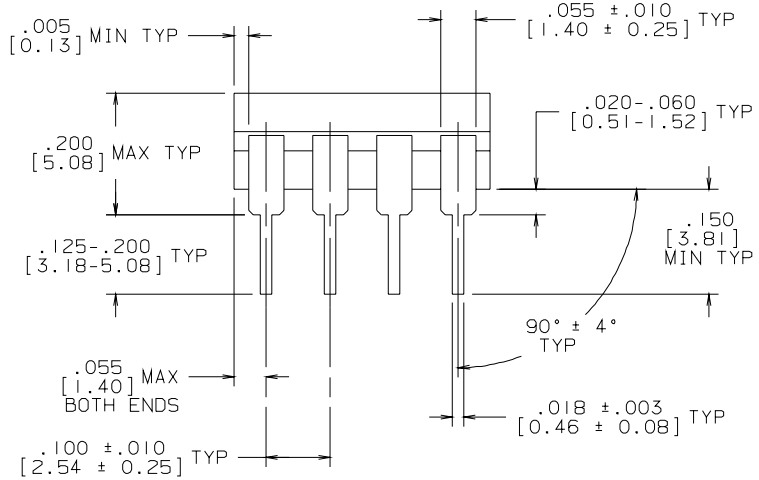
Graphics and Diagrams

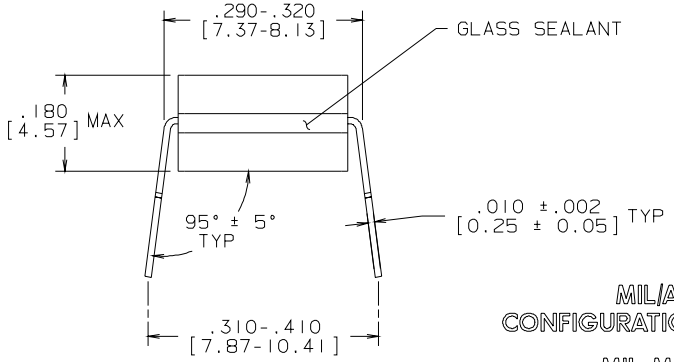
GRAPHICS#	DESCRIPTION
07070HRA2	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000409A	CERDIP (J), 8 LEAD (PINOUT)
P000448A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
WG10ARB	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

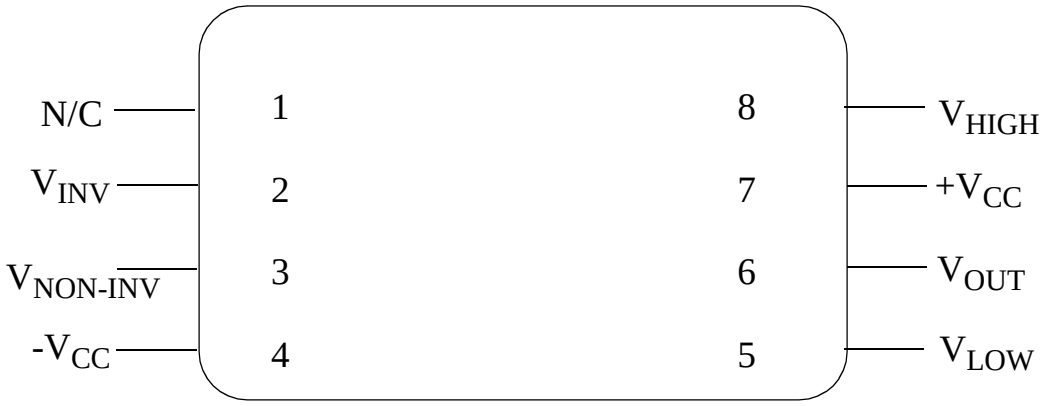
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC501J

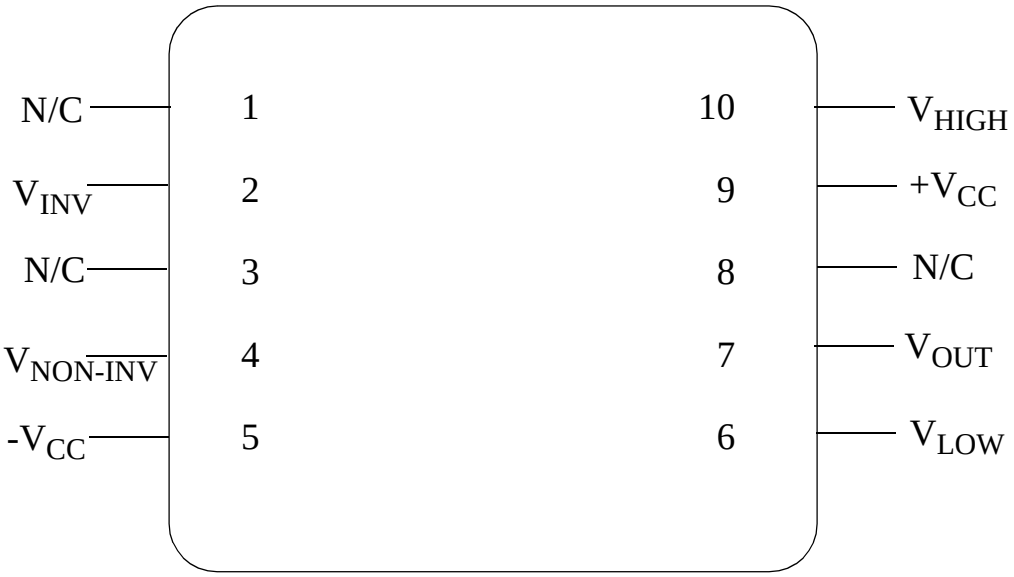
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000409A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC501AWG

10 - LEAD CERAMIC SOIC

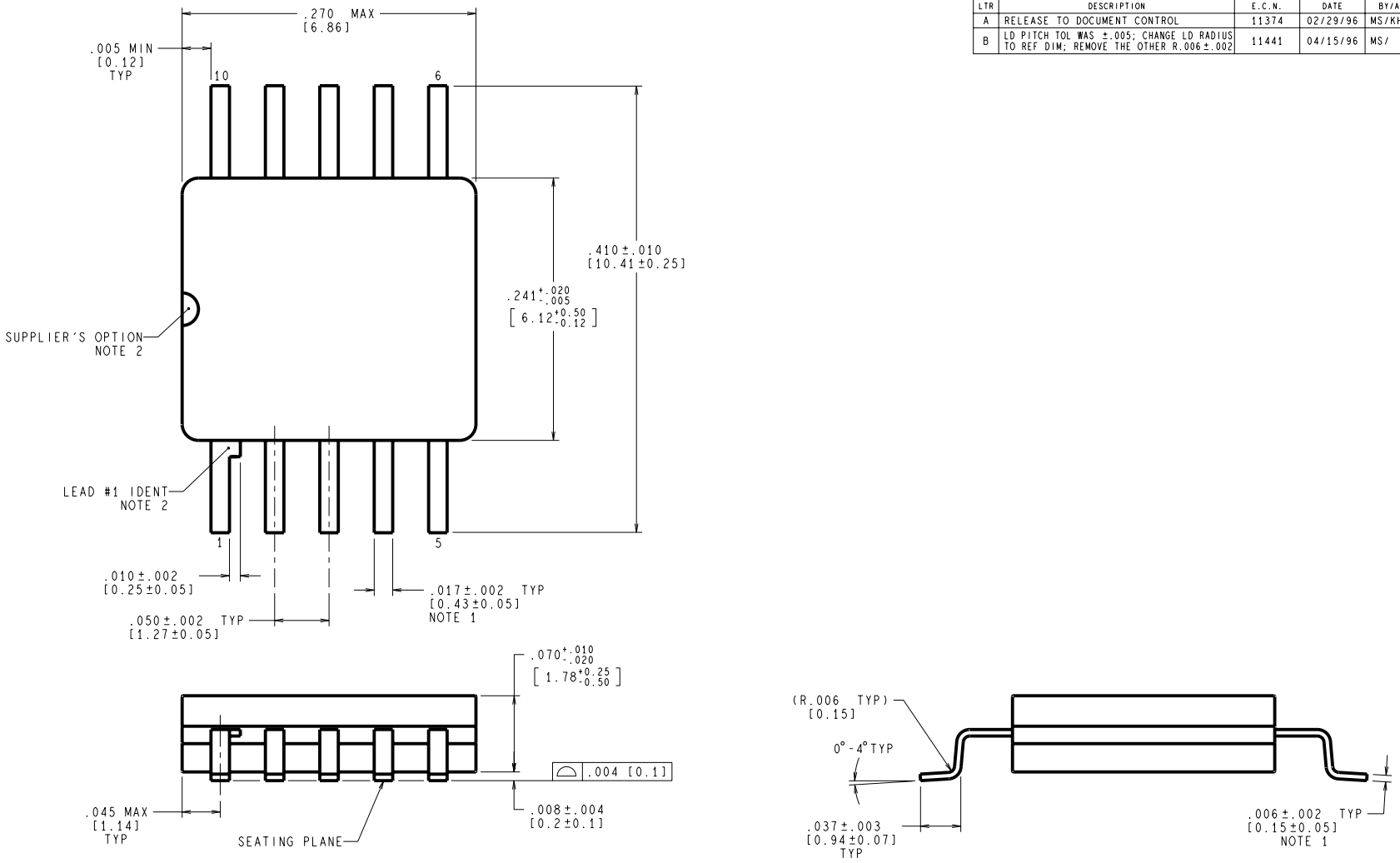
CONNECTION DIAGRAM

TOP VIEW

P000448A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/96	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002	11441	04/15/96	MS/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
10 LEAD,
GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-WG10A	B

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003288	03/09/99	Shaw Mead	Initial MDS Release