CODE No.		Total pages	88	Page	1
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(TENTATIVE)

SPECIFICATIONS

PART No. : MNF8931BK-C

V 1.05

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Please ask for the latest Specifications to guarantee the satisfaction of your product requirements.

SYSTEM LSI DIVISION
SEMICONDUCTOR COMPANY
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

ESTABLISHED BY	CHECKED BY	CHECKED BY	PREPARED BY

DATE PREPARED	DATE ESTABLISHED				
Mar. 12, 2003					

Table of Contents

1. Type

CMOS IC Controller Driver for LCD Panel Source Driving

2. Overview

This product is a single-chip IC incorporating a RAM controller source driver that displays 260000 colors for TFT LCD driving. By using this IC in combination with the MN863480, which is a gate driver with a built-in IC power supply, a 260000-color TFT display system with a maximum of 176 (H) × 240 (V) pixels will be constructed.

3. Features

1) Display capacity
- 176 pixels max. × RGB × 240 lines (528 output source driver/240 output gate driver control)

2) Display colors
- 260000 colors (18 bits/pixel, RGB: 6 bits each)

3) Interface
- Supports 80-/68-series (8-, 9-, 16-, or 18-bit) CPU interface, serial interface, or RGB interface.
  - → The CPU interface and RGB interface are different from each other in port. These ports are selected by command settings.
  - → The RGB interface is for writing GRAM (graphic RAM) data only. Commands are transferred through the CPU interface or serial interface.
  - → The serial interface allows data writing only.

4) GRAM (graphic RAM)

[Capacity]
- 176 × 18 (6 + 6 + 6) × 240 bits (760320 bits)

[Operation speed]
- Host write speed: 10 MHz

[GRAM control]
- RAM access range setting (A rectangular area specifies a GRAM access range.)
  - → Two modes of range setting are available (to specify the start and end points or the start point and access width)
- RAM address automatic count (with count direction control)
  - → The RAM write direction (vertically and horizontally) is variable, and so is the screen display size (vertically and horizontally).
- Generates addresses according to the mounting direction of the source driver. (X address reverse command)
- Access byte order variable (16-bit bus with 260000-color data × 2-time transfer/pixel)
- Window mask function (Write data mask specified inside and outside the window area)
- Pixel mask function (WDMSK pin)
- Bit write mask function (Bit mask command)
- RAM clear function (Data specified for R, G, and B independently)
- Display start line address setting (Used for vertical scrolling)

5) Display mode control
- Display control (Display OFF, all white display, normal display, and partial display)
- Display data reverse display function
- Gradation LSB function (Automatic generation of R and B's LSB in 65000-color mode)
- Digital brightness adjustment function (in R, G, and B independent control)

6) Display timing control
- Oscillation circuit built in (206.6-kHz display clock with no external CR circuit required)
- 1H period variable (8 to 24 clocks in 1-clock increments)
- 1V period variable (up to 1024H in 4H increments, the specified range of which varies with the number of gate outputs)
- Supports external synchronization (enabling animated picture data to be written)
- Alternation control (1H line/Frame reverse)

☆ This document is based on an equivalent Japanese document that was prepared on Jun. 3, 2002.

7) Partial display
- Possible to display up to two non-display areas
- Sets the refresh cycle of non-display areas

8) Partial scroll
- Allows partial area specification for scrolling (setting the start/end point and the number of scrolls)

9) Source driver
- Supports a maximum of 176 pixels
- Supports gradation/binary driving (with reduced power consumption by binary driving)
- Allows automatic drive interruption settings for blanking periods
- Analog gamma correction with VREF resistance adjustments (allowing independent positive and negative polarity settings)

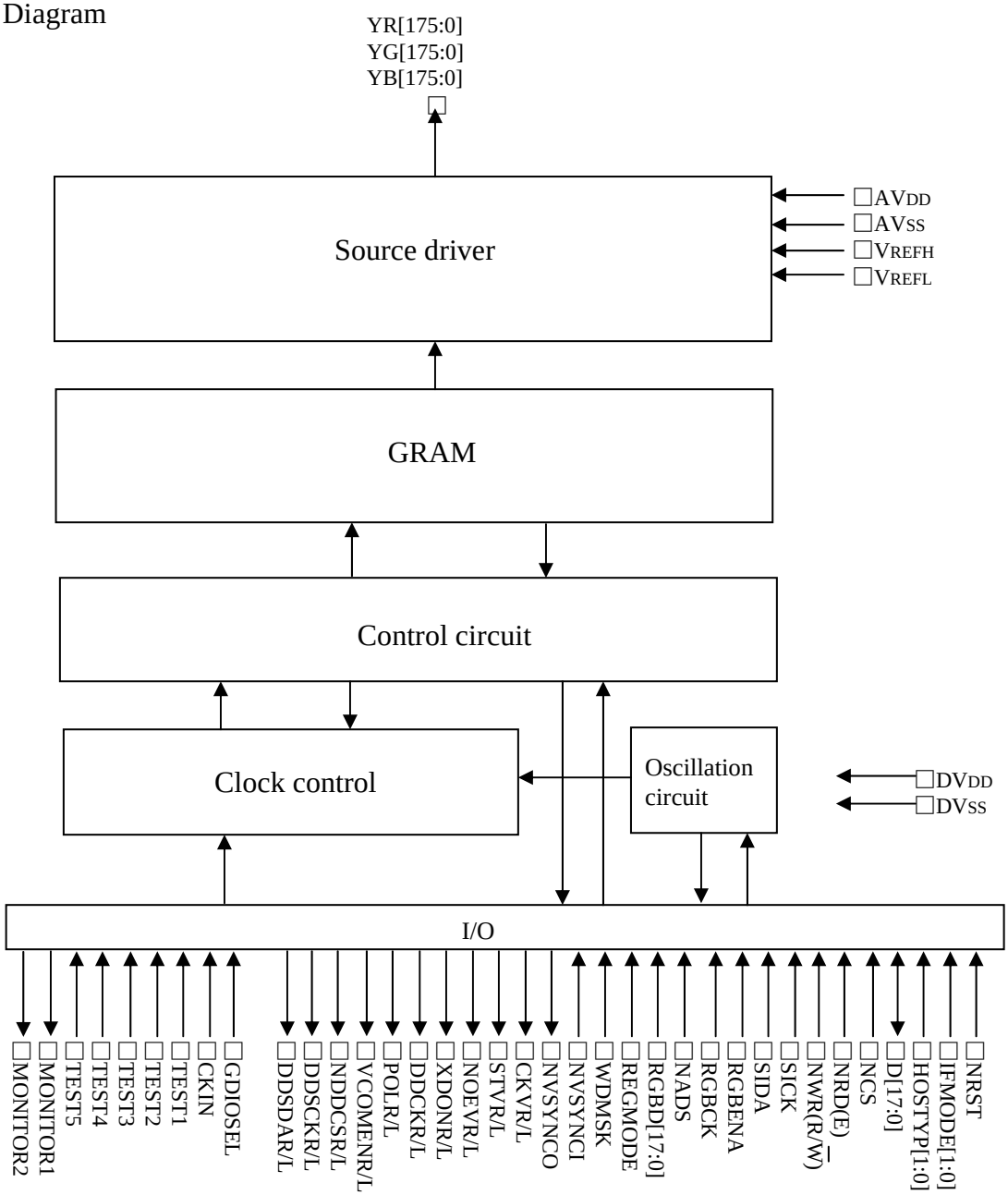
10) Gate driver/Power supply IC control

★ Controls the MN863480 gate driver with the built-in power supply IC to be used in combination.
- Automatic serial transfer of set values to the MN863480 by set value transfer commands.

[Gate driver control]
- Supports gate driver 192, 220, and 240 outputs
- Shift direction control
- Output prohibit period control (Timing variable within 1H in 1-clock increments)
- Gate all ON control (XDON pin)

[Power supply IC control]
- Power supply IC ON/OFF
- Power supply IC drive control
- Voltage adjustments to drive a variety of LCDs

4. Block Diagram



5. Pins

5.1 Host Interface Pins

Signal name	I/O	Function	Description
NRST	Input	Reset	A reset pin. The IC will be reset with the pin set low.
IFMODE[1:0]	Input	Interface mode selection	Used to set the data bus width of the interface.

IFMODE	Description	IFMODE	Description
00	18-bit mode	10	9-bit mode
01	16-bit mode	11	8-bit mode

HOSTYP[1:0]	Input	Host type selection	Used to select host CPU types.

HOSTYP	Description	HOSTYP	Description	HOSTYP	Description
00	80-series interface	01	68-series interface	1x	Serial interface

D[17:0]	I/O	Data I/O	Data I/O pins for the host interface. Pins are enabled by IFMODE pin settings (8, 9, 16, or 18 bits). Fix the pin at low or high level if the pin is not used. (The level is not fixed with IC output.)
NCS	Input	Chip select	A chip select input pin. The pin set low will be active.
NRD (E)	Input	Access control	• Used for read signal input if the 80-series CPU is connected. The data pin (D[17:0]) will be in the status of output with this pin set low. • Used for enable clock (E) input if the 68-series MPU is connected. The pin set high will be enabled.
NWR (R/$\overline{W}$)	Input	Access control	• Used for write signal input if the 80-series CPU is connected. The data pin will be in the status of input with this pin set low, and data will be latched at the rising edge of the write signal. • Used for read/write control input if the 68-series MPU is connected. The pin set high will be in read control. The pin set low will be in write control.
SICK	Input	Serial interface clock input	Used for serial interface clock input. Data will be retrieved at the rising edge of the input. Fix the pin at low level if no serial interface is used.
SIDA	Input	Serial interface data input	Used for data input into the serial interface. The first data is used to discriminate address transfer and data transfer. (Low: Address transfer; High: Data transfer) Fix the pin at low level if no serial interface is used.
RGBENA	Input	RGB interface selection	An enable pin for the RGB interface. The RGBD[17:0] pin will be enabled with this pin set high.
RGBCK	Input	RGB interface clock input	Used for clock input for the RGB interface. Data will be retrieved at the falling edge of the clock when the RGBENA signal is at high level.
RGBD[17:0]	Input	Data input	Used for data input for the RGB interface. Image data input will be retrieved at the falling edge of the RGBCK when the RGBENA is set high and the RMWR bit is set to 1. Fix the pin at low or high level when the pin is not used.
NADS	Input	Data discrimination signal	Used for discriminating addresses and data. Low: Addresses; High: Data
REGMODE	Input	Register write mode selection	Used to specify the register access mode while the IC is in 18-/16-bit interface mode. The following operation will be possible with this pin set when the NADS is set low. REGMODE set high: The address is specified by the upper 8 bits and data is specified by the lower 8 bits. REGMODE set low: Only the lower 8 bits are enabled to gain access to the register at a specified address and cycle of data transfer.
WDMSK	Input	Write data mask signal	Used to specify write masks in GRAM data pixels. When this signal is at high level, GRAM data written will be masked. There will be a GRAM address increment while the mask is enabled.
NVSYNCI	Input	External vertical sync signal input	Used for external vertical sync signal input. This pin enables the internal display operation of the IC in synchronization with vertical sync input provided by the host. Fix this pin at high or low level if no synchronization is required.
NVSYNCO	Output	Internal vertical sync signal output	Used for internal vertical sync signal output. The output is turned on regardless of settings during clock oscillation. This pin is used when the host writes data in synchronization with the internal vertical cycle of the IC.

5.2 Source Driver Output Pins

Signal name	I/O	Function	Description
YR[175:0]	Output	Source driver output	Source driver output of R pixels
YG[175:0]	Output	Source driver output	Source driver output of G pixels
YB[175:0]	Output	Source driver output	Source driver output of B pixels

5.3 Gate Driver/Power Supply IC Control Pins

(GDIOSEL is input into TOP_LCDC; other signals are CORE outputs)

Signal name	I/O	Function	Description
GDIOSEL	Input	Gate driver or power supply IC output selection	Used to enable output pins for the MN863480 (i.e., all the pins explained below will be enabled.) GDIOSEL: High — Enabled pins: CKVL, STVR, NOEVL, XDONL, DDCKL, POLL, VCOMENL, NDDCSL, NDDCSKL, NDDSDAL GDIOSEL: Low — Enabled pins: CKVR, STVR, NOEVR, XDONR, DDCKR, POLR, VCOMENR, NDDCSR, NDDCSKR, NDDSDAR Any signal name ending with L (or R) means that the pin is located on the left-hand side (right-hand side), provided that the chip bump side is upside with all the driver output pins are upside. Disabled pins are fixed at low-level output. Keep them open when using the IC.
CKVL CKVR	Output	Gate driver shift clock	A shift clock output pin for the gate driver to MN863480.
STVL STVR	Output	Gate driver start pulse	A start pulse output pin for the gate driver to MN863480.
NOEVL NOVER	Output	Gate driver output control	An output control pin (active at low level) for MN863480. The assert period is controlled according to the register OEVA and OEVN set values.
XDONL XDONR	Output	Gate driver all ON control	An all ON control pin for MN863480. All gate driver outputs will be ON with the pins set high. The register XDON set value is output as it is.
DDCKL DDCKR	Output	Clock output for power supply IC	A voltage step-up clock output pin for MN863480. The frequency dividing ratio can be set to the set value in the DDCKF register.
POLL POLR	Output	Alternation control	Alternation control pin (MN863480). Used for the toggle control of the opposite electrode. The pin supports line and frame reversion according to the register FRPOL set value.
VCOMENL VCOMENR	Output	Common electrode operation control	Common electrode operation control pin to MN863480. Used to toggle the opposite electrode ON and OFF at the time of line-reversed alternation driving (MN863480). Toggle is OFF if the LCD is not driven during the V blanking period or partially not driven at the time of partial display. The output is always active at the time of frame-reversed alternation.
NDDCSL NDDCSR	Output	Chip select for power supply IC	A chip select for command transfer to MN863480. (Active at low level)
DDSCKL DDSCKR	Output	Serial clock for power supply IC	Serial clock output for command transfer to MN863480. Command transfer will be performed with the register DTRN set to 1. A signal at the cycle of the built-in oscillation clock. The clock signal will be output only at the time of command transfer.
DDSDAL DDSDAR	Output	Serial data for power supply IC	Serial data output for command transfer to MN863480.

5.4 Power Supply and LCD Drive Voltage Input Pins

Signal name	I/O	Function	Description
DV_{DD}	Input	Logic power supply	A logic power supply pin. Supply 2.35 V to 3.6 V.
DV_{SS}	Input	Logic ground	A logic ground pin.
AV_{DD}	Input	Source driver power supply	A source driver power supply pin. Supply 3.5 V to 5.5 V. Connect this pin to the AV_{DD} of the MN863480.
AV_{SS}	Input	Source driver ground	A source driver ground pin.
V_{REFH}	Input	Gradation reference voltage high-level input	Used for the reference voltage input on the high-level side at the time of the gradation voltage generation for the source driver. Supply 3.0 V to 5.0 V (AV_{DD} – 0.5 V). Connect this pin to the V_{REFH} of the MN863480.
V_{REFL}	Input	Gradation reference voltage low-level input	Used for the reference voltage input on the low-level side at the time of the gradation voltage generation for the source driver. Normally ground this pin.
ODV_{DD}	Output	Logic power supply output	Use this pin for input pins fixed at high level.
ODV_{SS}	Output	Logic ground output	Use this pin for input pins fixed at low level.

5.5 Test Pins

Signal name	I/O	Function	Description
TEST1	Input	Test control	Test pin. Fix this pin at low level.
TEST2	Input	Test control	Test pin. Fix this pin at low level.
TEST3	Input	Test control	Test pin. Fix this pin at low level.
TEST4	Input	Test control	Test pin. Fix this pin at low level.
TEST5	Input	Test control	Test pin. Fix this pin at low level.
CKIN	Input	Clock input	A test clock input pin. Fix this pin at low level.
MONITOR1	Output	Output monitoring	A test pin to monitor internal signal. Keep this pin open. (Power supply output for oscillation circuit)
MONITOR2	Output	Output monitoring	A test pin to monitor internal signal. Keep this pin open. (Monitor output for NOEH)

6. Functions

6.1 Host Interface

6.1.1 Interface Mode Selection

(1) RGB Interface

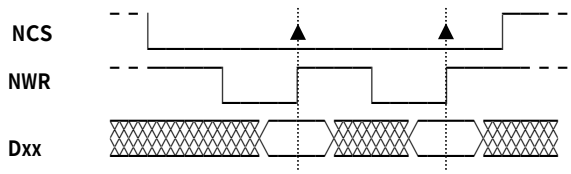
The IC has 80- and 68-series parallel and serial CPU and RGB interfaces as host interfaces. The CPU interface and RGB interface has an independent port each.

The RGB interface or CPU interface's GRAM access is selected by the RMWR bit.

The CPU interface is selected with the RMWR bit set to 0.

The RGB interface is selected with the RMWR bit set to 1.

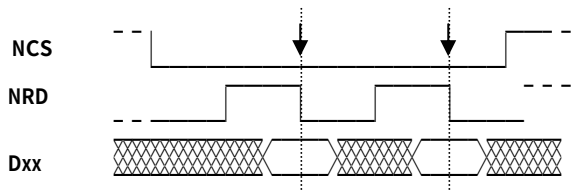
● **80-series CPU interface selected**



※ RMWR bit is set to 0 at the time of GRAM access

Fig. 6.1.1 (1) CPU interface (80 series)

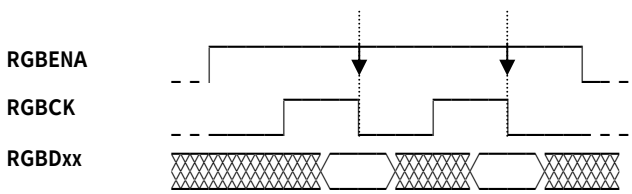
● 68-series CPU interface selected



※ RMWR bit is set to 0 at the time of GRAM access

Fig. 6.1.1 (2) CPU interface (68 series)

● RGB interface selected



※ RMWR bit is set to 1

Fig. 6.1.1 (3) RGB interface

The RGB interface is a GRAM-write-dedicated interface.
As shown in figure 6.1.1 (3), when the RGBENA is set high and the RMWR bit is set to 1, data will be retrieved from the RGBD [17:0] at the falling edge of the RGBCK and only GRAM write access will be implemented.

The RGB interface is not available to command transfer or read access.

Commands are transferred through the parallel or serial CPU interface. If the command (with address 0xh) related to GRAM control is transferred while RGB interface has GRAM access, GRAM data to be written will not be guaranteed. In that case, finish the RGB interface's access first.

To switch from the CPU interface to the RGB interface or vice versa, complete the present access cycle as shown below.

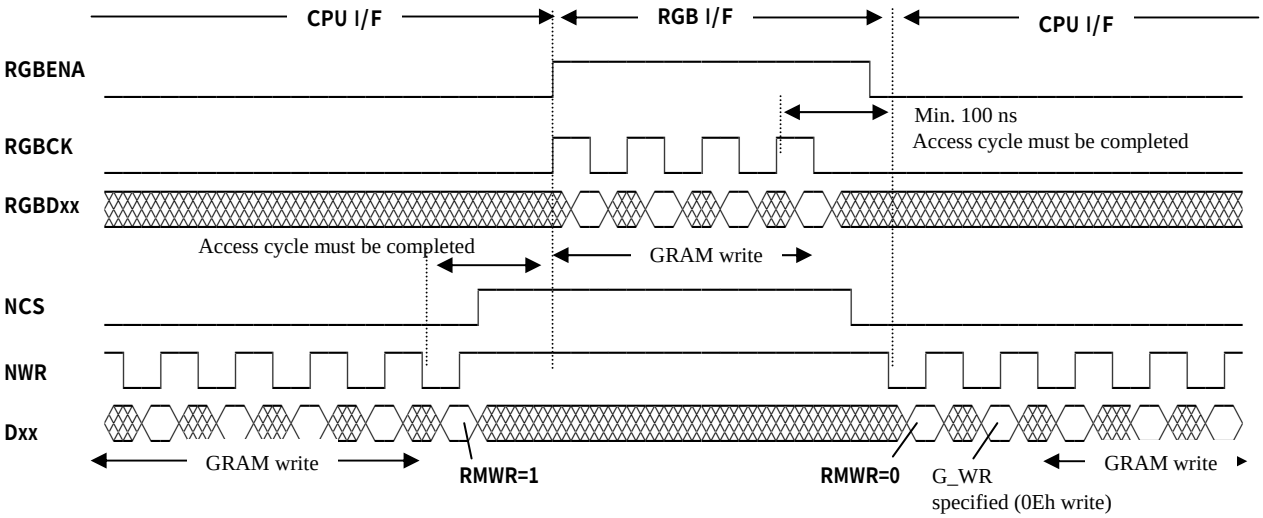


Fig. 6.1.1 (4) Selection of CPU interface or RGB interface (Example: 80-series CPU interface)

Supplement explanation

- The CPU interface's command access is always acceptable without being influenced by the RGBENA pin or RMWR bit. During the RGB interface's GRAM access, however, the transfer of commands related to GRAM control through the CPU interface is prohibited.
- The RGB interface's GRAM access is accepted when the RGBENA is set high and the RMWR bit is set to 1.

At that time, the setting of the GRAM write specify command (with address 0Eh) is not required.

- The GRAM access from the CPU interface will be accepted when the RMWR bit is set to 0 and the GRAM write specify command (with address 0Eh) is set. At that time, the status of the RGBENA pin will be ignored.

(2) CPU Interface

The IC has 80- and 68-series parallel and serial interfaces as host CPU interfaces.
Make the following settings in HOSTYP[1:0] pin.

HOSTYP[1:0]	CPU type	NRD pin	NWR pin	SICK pin	SIDA pin
LL	80-series CPU interface	Read signal (/ RD)	Write signal (/ WR)	Disabled	Disabled
LH	68-series CPU interface	Enable signal (E)	Read/Write specification (R/W)		
HL or HH	Serial interface	Disabled	Disabled	Serial clock	Serial data

(3) Data Bus Width and Interface Settings for GRAM

1) CPU Interface (Parallel Interface only)

- The data pin to be used will be determined by IFMODE[1:0] pin setting.
- The method of data transfer to GRAM is determined by the IFMODE[1:0] pin and GRAM interface setting command RMIF bit in combination.
  (Refer to Section 6.1.5 for the data format in detail.)

IFMODE[1:0]	Mode name	RMIF bit	Data pin used	Number of bits of GRAM transfer data	
LL	18-bit mode	0	D[17:0]	18 bits × 1	260000-color data
LH	16-bit mode	0	D[15:0]	16 bits × 2	260000-color data
		1		16 bits × 1	65000-color data
HL	9-bit mode	0	D[8:0]	9 bits × 2	260000-color data
HH	8-bit mode	1	D[7:0]	8 bits × 2	65000-color data

Notes: • Setting of IFMODE [1:0] and REGMODE would be disabled at serial interface.

2) RGB Interface

- The following settings are made with the RGBIF and RMIF bits of the GRAM interface setting command.
  (Refer to Section 6.1.5 for the data format in detail.)

RGBIF bit	RMIF bit	Mode name	Data pin used	Number of bits of GRAM transfer data	
0	0	18-bit mode	RGBD[17:0]	18 bits × 1	260000-color data
	1	16-bit mode	RGBD[15:0]	16 bits × 1	65000-color data
1	0	6-bit mode	RGBD[5:0]	6 bits × 3	260000-color data
	1	8-bit mode	RGBD[7:0]	8 bits × 2	65000-color data

Notes: • Fix the unused data pins (D** and RGBD**) at low or high level.
- The serial interface with the GRAM is possible only in 65000-color format of 16 bits.
  * Refer to the information in Section 6.1.2 Serial Interface and Section 6.1.5 (5) Data Format in detail.

6.1.2 Serial Interface

The serial interface will be enabled with the HOSTYP [1] set high.
The serial interface uses the SICK pin for serial clock transfer and SIDA pin for data transfer. The serial interface is accessible with the NCS set low, and SIDA data will be retrieved at the rising edge of the SICK clock signal. Data is transferred in units of 17 clocks. The first data is used for data discrimination (i.e., NADS in parallel mode with the REGMODE set high).

(1) Register Access

Register access is implemented as shown below with the first data item of data discrimination set low.

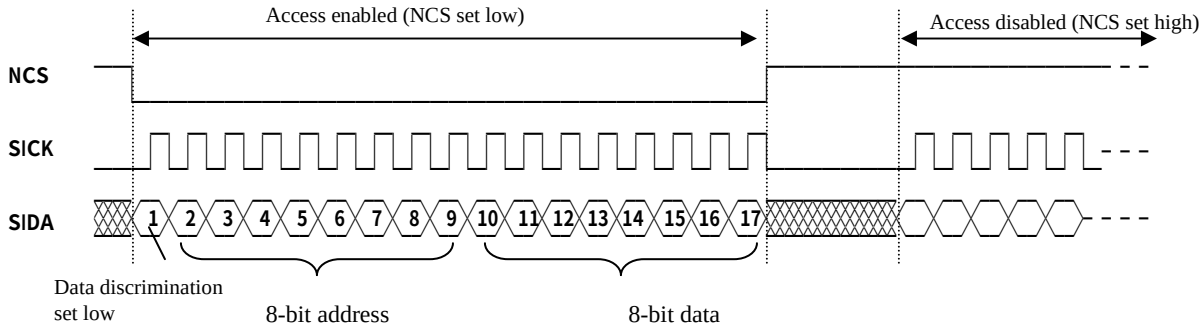


Fig. 6.1.2 (1) Serial Interface Register Access

Note: If the first data item is set high at the time of serial access, the data will be written to the register the address of which is specified then. At that time, the upper 8-bit data will be ignored, and the corresponding data in the above 8-bit data will be written.

(2) GRAM Access

At the time of GRAM access, set the GRAM write command (with the address 0Eh) and set the first data item of data discrimination high as shown below.
At the time of GRAM access through the serial interface, only the 65k-color (16-bit) data format will be used.

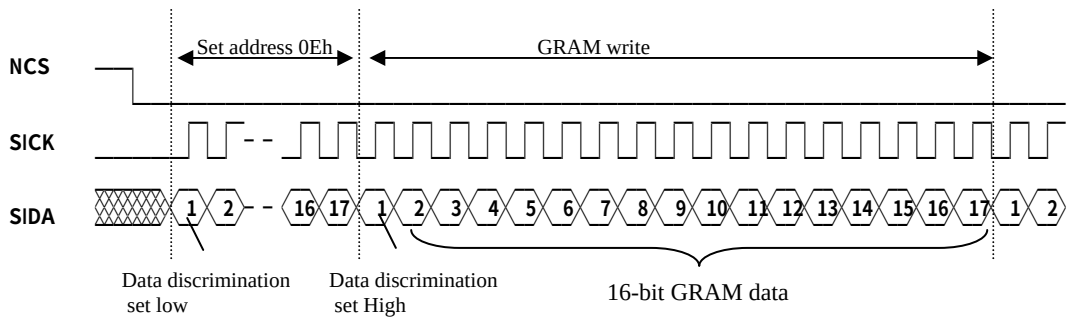


Fig. 6.1.2 (2) Serial Interface GRAM Access

6.1.3 Data Discrimination

At the time of access to the internal registers and GRAM through the CPU parallel interface, execute the write command with the NADS set low, and specify the address (at the address set cycle). Execute the write command with the NADS set high next and write the data (at the data cycle).
Written data is discriminated by the NADS pin as follows:

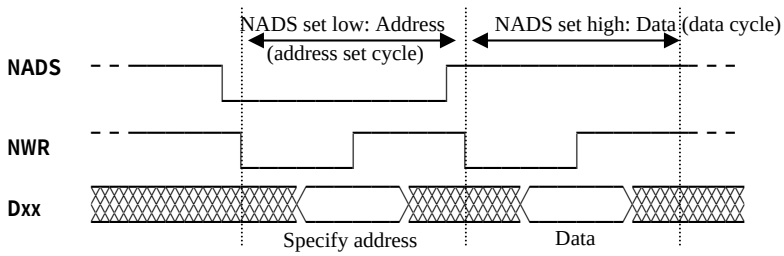


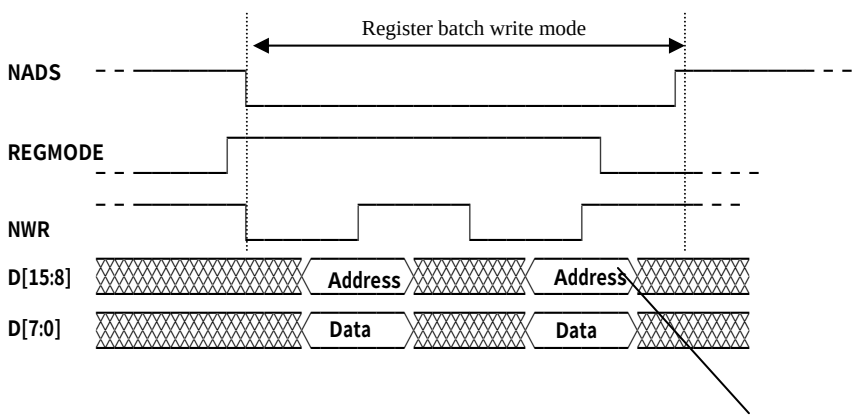
Fig. 6.1.3 Data discrimination (write operation) in CPU interface mode.

As explained in 6.1.2, the first data item in serial interface mode is used to discriminate between data of address-set type and that of data-set type.

6.1.4 Register Write Mode

In CPU interface mode, data write accesses to registers are classified into two types (address-set and data-set cycles) as specified in section 6.1.3.
In 18- or 16-bit interface mode, an address uses the upper 8 bits and data uses the lower 8 bits to be transferred per cycle.
This mode (hereafter called batch write mode) will be enabled with the REGMODE pin set high. Batch write will be executed at the address set cycle (with the NADS set low).

Note 1) Fix the REGMODE pin at high or low level.
Note 2) In 8- or 9-bit interface mode, set the REGMODE to low.
Note 3) This mode will be enabled only at the time of register access. When GRAM write is specified (with the address 0Eh), the lower 8-bit data will not be written to the GRAM.



No data will be written in the case of addresses (0Eh and 0Fh) specifying access to the GRAM.

Fig. 6.1.4 Register Batch Write Mode

6.1.5 Data Format

(1) CPU Interface: 18-bit Mode (HOTYP[1] Set to 0, IFMODE[1:0] Set to 00, and RMWR Bit Set to 0)

1) Image Data

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

2) Command Data

- Batch Write Mode (REGMODE Set High)

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

- 8-bit Write Mode (REGMODE Set Low)

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address cycle	-	-	-	-	-	-	-	-	-	-	A7	A6	A5	A4	A3	A2	A1	A0
Data cycle	-	-	-	-	-	-	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

3) GRAM Write with REGMODE Set High

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address cycle	-	-	A7	A6	A5	A4	A3	A2	A1	A0	-	-	-	-	-	-	-	-
Data cycle	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Note: Set 0 to the RMIF when this mode is used. If the RMIF is set to 1, read data for R0/B0 display will be in reverse control according to RLSB/BLSB bit settings.

(2) CPU Interface: 16-bit Mode (HOTYP[1] Set to 0, IFMODE[1:0] Set to 01, and RMWR Bit Set to 0)

1) Image Data

[RMIF=0]

• BODR=0

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R5	R4
2nd cycle	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

• BODR=1

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2
2nd cycle	B1	B0	-	-	-	-	-	-	-	-	-	-	-	-	-	-

[RMIF=1]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

2) Command Data

• Batch Write Mode (REGMODE Set High)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

• 8-bit Write Mode (REGMODE Set Low)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address cycle	-	-	-	-	-	-	-	-	A7	A6	A5	A4	A3	A2	A1	A0
Data cycle	-	-	-	-	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

3) GRAM Write with REGMODE Set High

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address cycle	A7	A6	A5	A4	A3	A2	A1	A0	-	-	-	-	-	-	-	-

Data cycle

[RMIF=0]

• BODR=0

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R5	R4
2nd cycle	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

• BODR=1

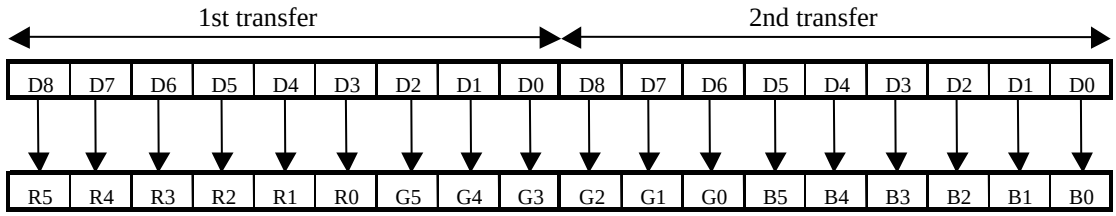
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2
2nd cycle	B1	B0	-	-	-	-	-	-	-	-	-	-	-	-	-	-

[RMIF=1]

R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1

(3) CPU Interface: 9-bit Mode (HOTYP[1] Set to 0, IFMODE[1:0] Set to 10, and RMWR Bit Set to 0)

1) Image Data

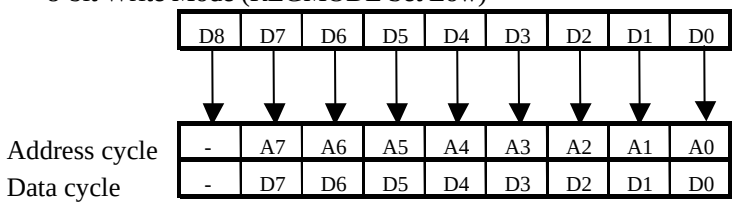


2) Command Data

- Batch Write Mode (REGMODE Set High)

  Use prohibited

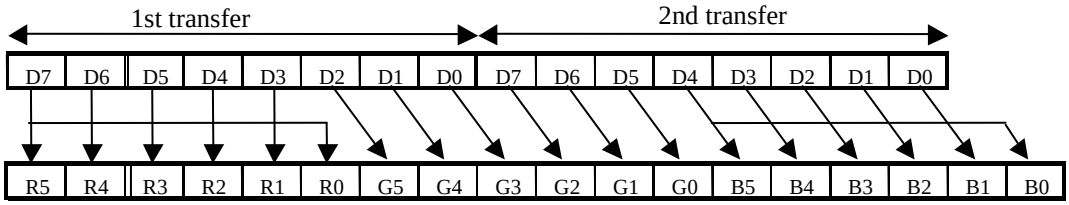
- 8-bit Write Mode (REGMODE Set Low)



Note: Set 0 to the RMIF when this mode is used. If the RMIF is set to 1, read data for R0/B0 display will be in reverse control according to RLSB/BLSB bit settings.

(4) CPU Interface: 8-bit Mode (HOTYP[1] Set to 0, IFMODE[1:0] Set to 11, and RMWR Bit Set to 0)

1) Image Data

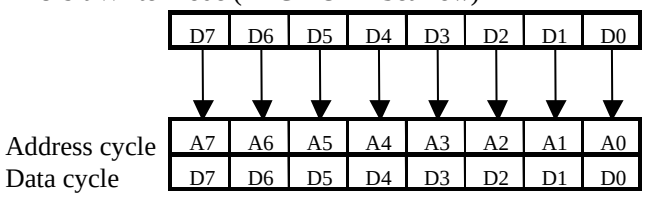


2) Command Data

- Batch Write Mode (REGMODE Set High)

  Use prohibited

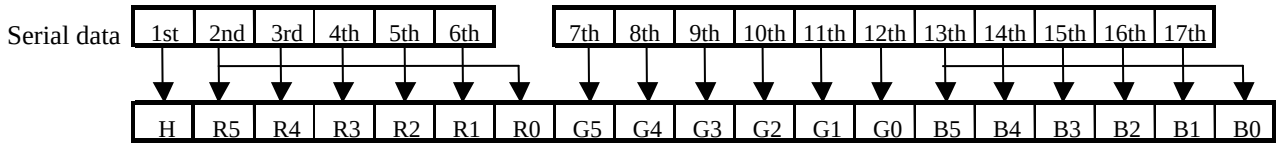
- 8-bit Write Mode (REGMODE Set Low)



Note: Set 1 to the RMIF for the reverse control of read data for R0/B0 display with RLSB/BLSB bit settings in this mode.
(If RMIF is set to 0, the reverse control of read data for R0/B0 display with RLSB/BLSB bit settings will not be possible.)

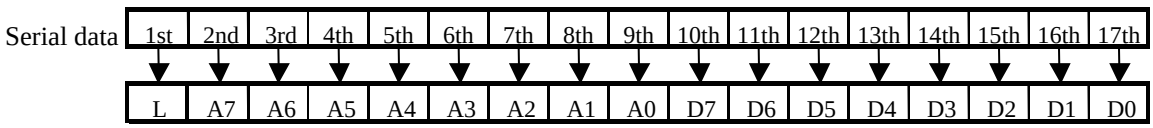
(5) Serial Interface (HOSTYP[1] Set to 1 and RMWR Bit Set to 0)

1) Image Data

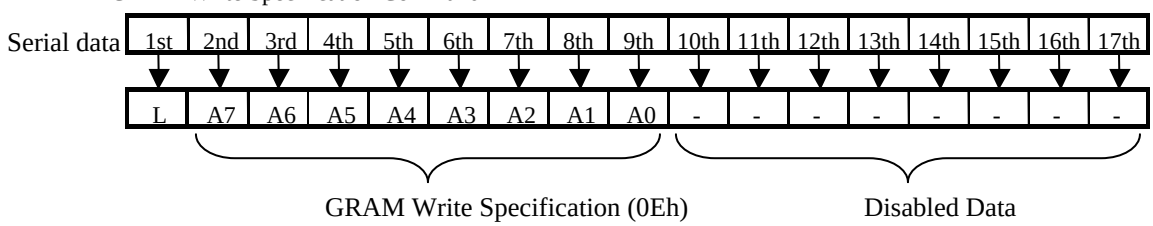


2) Command Data

- Other than GRAM Write Specification Command



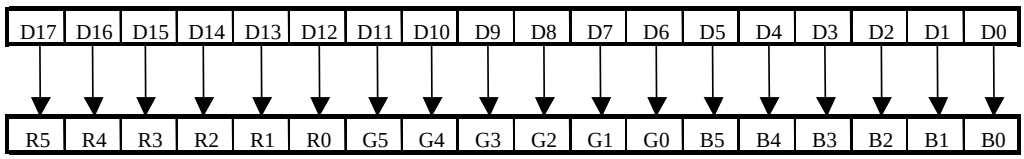
- GRAM Write Specification Command



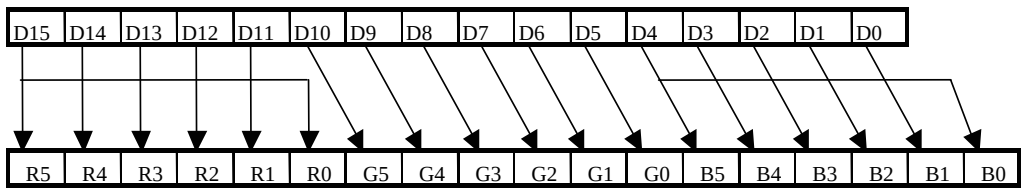
Note: Set 1 to the RMIF for the reverse control of read data for R0/B0 display with RLSB/BLSB bit settings in this mode.
(If RMIF is set to 0, the reverse control of read data for R0/B0 display with RLSB/BLSB bit settings will not be possible.)

(6) RGB Interface (RMWR Bit Set to 1)

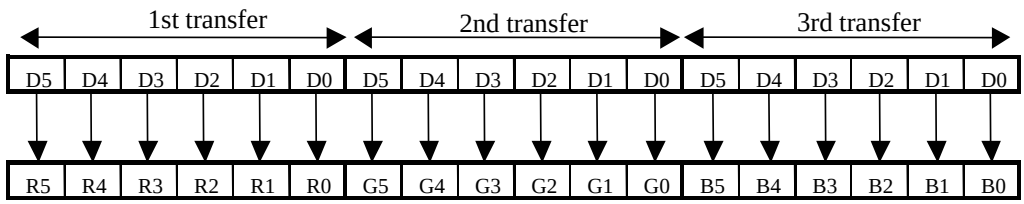
1) RGB Interface: 18-bit Mode (RGBIF Bit Set to 0 and RMIF Bit Set to 0)



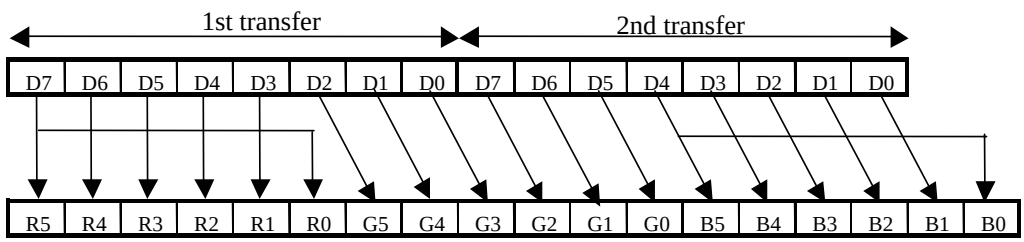
2) RGB Interface: 16-bit Mode (RGBIF Bit Set to 0 and RMIF Bit Set to 1)



3) RGB Interface: 6-bit Mode (RGBIF Bit Set to 1 and RMIF Bit Set to 0)



4) RGB Interface: 8-bit Mode (RGBIF Bit Set to 1 and RMIF Bit Set to 1)



6.1.6 Sequence

(1) GRAM Write Access

As shown in figure 6.1.6 (1), GRAM write access is performed at the address set cycle (for GRAM write specification) and the data cycle.

[Explanation of Write Operation]

1) First, specify GRAM write (0Eh) at the address set cycle with the NADS set low.
   The address counter will be initialized at the rising edge of the NWR signal.
2) Execute GRAM write at the data cycle with the NADS set high.
   - Write will be executed at the rising edge of the NWR signal. Simultaneously, address count will be executed.
3) Hereafter, addresses will be automatically counted and write will be executed in the case of continuous access.
4) If the address set cycle is executed with the NADS set low during continuous access, GRAM access will be interrupted. To execute GRAM write again, take step 1) and specify GRAM write again.
   * The above is an explanation of the 80-series CPU interface at the rate of single transfer cycle per pixel.

[Relationship with Interface Mode]

- GRAM address management is performed in units of pixels (18 bits).
- In 16-bit, 260000-color mode, 8-bit mode, or 9-bit mode, a single pixel is transferred with two accesses.
- If two accesses are required to transfer each pixel, do not interrupt the access while the pixel is being transferred, otherwise write will not be executed.

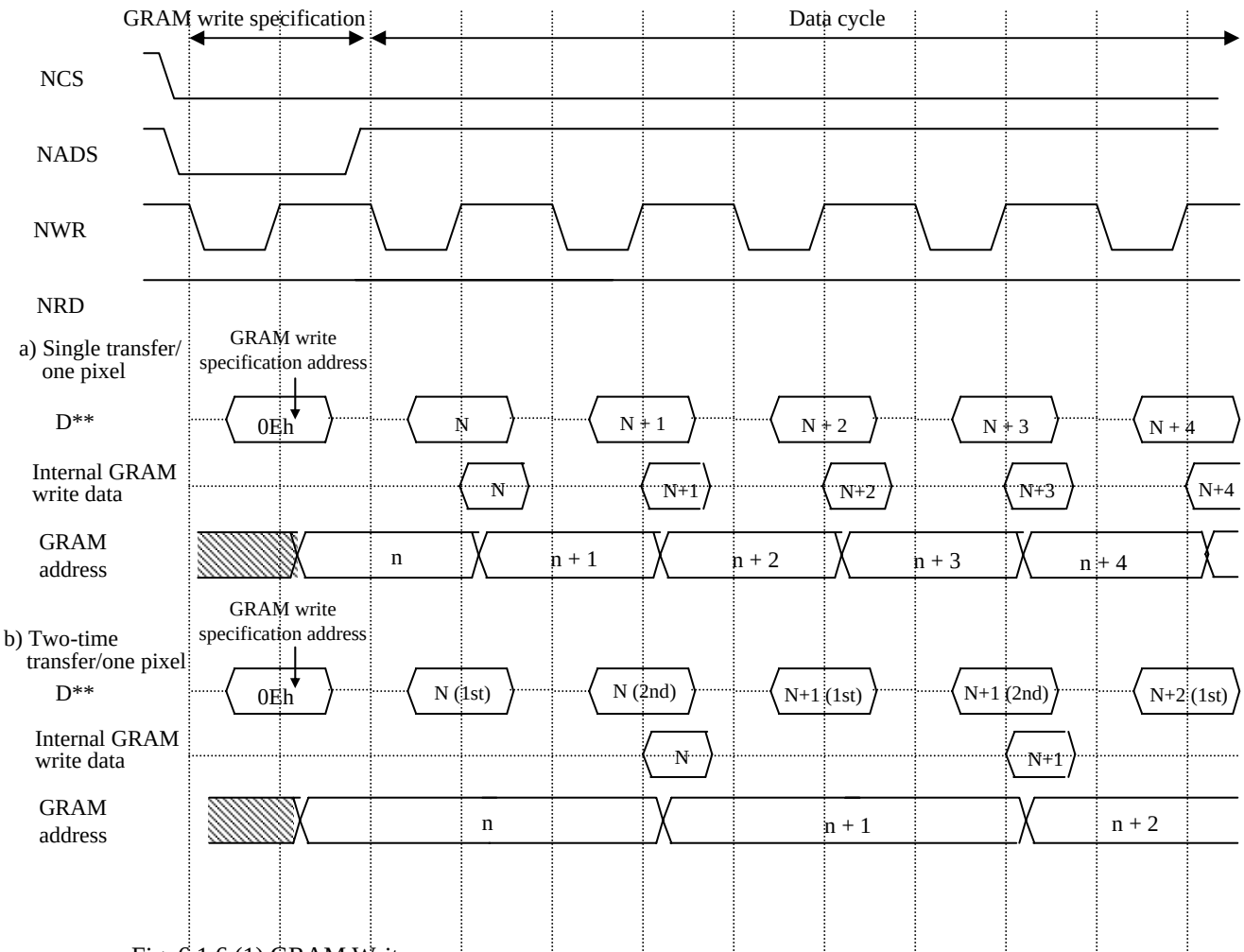


Fig. 6.1.6 (1) GRAM Write

(2) GRAM Read Access

As shown in figure 6.1.6 (2), GRAM read access is performed at the address set cycle (for GRAM read specification) and the data read cycle.
The first read data is dummy read data. The desired data will be read at and after the second read command executed.

[Explanation of Read Operation]

1) First, specify GRAM read (0Fh) at the address set cycle with the NADS set low.
   The address counter will be initialized at the rising edge of the NWR signal.
2) Execute GRAM read with the NADS set high and the NRD signal asserted.
   - At the falling edge of the NRD signal at the first data cycle, dummy data will be read.
   - The IC will internally execute the read command from the GRAM to the internal bus at the rising edge of the NRD signal.
   - The desired data will be read at the falling edge of the NRD signal at and after the second read command executed.
3) Hereafter, addresses will be automatically counted and read will be executed repeatedly in the case of continuous access.
4) If the address set cycle is executed as a write access with the NADS set low during continuous access, GRAM access will be interrupted. To execute GRAM read again, take step 1) and specify GRAM read again.
   * The above is an explanation of the 80-series CPU interface at the rate of single transfer cycle per pixel.

[Relationship with Interface Mode]

- GRAM address management is performed in units of pixels (18 bits).
- In 16-bit, 260000-color mode, 8-bit mode, or 9-bit mode, a single pixel is transferred with two accesses.
- If two accesses are required to transfer each pixel, do not interrupt the access while the pixel is being transferred.

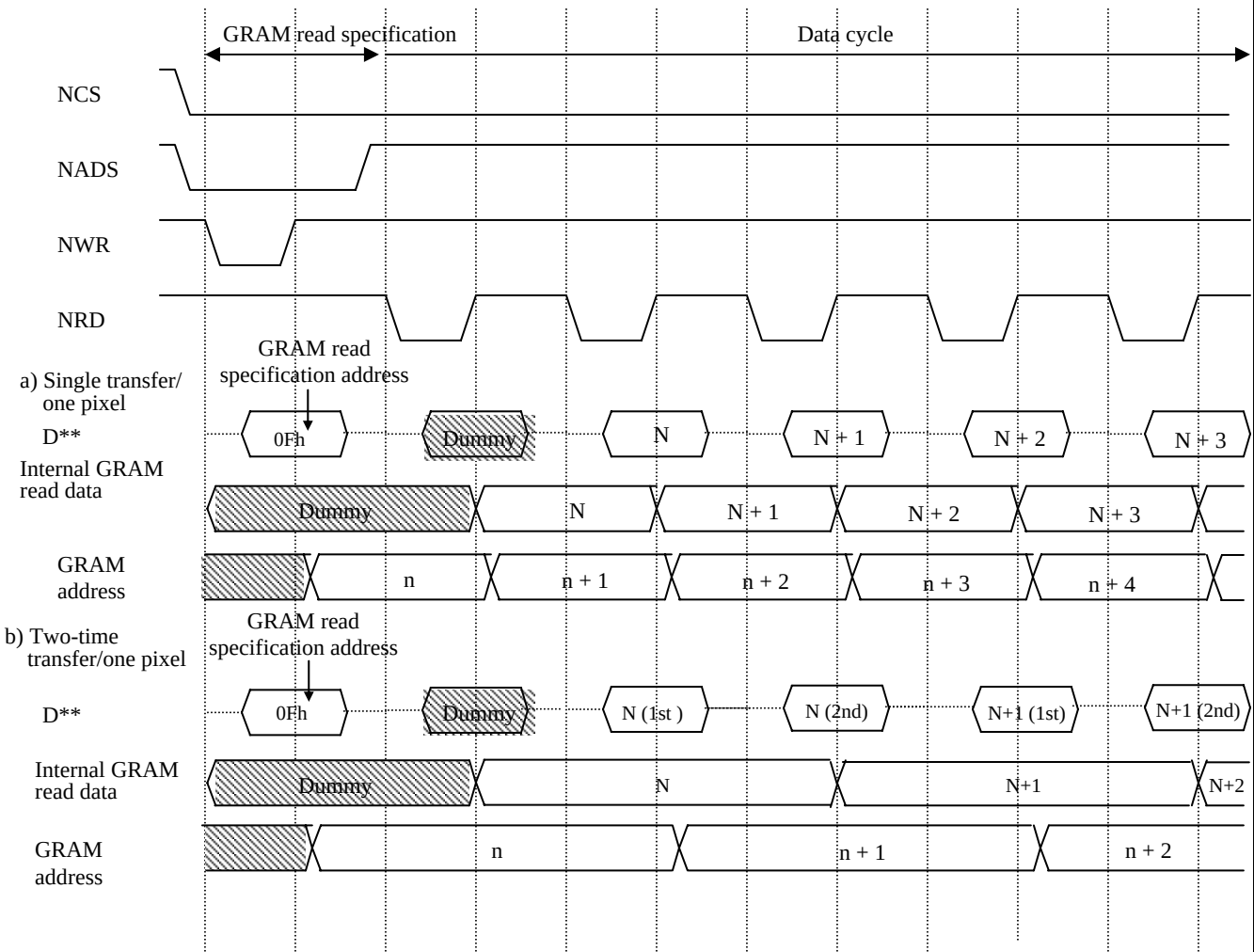


Fig. 6.1.6 (2) GRAM Read

(3) Register Access

1) Register Write

As explained in section 6.1.3 and section 6.1.4, the following two types of access methods are available. See these sections for details.

- 8-bit access mode, in which registers are accessed at the address set cycle and data write cycle.
- Register batch write mode, in which data is written with each address simultaneously at address set cycle.

2) Register Read

【REGMODE set low】

1) The target register is specified at the address set cycle with the NADS set low.

2) The NRD signal is asserted with the NADS set high and the read command is executed.

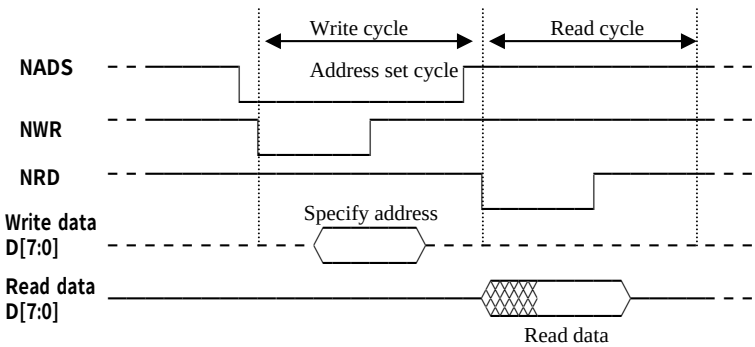


Fig. 6.1.6 (3) Register Read (REGMODE set low) (80 series)

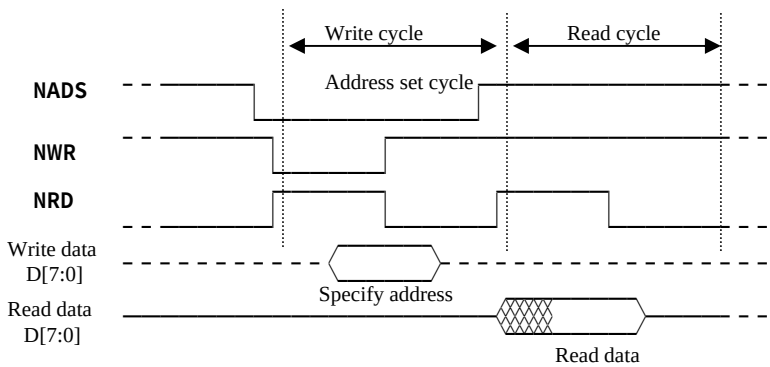


Fig. 6.1.6 (4) Register Read (REGMODE set low) (68 series)

【 REGMODE set high 】

If the REGMODE is fixed at high level, data will be simultaneously written when the target register is specified at the address set cycle.

Therefore, the address register (80h) is prepared for address setting. Execute the following steps.

1) Specify the address 80h with the NADS set low. Then write data on the address of the register to be specified to the address register.
2) Assert the NRD signal and execute the read command at the data cycle.

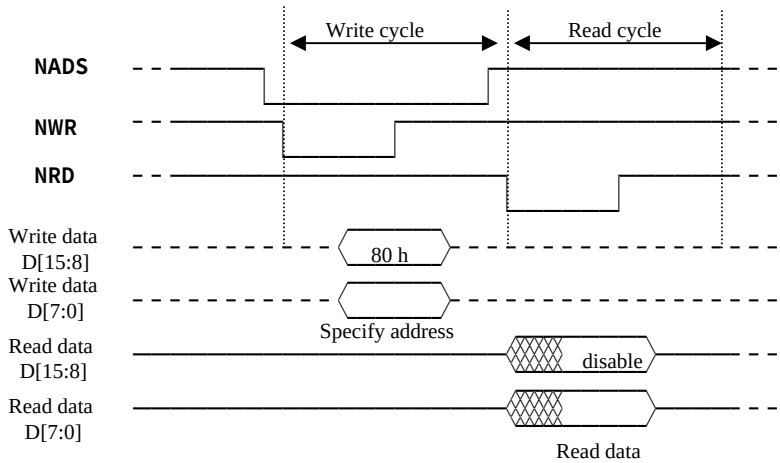


Fig. 6.1.6 (5) Register Read (REGMODE set high) (80 series)

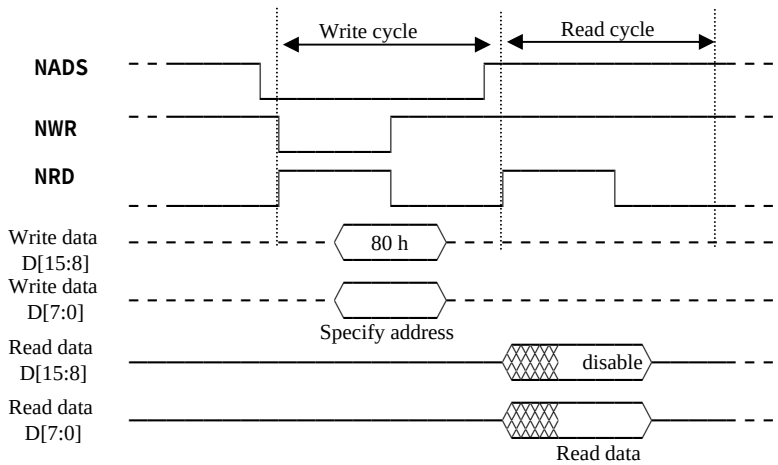


Fig. 6.1.6 (5) Register Read (REGMODE set high) (68 series)

6.2 GRAM (Graphic RAM)

6.2.1 GRAM Configuration

This IC has a built-in 760320-bit (176 × 18-bit RGB × 240) GRAM to store LCD data.
Each bit of the GRAM corresponds to each dot of the LCD to display data in a bitmap format.
Each pixel consists of 18 bits (6 bits each for RGB). The host specifies X and Y addresses to gain access pixel by pixel.
The source driver that drives the LCD panel reads data line by line at the horizontal cycle independent from the host's access to the GRAM. This is called display read. Display read is controlled by line addresses.
The GRAM physically fully corresponds to the source driver output circuit. Therefore, the enabled range of the GRAM as shown below will be enabled by the output pins of the source driver in use. Access to areas outside the GRAM's enabled range will be executed but not reflected on the output of the source driver.
The line address maximum value to be read will vary with the number of set outputs (GSL[2:0] bits) of the gate driver.

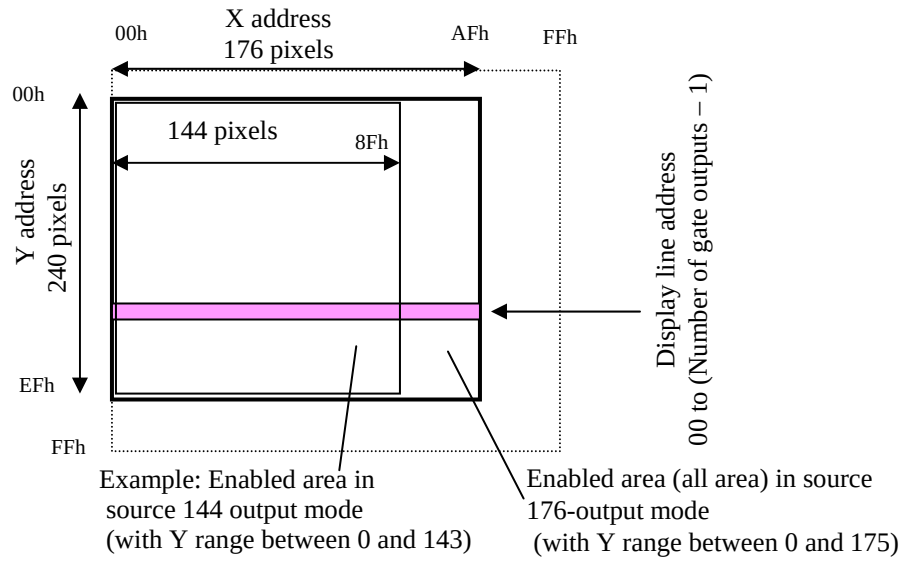


Fig. 6.2.1 GRAM Configuration

6.2.2 GRAM Address

X and Y addresses will specify each pixel when the host gains access to the GRAM.
When the read command is executed, line addresses specify each line.
The following graph shows the relationship of the X and Y addresses of the GRAM, source driver outputs, and line addresses with display read executed.

		X address											
SDIR	0	0	1	2	3	4	···	170	171	172	173	174	175
	1	175	174	173	172	171	···	5	4	3	2	1	0

Y address	Line address
0	0
1	1
2	2
·	·
·	·
·	·
237	237
238	238
239	239

Source Driver Output													
	YR	0	1	2	3	4	···	170	171	172	173	174	175
	YG												
	YB												

(※) Each address is described in decimal for convenience.

Fig. 6.2.2 GRAM Addresses

6.2.3 GRAM Address Control Function

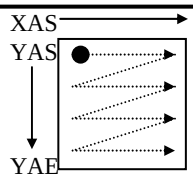
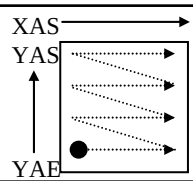
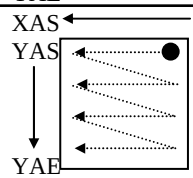
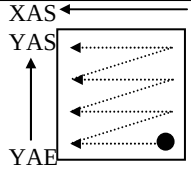
The IC has the following address control functions. It achieves display according to mounting direction of the LCD panel and variety of display in which, vertically and horizontally, upside down, or right and left reverse. Settings are made on each bit of the memory operation mode register.

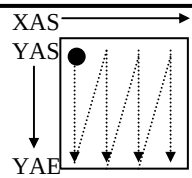
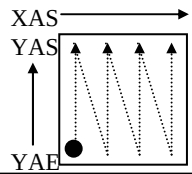
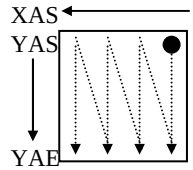
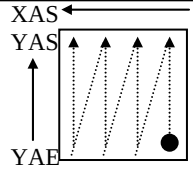
Function	Control bit	Setting
Address count direction control (Within access assignment area)	ADIR	0: Address count in the direction of X 1: Address count in the direction of Y
X address increment direction (Within access assignment area)	XDIR	0: Normal (address increase from start point) 1: reverse (address decrease from end point)
Y address increment direction (Within access assignment area)	YDIR	0: Normal (address increase from start point) 1: Reverse (address decrease from end point)
Source driver shift direction (Driver output pin at X address at 0 to 175)	SDIR	0: Normal (Driver output shift direction Y[R,G,B]00 to 175) 1:Reverse (Driver output shift direction Y[R,G,B]175 to 00)

★Notice This function is used when the data is written to the GRAM. Therefore it should be set before the GRAM is written. Otherwise the setting will not become effective.

■ Address Increment control function：XDIR,YDIR,ADIR

The following table shows each setting and the condition of GRAM address count.

ADIR	XDIR	YDIR	Schematic diagram
0	0	0	
		1	
	1	0	
		1	

ADIR	XDIR	YDIR	Schematic diagram
1	0	0	
		1	
	1	0	
		1	

The dot (●) in each diagram shows the start point.

Fig. 6.2.3 (1) GRAM Address Count

■ Source driver shift direction control (Control relations X address and driver output)：SDIR

To assign source driver output and GRAM X address relations.

- At "0", GRAM (X address "0" to "175") correspond to source driver output ("0" to "175").
- At "1", GRAM (X address "0" to "175") correspond to source driver output ("175" to "0").

Herewith, it can set address "00h" (X direction) position depending on driver packaging direction.

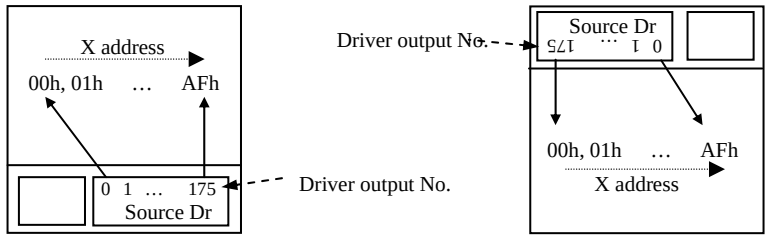


Fig 6.2.3 (2) Source driver shift direction setting

6.2.4 GRAM Access Control

(1) GRAM Access Operation

By specifying the size of the rectangular access area of the GRAM from the host, gaining access to the specified area in the GRAM for writing or reading data will be possible.

In the case of continuous access, automatic address count will start in the specified area in address count mode as specified in Section 6.2.3.

Address count will stop when the end address is reached.

Therefore, address initialization is required whenever a single screen is refreshed.

Address initialization is performed in the following cases.

1) CPU interface mode: When GRAM write command (0Eh) or GRAM read command (0Fh) is executed.
2) RGB interface mode: When the external vertical sync signal is input.

(2) Specifying GRAM Access Range

The following two methods are available. The AEMODE bit is used for mode selection.

1) When AEMODE is set to 0:

The starting point of the access range is specified by XAS and YAS and the end address is specified by XAE and YAE as shown in figure 6.2.2 (2). Address count is performed in the method explained in Section 6.2.3.

XDIR set to 0: Increasing from XAS to XAE

XDIR set to 1: Decreasing from XAE to XAS

Note 1) XAS must be the same or less than XAE while YAS must be the same or less than YAE.

2) When AEMODE is set to 1:

The starting point of the access range is specified by XAS and YAS and the access width is specified by XAE and YAE as shown in figure 6.2.2 (3).

Set the access width minus 1 for XAE and YAE. Set 0 when gaining access to a single pixel only.

Address count is performed in the method explained in section 6.2.3.

XDIR set to 0: Increasing from XAS to XAS+XAE

XDIR set to 1: Decreasing from XAS+XAE to XAS

Note 2) In both cases, X addresses must be within the GRAM area corresponding to the available output range of the source driver while Y addresses must be between 00 and EFh.

* If the conditions in Note 1 or Note 2 are not satisfied, the GRAM write command cannot be executed normally. When writing one dot, set both XAE and YAE to 00h.

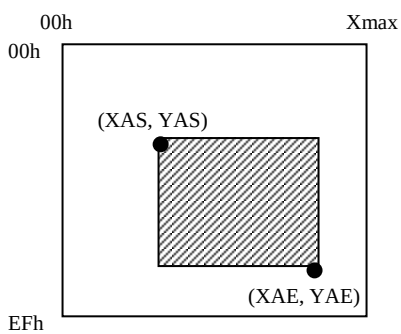


Fig. 6.2.4 (1) AEMODE=0

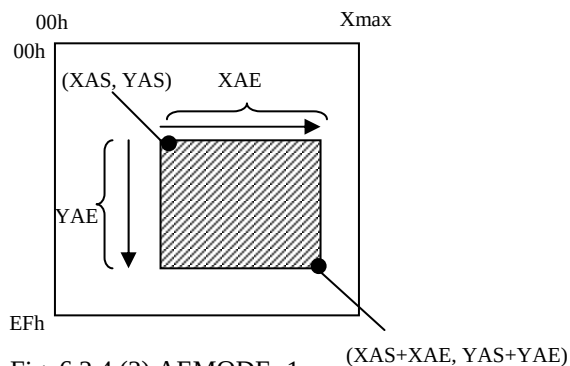


Fig. 6.2.4 (2) AEMODE=1

6.2.5 GRAM Data Mask Function (WDMSK Pin)

This IC has a function to mask GRAM write data in units of pixels or bits and a window area can be specified.

(1) Write Data Mask Function in Units of Pixels (WDMSK Pin)

Write data masking is possible with the WDMSK pin set high at the time of GRAM write access. In this case, address count will be performed normally.

If multiple data access modes (including the serial interface mode) are used to execute GRAM write, the whole data area including the final access cycle needs to be masked.

Write mask is not executed if only a cycle other than the final access is masked. (See figure 6.2.5 (2) and (3))

Note: The function of this pin is available while execute RAM clear, too.

During RAM clear execution, WDMSK pin = L is required.

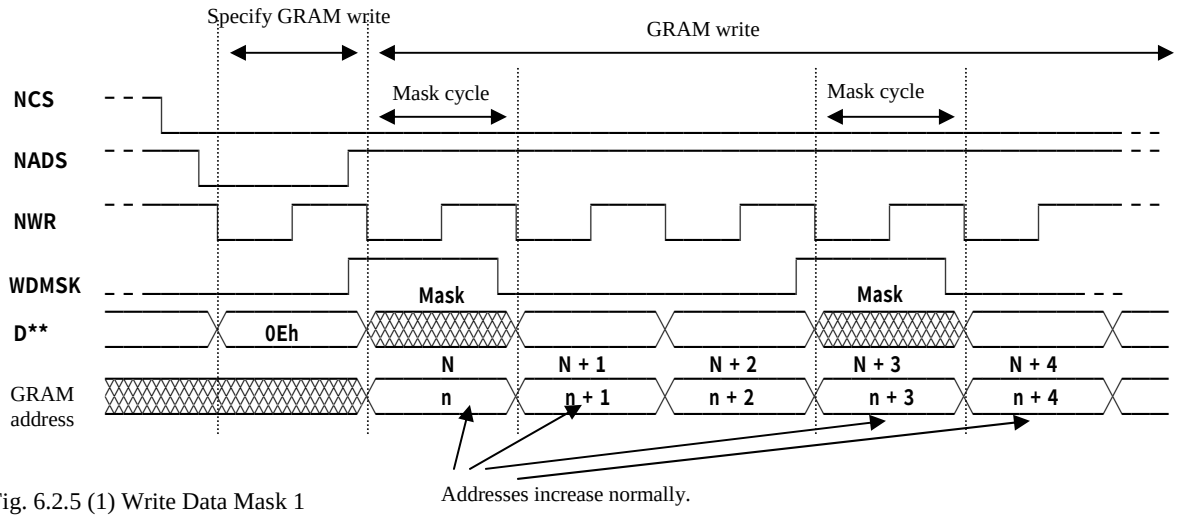


Fig. 6.2.5 (1) Write Data Mask 1

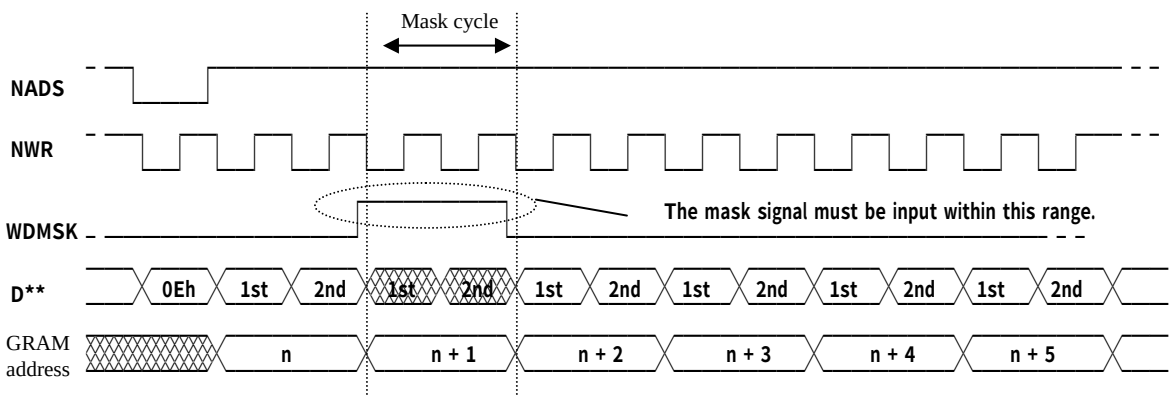


Fig. 6.2.5 (2) Write Data Mask 2

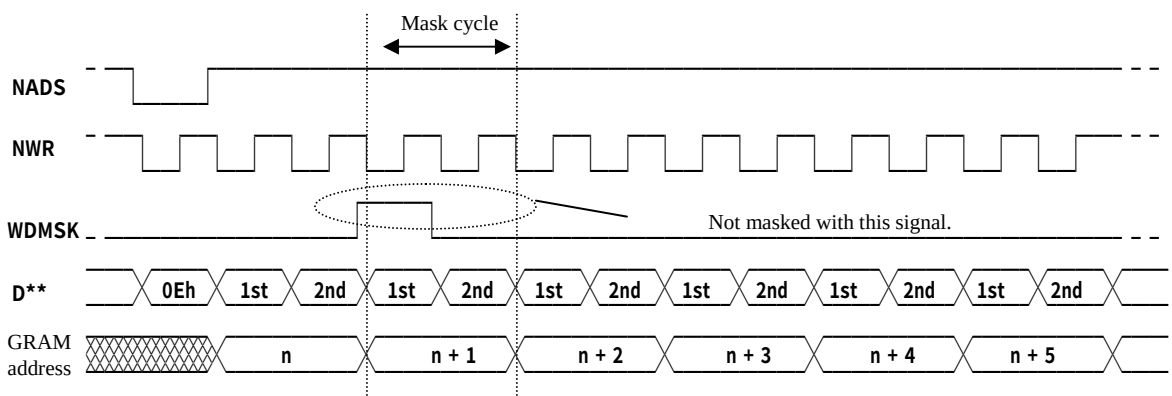
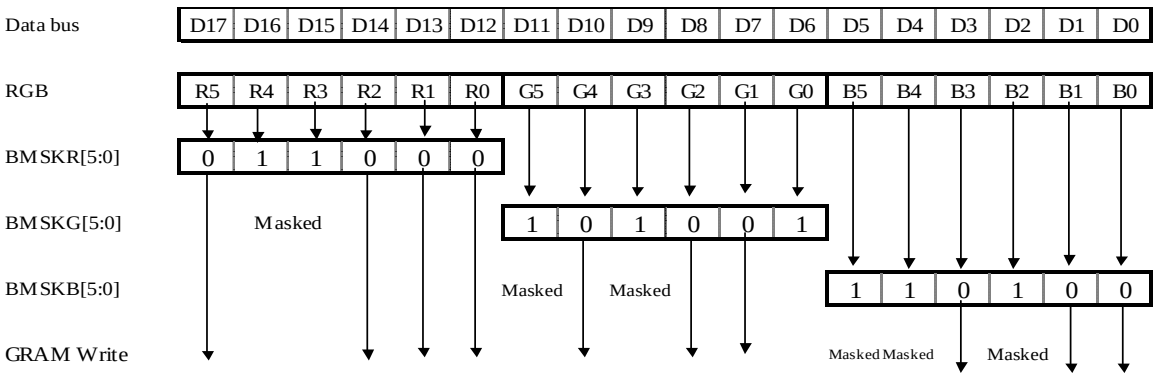


Fig. 6.2.5 (3) Not write data masked

(2) Bit Mask Function

By setting the command register BMSK* bit when writing GRAM data, the GRAM write data will be masked in units of bits.
Bit mask control can be set in units of R, G, and B bits independently.
The following example is a bit mask example with the IFMODE[1:0] set to 00 (at the time of 260000-color, 18 bits × single access)



No RGB data of masked bits will be written to the RAM when the BMSK* bit of the control command is set to 1.

Fig. 6.2.5 (4) Bit Mask

(3) Window Mask Function

When writing data to the GRAM, the write data within and outside the specified window on the LCD will be masked.
The window is specified by the mask area's X and Y start addresses (WMXS and WMYS) and end addresses (WMXE and WMYE).
With the WMMODE register is set to 0, the area within the window will be masked. With the WMMODE register is set to 1, the area outside the window will be masked.
Note 1) The window mask area needs to be set inside the GRAM access area. See Section 6.2.4 (2).
Note 2) Do not reverse the magnitude relation between the start and end addresses.
i.e., XAS ≤ WMXS ≤ WMXE ≤ XAE (AEMODE is set to 0 in this example)
YAS ≤ WMYS ≤ WMYE ≤ YAE (AEMODE is set to 0 in this example)
Note 3) The borderline of the specified window will be masked only when the WMMODE is set to 0.

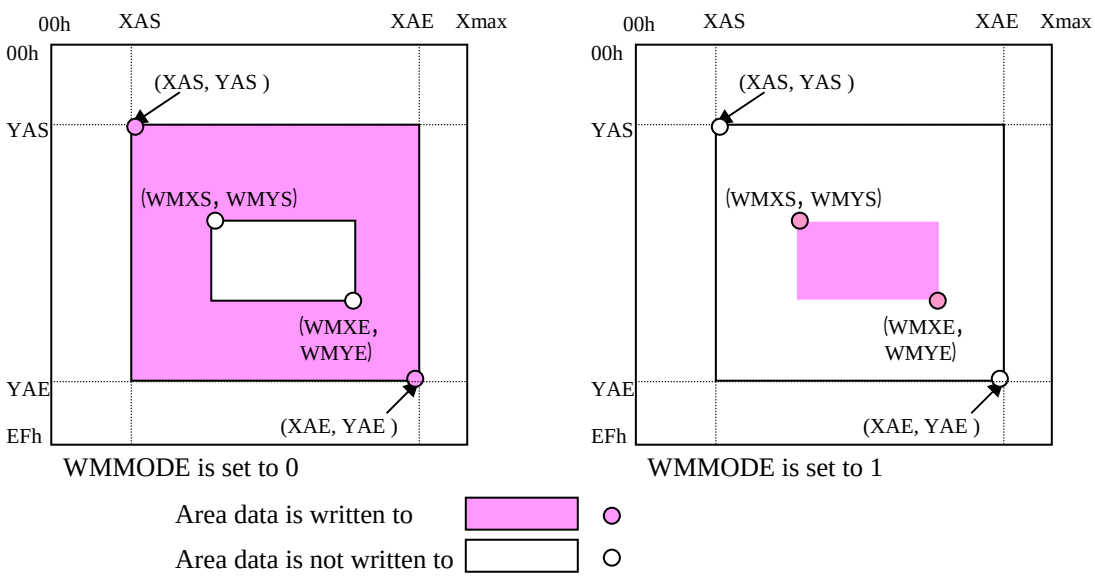


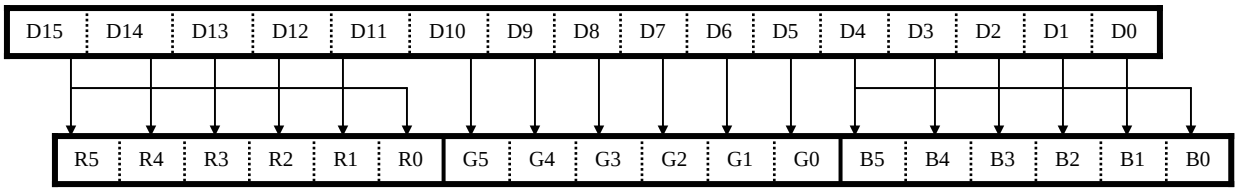
Fig. 6.2.5 (5) Window Mask

* The write data mask function (WDMSK pin), the bit mask function, and window mask function can be used together. Each mask function will be in OR-process.

6.2.8 Gradation LSB Generation Function (in 65000 Colors)

This IC displays gradation with pixels, each of which has 18 bits (consisting of six R bits, six G bits, and six B bits).
In 65000-color interface mode (with the RMIF bit set to 1), data from the host will be provided in blocks of 16 bits (five R bits, six G bits, and five B bits). The LSB of the R signal and that of the B signal are generated with the R5 MSB data and B5 MSB data used. See below.

(1) Write Data to GRAM

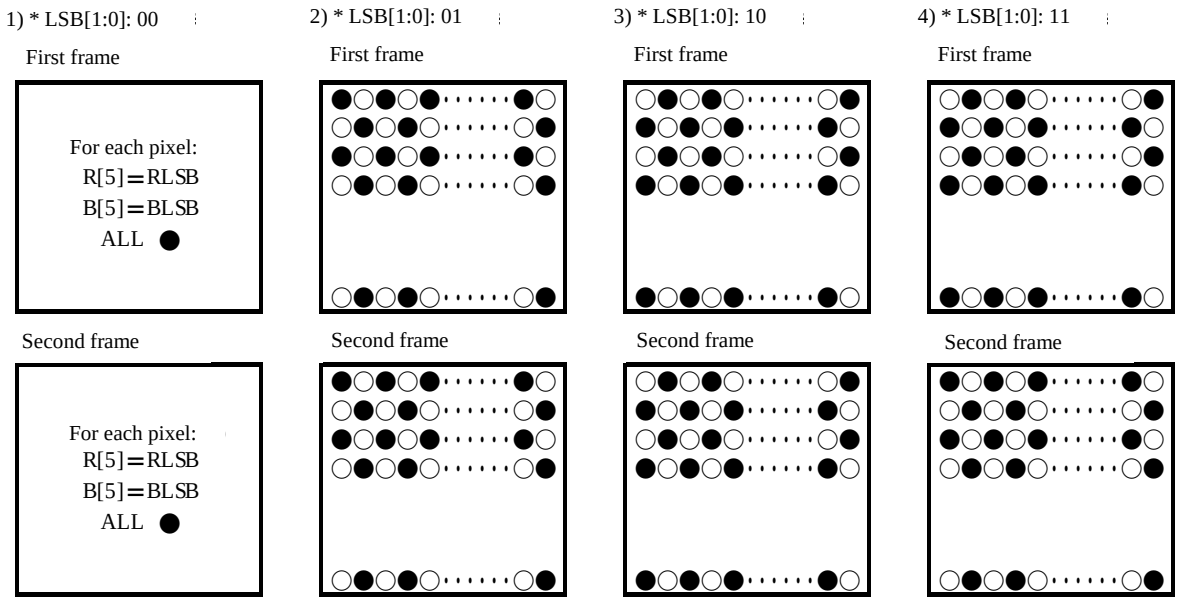


(2) Display Read Data Control

The following diagrams show the status of the RLSB or BLSB.
The following display data will appear according to RLSB[1:0] and BLSB[1:0] bit settings based on the data written to the RAM in 1).

●: GRAM data is output as it is.
○: GRAM data is reversed and output.

Note: 1. Data processing is enabled when the RMIF bit is set to 1.
2. Data processing is executed before alternation. Data after alternation shows processed alternation data.



●: GRAM data is output as it is.
○: GRAM data is reversed and output.

6.2.9 Display Data Reverse Function

With a command register DISPINV bit setting, displayed read data will be reversed and output from the GRAM.
With the DISPINV set to 1, data reversion will be executed. This will be processed at the final output stage of the source driver after the displayed data is latched as explained in Section 6.2.7. Therefore, GRAM data is not influenced.
Display data is reversed according to the results of digital brightness adjustment (see Section 6.3.4) and gradation LSB image processing.
The display data reverse function is not available to the display all white command (see Section 6.3.1) or refresh white display. The LCD panel will be displayed all white in that case.
The function supports negative and positive reversed display and LCD display modes (normally white and normally black modes).
In normally black mode, the black and white polarities will be completely reversed. Therefore, the LCD panel will be displayed all black at the time of whole screen white display or refresh white display.
With the DISPINV set to 0, the LCD display will be in normally white mode.

6.2.6 GRAM Clear Function

The IC has a GRAM clear function. RAM data will be automatically set to 1 and 0 by setting the RAMCLR bit to 1.

At that time, RGB data can be all set to 1 or 0 by the CLR_COL bit setting.
Furthermore, the access area specification, window mask function, and bit mask function can be used together.
The RAM is cleared by using the clock of the built-in oscillation circuit (at 206.6 kHz). It required at maximum approx. 200 ms (i.e., 176 × 240 × 1/206.6 kHz) to clear the whole screen.
This RAM clear time is determined by the GRAM access specification range.
After clearing the RAM, the RAM_CLR bit will be automatically cleared and set to 0.
The operation in process will be canceled if the host sets 0 to the bit during clearing.
Note 1: Do not execute GRAM access while the RAM is being cleared, otherwise the GRAM value will not be guaranteed.
Note 2: During RAM clear execution, WDMSK pin = L is required. In this case, if WDMSK = H, Data mask function will active and content of GRAM are not updated.

6.2.7 Display Read Function

(1) Display Data Latch

The stored display data in the GRAM is transferred to the latch circuit at the rate of one line per horizontal cycle and provided to the source driver. The display read operation is independent from the Host's access. Therefore, there will be no access limits imposed on the host.

(2) Display Line Address

The GRAM display read operation is managed by line addresses.
The first line on the LCD and the address of the display start line are set by the command setting.
Line addresses are counted from the address of the display start line and the count automatically increases at 1H intervals.
The number of displayed lines in the Y direction can be set to 192, 220, or 240 (with the GSL[2:0] bit to set the number of gate driver outputs).
The line address count will return to 00h (i.e., the display start line) when all the addresses corresponding to the number of displayed lines are counted.

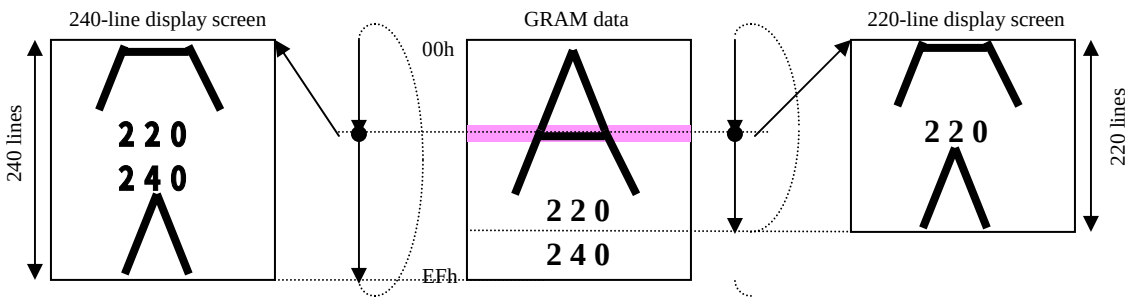


Fig. 6.2.7 (1) Line Addresses and LCD

By controlling the address of the display start line, the vertical scroll function, for example, will be available.
(The address of the display start line is refreshed in synchronization with the vertical sync signal after the command is set.)

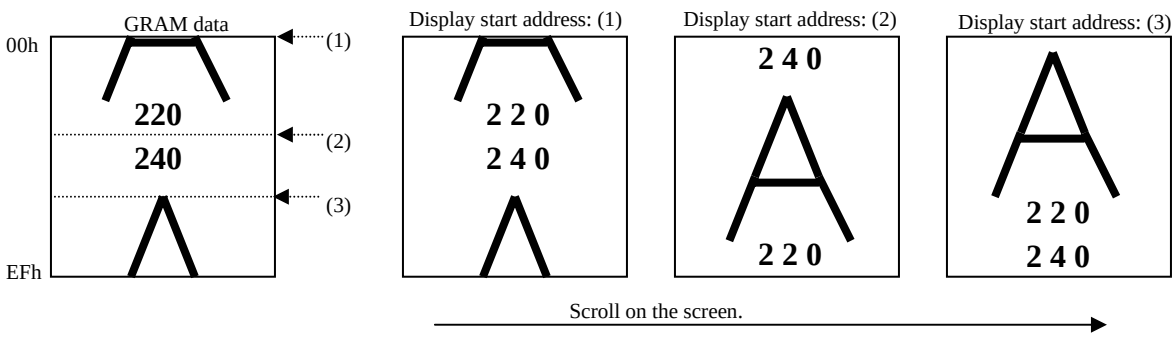
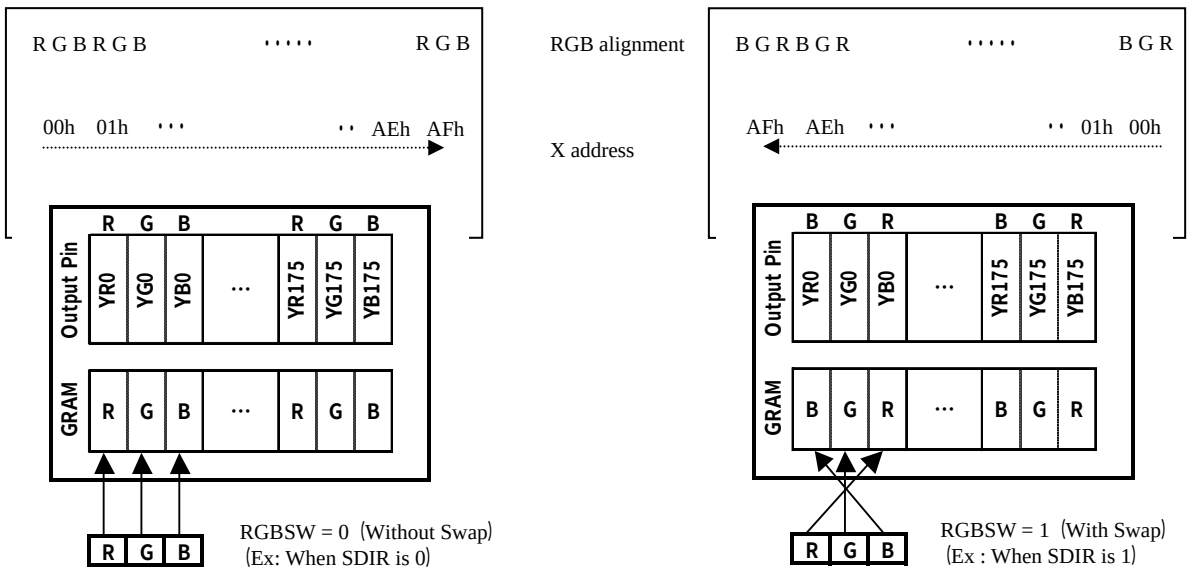


Fig. 6.2.7 (2) Display Start Line Address Setting and Vertical Scroll

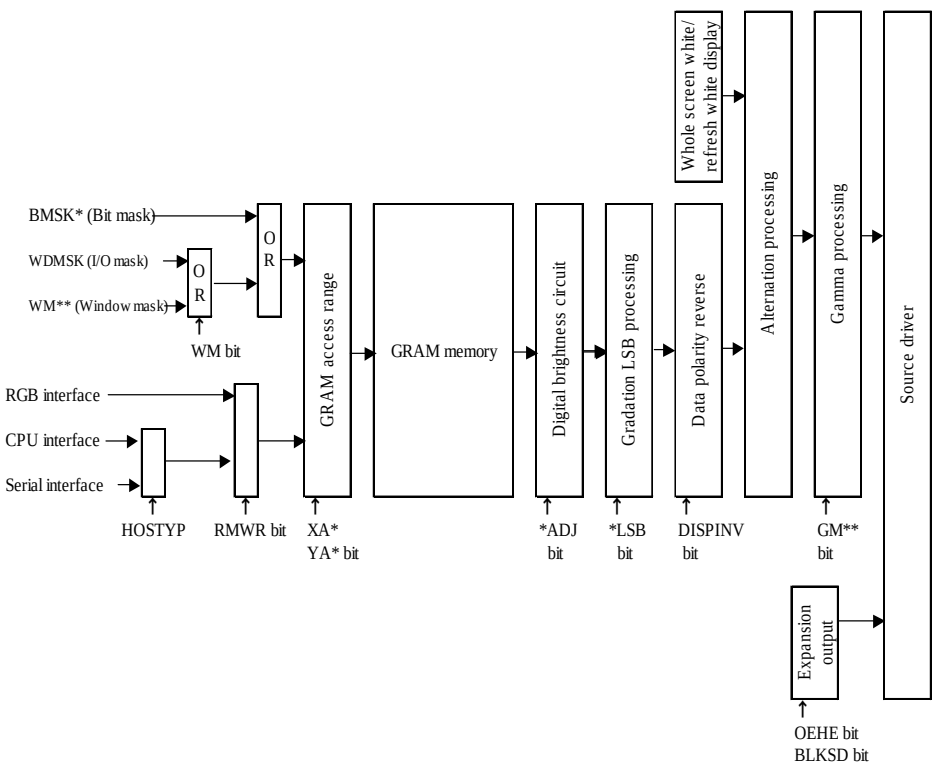
6.2.10 RGB Swap function

By setting command register RGBSW bit (address 0Dh, D[3]), driver output of R and B is counterchanged when pixel of R and B is swapped at writing to GRAM.
The function in combination of SDIR function make use of driver packaging direction and color filter alignment possible.
In addition, when GRAM read, the data which swapped at writing time return to its normal state as it is swapped reversely.

★Notice This function is used when the data is written to the GRAM. Therefore it should be set before the GRAM is written. Otherwise the setting will not become effective.



6.2.11 Display Data Processing Block Diagram



6.3 Display Control Function

6.3.1 Display Mode Control

The following four display conditions are controlled with command register DISP [1:0] settings.
The commands explained below are executed in synchronization with the vertical sync signal after the commands are set.

(1) Display OFF (DISP: 00)
The IC stops driving the LCD.
Turn off the LCD when overwriting the GRAM, in order not to reflect setting changes such as power supply setting changes on the display, or for a shutdown sequence.
When the display off command is executed, the IC operates as explained below.
- The source driver will have high-impedance output.
- The high-level output of the gate driver will stop with the NOEV* set high. (If the MN863480 is used in combination, the MN863480 will have VOFF- or VEE-level output.)
- With the VCOMEN* set low, the AC of the opposite electrode will stop, and VCOMLvoltage will be output.
  If the MN863480 is used in combination, the MN863480 will have output, the potential level of which will be intermediate VCOML potential.

Note: The oscillation circuit or power supply IC will not be stopped only by executing this command.
The operational amplifier of the source driver will, however, stop.

(2) Display Whole White (DISP: 01)
The LCD will be driven so that the whole screen will be white regardless of the contents of the GRAM.
This function is used to let the LCD discharge electricity before turning the display on or off during the setup or shutdown sequence.
The LCD displays white regardless of DISPINV bit settings.
The IC operates as described below with the display whole white command is executed.
- The source driver drives the white level (corresponding to 3F GRAM data). Specified alternation driving is performed.
- The gate driver is in normal operation, so is the alternative driving of the VCOM.

(3) Normal Display (DISP: 10)
In normal display mode, the whole screen will be displayed normally.

(4) Partial Display (DISP: 11)
In this mode, the screen is partially displayed.
By reducing the drive area, the power consumption of the IC will be saved. The non-display area will be white.
With an RFR bit setting, the non-display period will be regularly refreshed, when the display will be white.
For details, see Section 6.3.2.

6.3.2 Partial Display Function

When the IC is in partial display mode, the screen will be partially displayed (driven) in the Y direction, which will suppress the current consumption.
The following display patterns are available.
In the non-display area, the output of the gate driver, the driving operation of the source driver, and the display read operation will stop.
The non-display area is regularly refreshed, when the display will be white.
The partial display function will be set by specifying the start point of a maximum of two non-display areas with MASKS1 and MASKS2 and the end point with MASKE1 and MASKE2. The refresh cycle of the non-display area is specified with RFR (to be refreshed per frame, or not refreshed, or refreshed at any time).
Note 1) Satisfy the following conditions. MASKS1<MASKE1<MASKS2<MASKE2
Note 2) The MASK* setting must be less than the number of displayed lines (i.e., 240, 220, or 192 lines according to the GSL[2:0] setting).
Note 3) MASKS1 and MASKE1 are used together and so are MASKS2 and MASKE2. When MASKE1 is set, all the other settings will be refreshed.
Note 4) The display read operation will stop, but line addresses will be counted normally. Therefore, the relationship between GRAM data and LCD display is the same as that in normal display mode.
Note 5) To set a single non-display area, set both MASKS2 and MASKE2 to FFh.

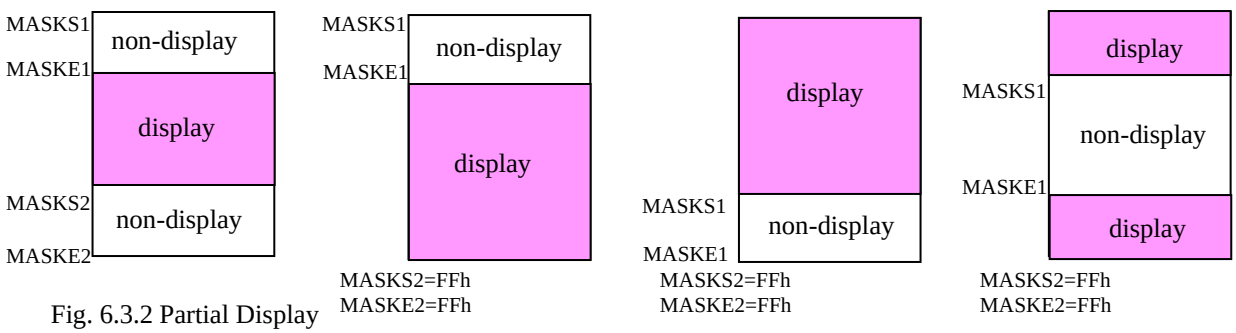


Fig. 6.3.2 Partial Display

6.3.3 Partial Scroll Function

By the control of the address of display start line as explained in Section 6.2.7, the vertical scroll function is available. In that case, the whole area of the GRAM will be the subject of scroll control.
By using the partial scroll function, the display area will be scrolled except some portions (such as the antenna mark portion), which will remain unchanged.
The following partial scroll settings are possible.
If the partial scroll specify bit SCRON is set to 0:
When the scroll area start specify bit SCRS, scroll area end bit SCRE, and scroll number bit SCRN are set, the settings will be reflected and executed at the vertical cycle after the SCRON bit is set to 1.
If the partial scroll specify bit SCRON is set to 1:
When the scroll area start specify bit SCRS or scroll area end bit SCRE or scroll number bit SCRN is set, the setting will be reflected and executed at the next vertical cycle.
When setting SCRS, SCRE, and SCRN bits in sequence over the vertical sync period, any bits executed after the vertical sync period (i.e., at the falling of the NVSYNCO) will not be reflected until the next vertical sync period is over.

Note 1) Make GSL[2:0] settings for the number of displayed lines (240, 220, or 192) to satisfy the following conditions.
SCRS < SCRE
SCRE − SCRS ≥ SCRN > Number of display lines
The display of the LCD will not be guaranteed unless the following condition is satisfied.
Display start line address LAS ≤ Scroll start address SCRS

Note 2) This function is used to control display line addresses. Therefore, the status of LCD display varies with the setting for the address of display start line.

Note 3) The partial display function explained in the previous section is not in any control of line addresses. The partial display function can be used together with the partial scroll function. As for display, the partial display function will take precedence. Therefore, the non-display area will be white.

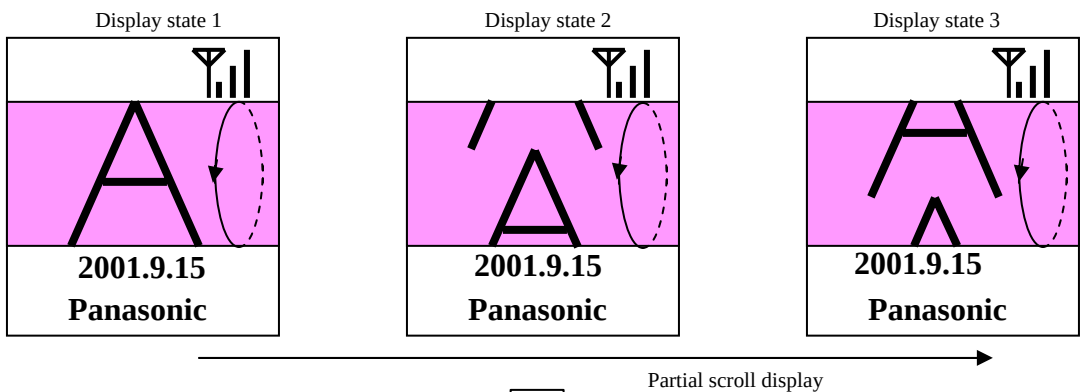
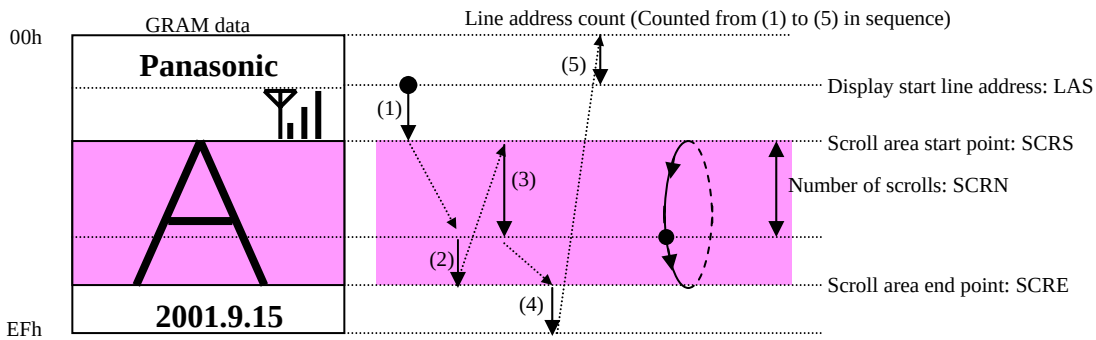


Fig. 6.3.3 (1) Partial Scroll Display



This chart shows the relationship between GRAM data and display read performance in display state 2 in figure (1).

Fig. 6.3.3 (2) GRAM Data and Line Addresses in Partial Scroll Display on LCD

6.3.4 Digital Brightness Adjustment Function

With the color adjustment commands executed by addresses 28h to 2Ah, brightness adjustments to R image data, G image data, and B image data can be made digitally respectively.
The set values in the RADJ[5:0], GADJ[5:0], and BADJ[5:0] registers are added to or subtracted from display read data from the GRAM and the data will be provided to the source driver.
The result of addition or subtraction will be a maximum of 00h or a minimum of 3Fh regardless of whether the actual value is larger than 3Fh or smaller than 00h.
This command enables brightness and white balance adjustments to displayed images.

6.3.5 Sync Control with Host

This IC supports moving images. Therefore, the IC has an external vertical sync mode, where the operation of the IC is in synchronization with the VSYNC supplied externally.

(1) Switching to External Vertical Sync

The IC will be set to external vertical sync mode by setting 1 to the VSYMODE.
After the command is set, the switching of the mode is detected by the internal vertical sync signal. Then the mode will be switched.
After the mode is switched, external VSYNC input will reset the vertical counter and the IC operates in new mode.
Therefore, as shown below, it is necessary to wait for two frames to go to external vertical sync mode.
While the IC is in external vertical sync mode, the blanking period will continue and the LCD will not be driven unless the external VSYNC signal is input.

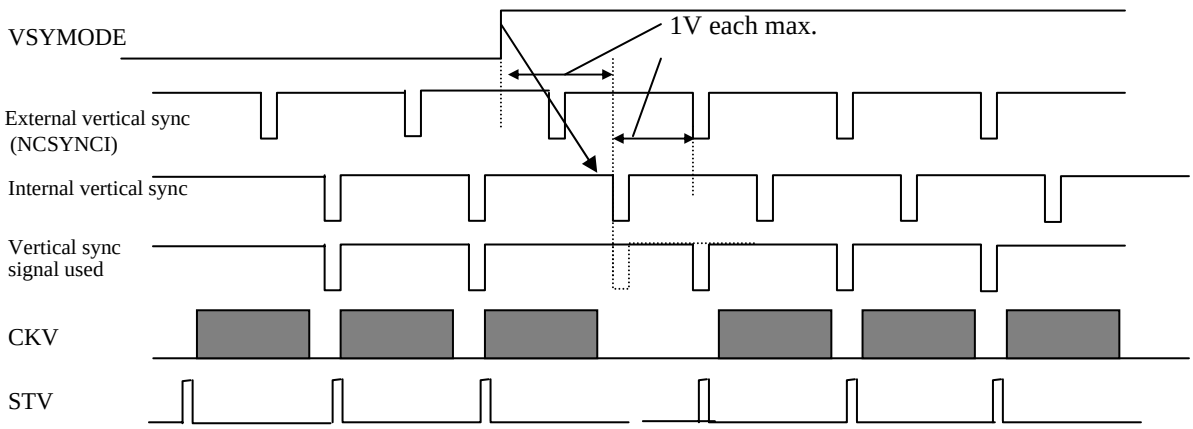


Fig. 6.3.5 Vertical Sync Switching (from Internal to External Vertical Sync)

(2) Switching to Internal Vertical Sync

Again, it is necessary to wait for two frames to go to internal vertical sync mode from external mode.
Note) After the command is set, it is necessary to provide the external vertical sync single for a minimum of 1V period, otherwise the switching of the vertical sync mode will not be detected. Therefore, the display on the panel will stop.

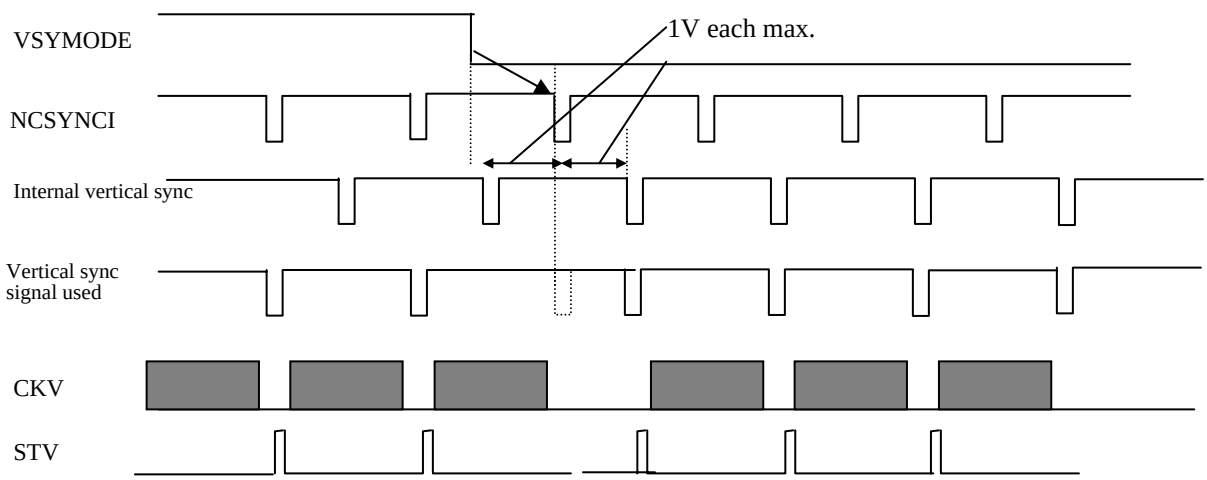


Fig. 6.3.5 Vertical Sync Switching (from External to Internal Vertical Sync)

(3) Relationship between LCD (Display Read) and RAM Write

When the IC is in external vertical sync mode, set the following lower limit of RAM write speed to satisfy the following conditions in consideration of the built-in oscillator frequency so that smooth moving images will be displayed.

- RAM Write Completion Time < Display Read Completion Time − Time margin
  (A time margin of two display read lines is required.)
  - RAM write completion time = Write start time + Number of written lines × 1-line write time

    Number of written pixels per line × (1/RAM write speed) + Horizontal write blanking period
  - Display read completion time − Margin time = (240 + Back porch − 2) × 1-line display read time

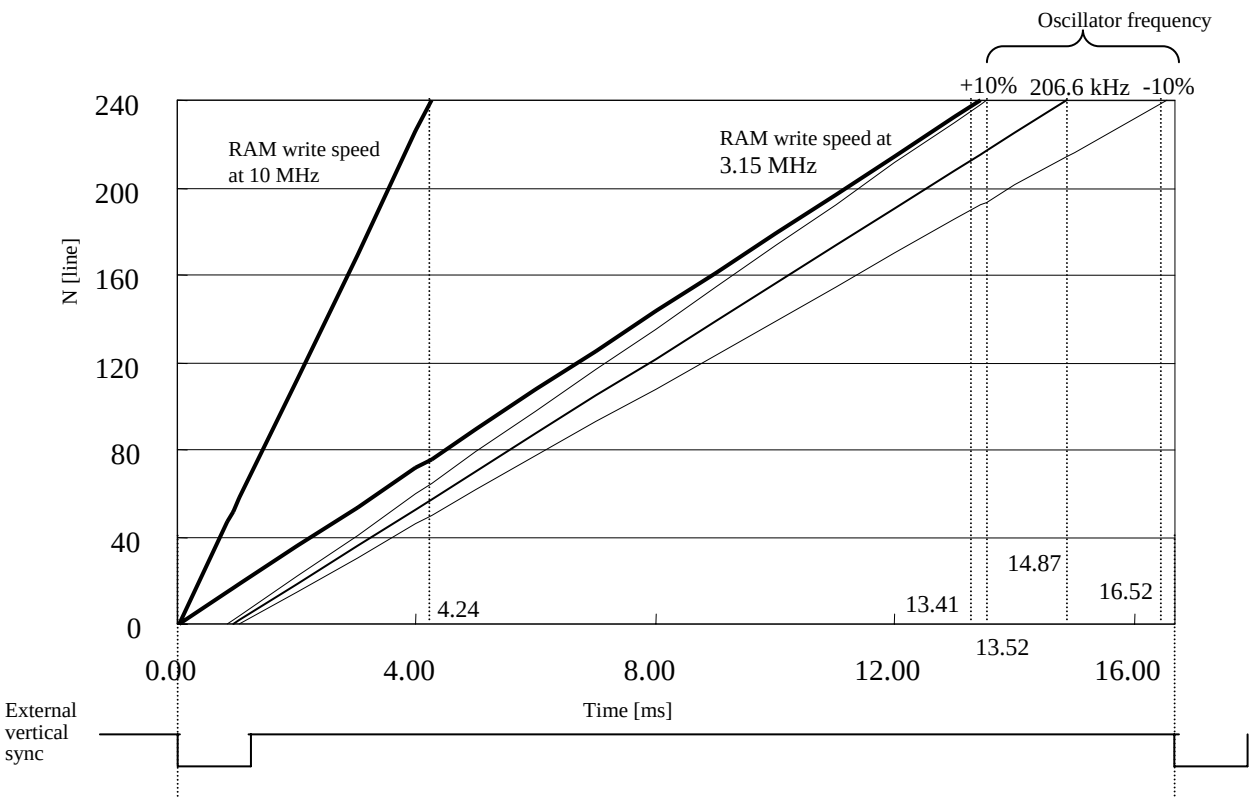
    Margin time: 2 lines; Back porch: 16; 1-line display read time: Number of 1H clock pulses × (1/Oscillator frequency)

[Calculation example]

A calculation example is shown below under the following conditions.

- Write start time: 20 μs after external sync
- Number of write lines: 240
- Number of written pixels per line: 176
- Horizontal write blanking period: 0
- Number of 1H clocks: 12 clocks (with HCNT set to 0B)
- Oscillator frequency: 206.6 kHz ± 10%

RAM write speed > 240 × 176 pixels/{(240 + 16 − 2) lines × 12 clock pulses × (1/206.6 kHz × 1.1) − 0.02 ms} = Approx. 3.15 MHz



6.3.6 Built-in Oscillation Circuit

This IC has a built-in oscillation circuit that generates display clock pulses as reference for the display control system and voltage step-up clock pulses for the power supply IC.

This oscillation circuit does not require any external parts, such as capacitors or resistors. The standard oscillator frequency is 206.6 kHz.

The oscillation is under ON/OFF (1: ON; 0: OFF) control by the command register OSCON bit. The oscillation is by default turned off.

6.3.7 Control of Horizontal Cycle and Vertical Cycle

The above display clock is used to control the horizontal cycle (H cycle) and vertical cycle (V cycle). The H cycle and V cycle are adjustable with the command register HCNT[4:0] and VCNT[9:2].

(1) H Cycle Settings

By making H cycle adjustments, the driving period (i.e., LCD panel charging period) of the source driver will be adjusted.

The period is adjustable between a period of 8 clock pulses and 24 clock pulses in 1-clock-pulse increments. The initial value is 12 clock pulses (with the HCNT set to 0B).

Therefore, 1H period is adjustable between 38.7 μs and 116.2 μs. The initial value is 58.1 μs, provided that the standard oscillator frequency is applied.

In external sync mode, the following time conditions must be kept.

Desired H cycle × (Preset number of gate driver output pins + 8H) < V cycle period

[Calculation example ; H cycle setting]

Use external V sync mode with V cycle : 60 Hz, Gate Driver output : 240 line,

(i.e., oscillator frequency variation ⇒10 %)

In 1 H clock value < (206.6 kHz × 0.9) / [60 Hz × (240 + 8) line] = 12.5

⇒ therefore, it requires under 12 clock setting.

Make an optimum H cycle period setting in consideration of the LCD's pixel load characteristics and the source driver's current capacity setting.

(2) V Cycle Settings

By making V cycle adjustments, the frame frequency will be adjusted. If the display quality of the LCD is kept, the power consumption of the system can be saved by reducing the frame frequency.

If the frame frequency is reduced, however, the image quality will be adversely affected. Therefore, fully evaluate the circuit design.

sThe V cycle set bit VCNT will be enabled only in internal sync mode. The VCNT set value will be ignored when the IC is in external sync mode.

In internal sync mode, the fol lowing condition must be kept.

(VCNT [9:1] + 1) × 4 ; as line value in 1 V cycle.

It is possible to set the V cycle to a maximum of 1024H in 4H increments. It is, however, necessary to set the preset number of gate driver output pins plus a minimum of 8H lines. The value is by default set to 300H (i.e., the VCNT[9:2] set to 4Ah).

[Calculation example ; V cycle setting]

Use internal V sync mode, set H cycle = 12 clock (HCNT = OB) and V cycle = 60 Hz.

(i.e., calculate oscillator frequency = 206.6kHz)

In 1 V line value = (206.6 kHz / 12 clock) / 60 Hz = 286.9 line.

It is able to choose 284 line case or 288 line, as setting is per 4 line.

284 line case, VCNT set to 284 / 4 – 1 = 70, VCNT = 46 h.

6.4 LCD Drive Control

6.4.1 LCD Drive Signal Generation

The following signals are generated to drive the LCD. Figures 6.4.1 (1) to (4) show the generation timing of each drive signal.

( ): Internal signal

Function	Control signal	Description of control	Command set bit
Transfer of source driver data	(LD)	Used to transfer display read data from the GRAM to the source driver.	–
Control of drive/stop timing of source driver	(NOEH)	Used to control the drive/stop timing of the source driver within a 1H period.	OEHA/OEHN
		Used to control the drive/stop timing of the source driver at the V cycle. 1) Starts the source driver 1H before the display period. 2) Controls the extension of the drive period after the display period completes in order to stabilize the potential of the source line during vertical blanking.	OEHON/OEHE GSL/MASK** /RFR
		The impedance of the output pin will be high while the source driver is not in driving operation.	AMPON
Generation of gate driver drive signal	STV∗	Used to output the display start position of the gate driver start pulse.	–
	CKV∗	Used to generate the gate driver shift clock. The clock will be continuously output during the vertical period.	CKVPW
Control of gate driver output prohibit timing	NOEV∗	Used to control the output prohibit timing of the gate driver within a 1H period.	OEVA/OEVN
		Used to control the output prohibit timing of the gate driver at the V cycle. 1) Stops output from lines other than that for the display period. 2) Prohibits the output of the non-display period according to the partial display setting.	GTYP/MASK** /RFR
AC control of opposite electrode (VCOM)	POL∗	Used to specify the alternation polarity of the VCOM.	FRPOL
	VCOMEN∗	Used to control the drive/stop timing of the VCOM at the V cycle. 1) Starts driving the VCOM 1H before the display period. 2) Controls the extension of the drive period after the display period completes.	VCOMON /VCOME

Note) The STV*, CKV*, and POL* signals are continuously output without interruption simultaneously with the oscillation of the internal oscillation circuit. These signals will stop when the internal oscillation circuit stops operating.

6.4.1 Relationship between display timing and host writing at RGB interface

External vertical sync signal input (cmd_11h=80h) should be used at RGB interface and supply vertical sync signal from VSYNCI.

This setting make writing **from host** and LCD display synchronize. Moreover, GRAM address will be initialized by external vertical sync signal input at RGB interface, writing from host cannot operate without input the external vertical sync signal.

H-signal is created by internal OSC and resister value of number of 1H-clock, so external H-signal is no need.

With following figures 6.4.2 ① ～ ③, the description of usage shows on next page.

Condition : 1H =12 clock (cmd_1Eh=0Bh) / 240 line display (cmd_20h[7:5] = "111")

Display timiming

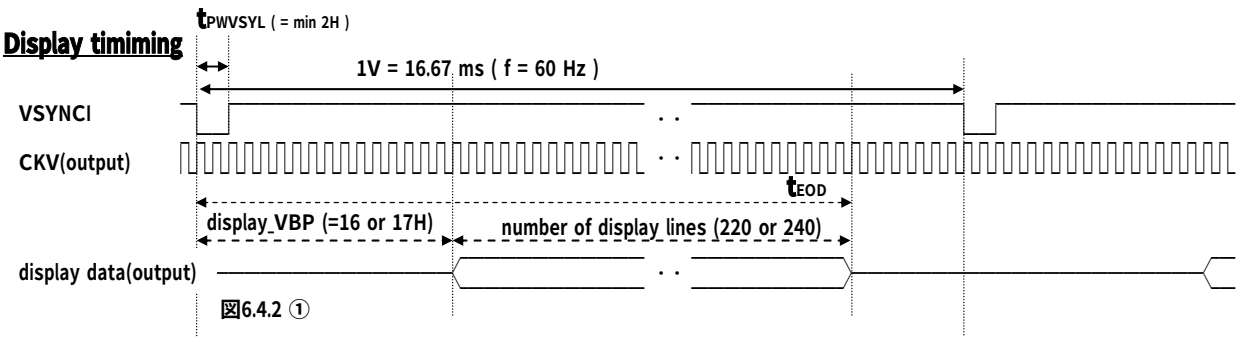


図6.4.2 ①

Host writing timing for 1-frame

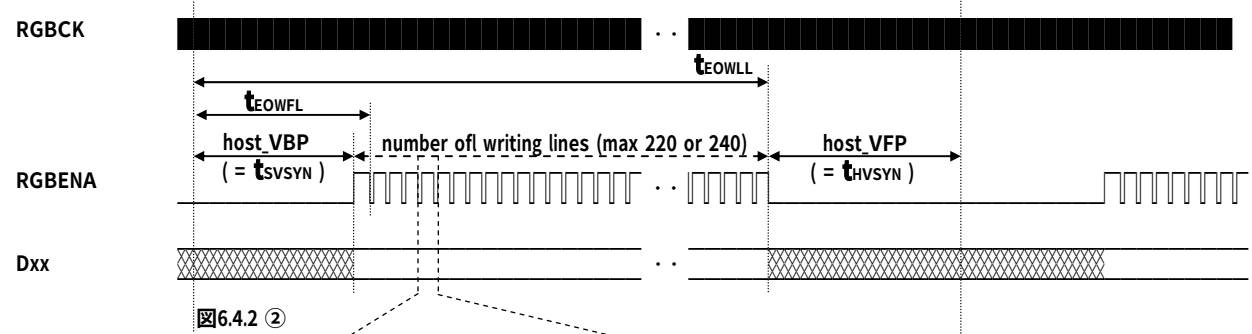


図6.4.2 ②

Host writing timing for 1-Line

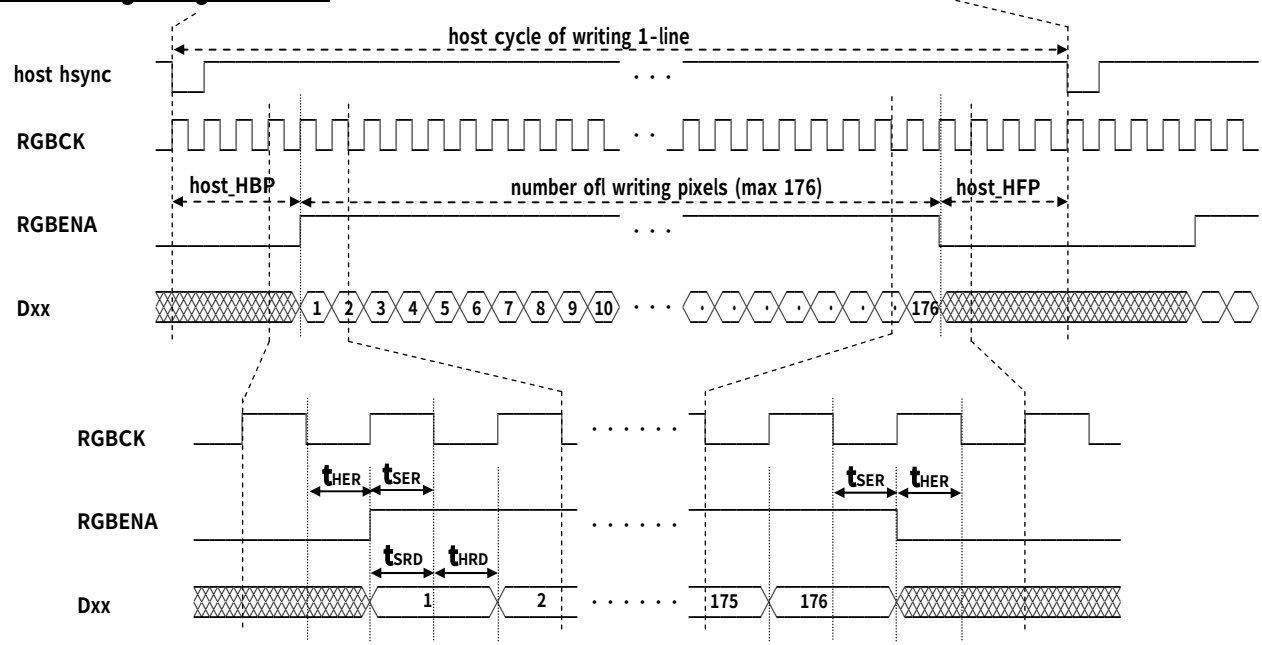


図6.4.2 ③

Following condition (①~⑥) should be satisfy at RGB interface.
Condition : 1H =12 clock (cmd_1Eh=0Bh) / 240 line display (cmd_20h[7:5] = "111")

■ Limitation in order to complete initialize GRAM address and V-timing of LCD display by external vertical sync signal.

① Pulse width of external vertical sync signal.
→ t_{PWVSYL} : need over 2H period MIN should be 0.13 ms

② Relation of external vertical sync signal and host writing start / complete time.
→ t_{SVSYN} : over 15 μs
→ t_{HVSYN} : over 10 μs

■ Limitation in order to prevent display distarbance by collision of Host-write-timing and display-read-timig.

③ Set to YDIR = ADIR = 0

④ Start writing before display and complete writing before the first line on the LCD display.
→ t_{EOWFL} : Operate within 0.84 ms (MIN)

⑤ Complete writing before the last line on the LCD display
→ t_{EOWLL} : Operate within 13.46 ms (MIN) [when oscillate clock has + 10%]

■Limitation in order to display all lines within 1V period of the external vertical sync.

⑥ Keep 1 vertical period that enable to display all lines, in consideration of variation of the oscillation frequency.
→ t_{EOD} : **Keep more than 8H period (16.1ms [MIN])**

NOTE) ★ **After LCD vertical cycle action initialized by external vertical sync signal, the control of LCD horizontal cycle is operated by internal oscillator clock based on 1 H clock. Therefore there is no need to provide horizontal sync signal.**
★ **After writing address from host to GRAM initialized by external vertical sync signal, writing address from host to GRAM can automatically count every accesses according to the indicated writing address area.**
(This operation is unrelated LCD display)
★ **When interrupting GRAM-write, RGBENA should be once inactivated (RGBENA = L)**
(Ex, vertical blanking provide in line unit at writing)
When RGBCK is supplied as RGBENA = H, the data will be accepted and updated GRAM data and address.

[Description of symbols in figure 6.4.2]

Figure 6.4.2 ①

t_{PWVSYL} (end of display) : **"L" pulse width which need to External vertical sync signal "NVSYNCI" signal. This require 2 H period out of minimum display.**
Minimum value : 0.129 ms (Oscillator clock = -10%)

t_{EOD} (end of display) : **End of display time from Vertical sync signal**
When 240 line display sets, 1H period x (16 or 17 line + 240 line)
Maximum value : 16.586 ms (Oscillator clock = -10%)

display_VBP : **A period from vertical sync signal to display start. The horizontal cycle controlled at Oscillator clock is 16 to 17 H**

Figure 6.4.2 ②

t_{EOWFL} (end of writing 1st line) : **Writing completed time at the first HOST line. Complete before display first line drives.**
Minimum value : 0.84 ms (Oscillator clock = +10%)

t_{EOWLL} (end of writing last line) : **Writing completed time at the last HOST line. Complete before display last line drives.**
Minimum value : 13.46 ms (Oscillator clock = +10%)

t_{SVSYN} (VSYNC set-up time) : **VSYNC input set up time for starting data transfer. Keep more than 15 μs.**

t_{HVSYN} (VSINC hold time) : **VSYNC input hold time for ending data transfer to VSYNC input Keep more than 10 μs.**

Figure 6.4.2 ③

t_{SER} (Enable set-up time) : **RGBENA signal set up time for RGBCK↓ Keep the regulation value in the product standards**

t_{HER} (Enable hold time) : **RGBNA sygnal hold time for RGBCK↓ Keep the regulation value in the product standards**

t_{SRD} (Data set-up time) : **Data Input set up time for RGBCK↓ Keep the regulation value in the product standards**

t_{HRD} (Data hold time) : **Data hold time for RGBCK↓ Keep the regulation value in the product standards**

Host_HBP : **Back porch period of H cycle that writing into HOST. There is no regulation**

Host_HFP : **Front porch period of H cycle that writing into HOST. There is no regulation**

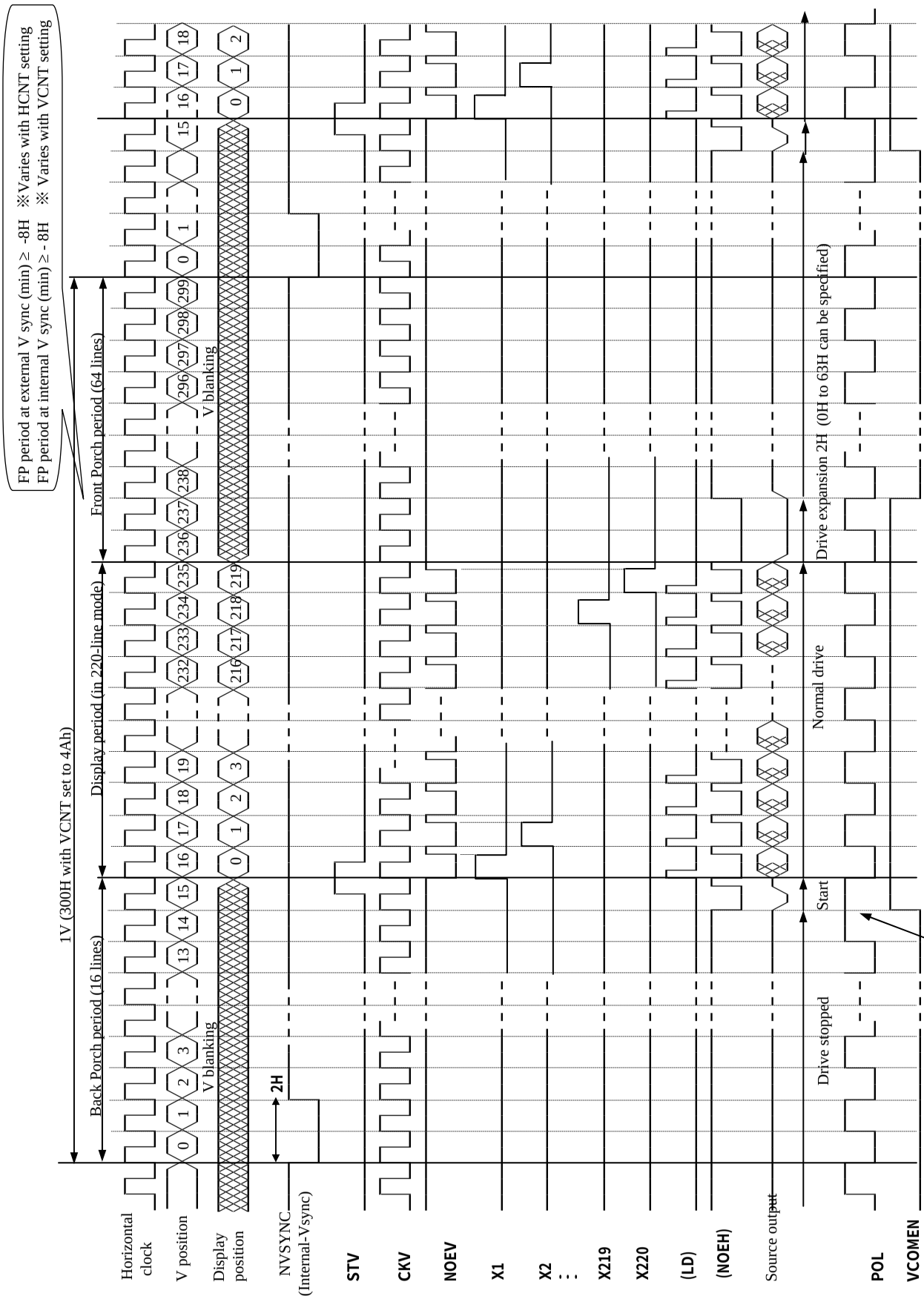


Fig. 6.4.1 (1) Timing Chart of Each LCD Drive Signal (V Cycle)

Note: There is an OEHE/VCOME expansion of 02h.

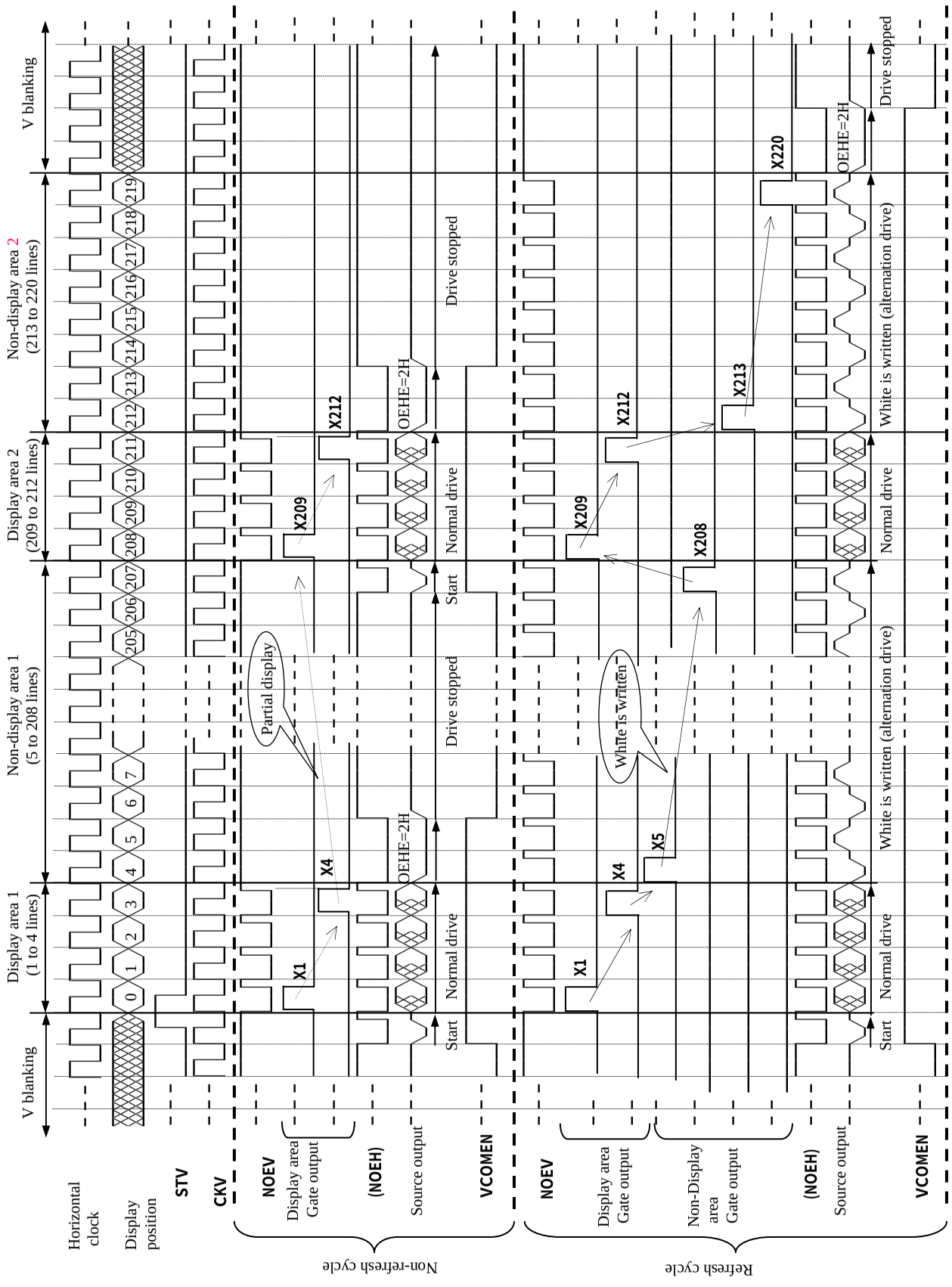


Fig. 6.4.1 (2) Timing Chart of Each LCD Drive Signal in Partial Display Mode

Note: There is an OEHE/VCOME expansion of 2H.

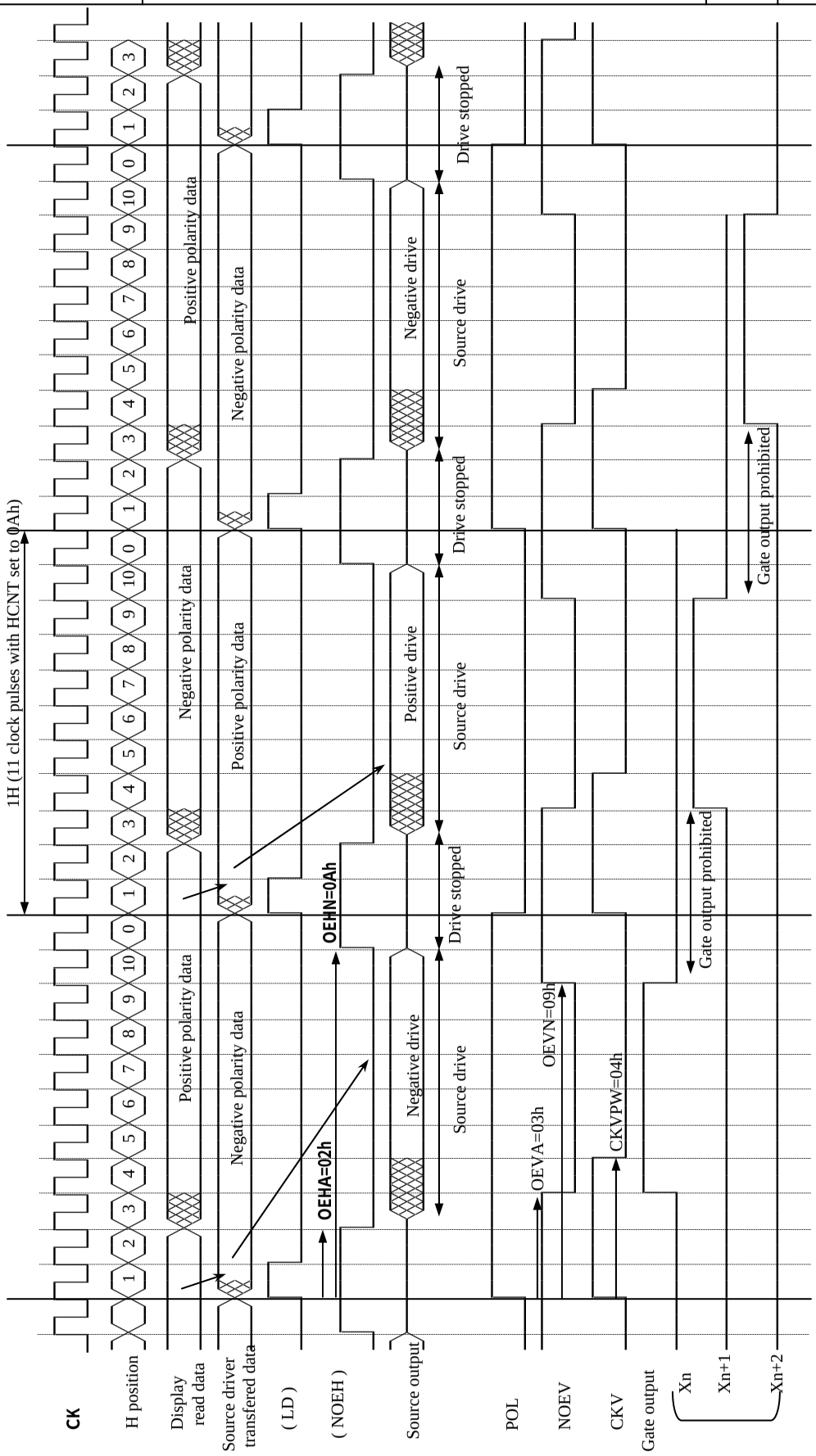


Fig. 6.4.1 (3) Timing Chart of Each LCD Drive Signal (H Cycle)

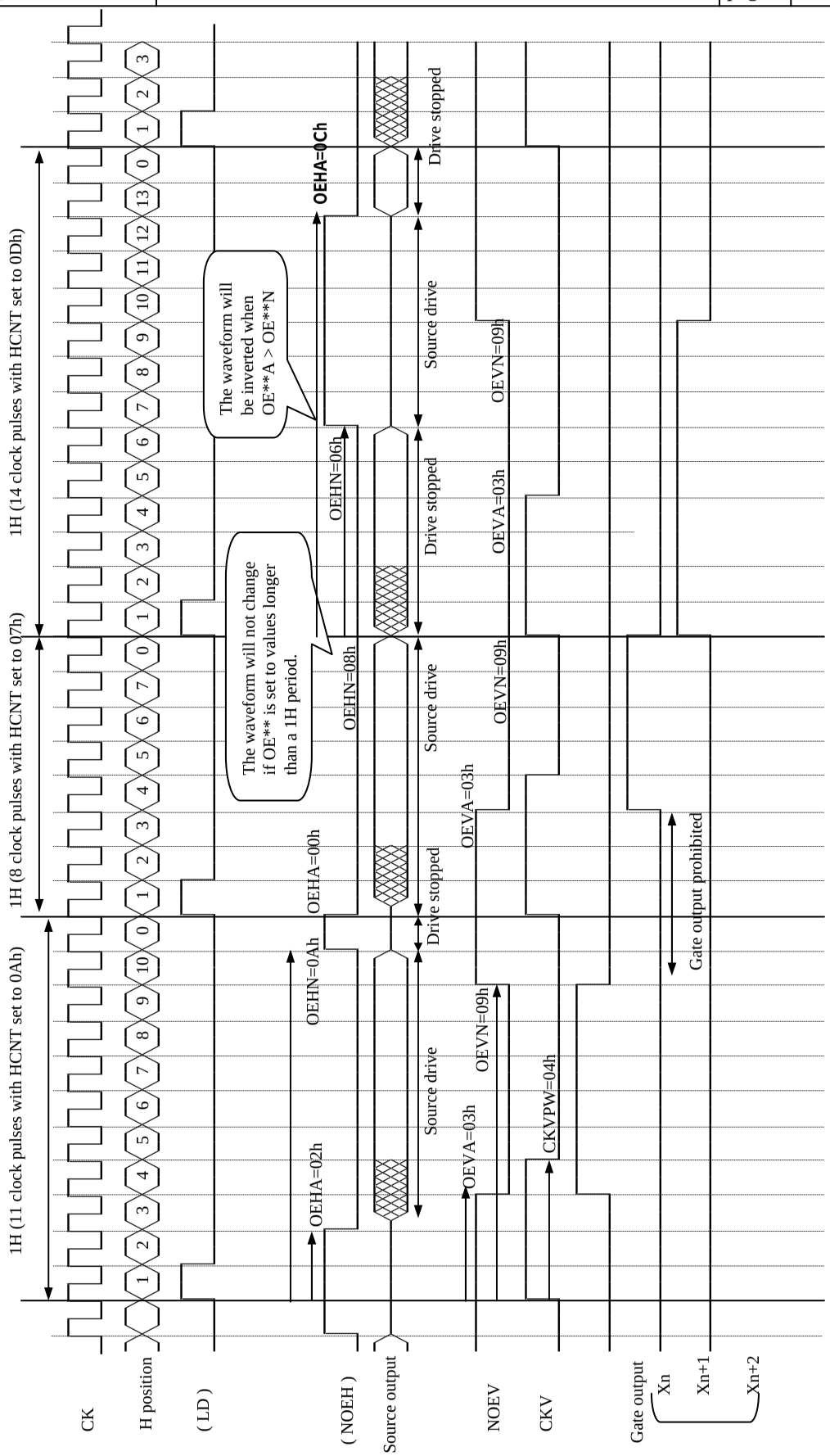


Fig. 6.4.1 (4) Timing Control of LCD Drive Signals within 1H Periods (OEHA, OEHN, OEVA, and OEVN)

6.5 Source Driver Operation Setting

6.5.1 Gradation/Binary Drive Mode

The source driver has a 6-bit DAC for 64-step RGB gradation drive control. If gradation display is not required, binary driving will be possible. At the time of binary driving, the static current flowing to the operational amplifier of the DAC circuit of the above source driver and the internal resistor (i.e., VREF resistor) for gradation voltage generation will be stopped, which will save the power consumption of the system.
By setting the COL bit of the driver operation setting 2 register to 0, the IC will be in binary drive mode.
The IC will use only R5, G5, and B5 data for display, and any other data will be ignored when the IC is in binary mode.The source driver will drive the LCD by using only MSB bit of each RGB pixel of the GRAM while the IC is in binary drive mode. After this command is set, the command will be executed in synchronization with the V sync signal.

6.5.2 Separation of VREF Resistor

As explained above, when the IC is in binary drive mode, the VREF resistor for gradation voltage generation is separated for static current suppression. At the time of gradation driving, VREF resistor separation during the V blanking period will be possible. The VREF resistor will be separated by setting 0 to the RSWON bit of the driver operation setting 2 register. The VREF resistor will be automatically connected before the LCD starts display.When using this mode, the panel load will influence the quality of display. Check the quality of display on the actual panel before applying the IC to the products.

6.5.3 Source Driver Driving Output

1) Source Driver Driving Capacity Adjustments

The driving capacity of the source driver is adjusted by the SAMP[2:0] bits of the driver operation setting 2 register. (See table below.) When the bits are set to 000, the source driver will stop driving. (The value is by default set to 011.)

The necessary drive capacity is influenced by the panel load. Check the display quality on the actual panel before applying the IC to the products.

SAMP[2:0]	Capacity
000	Stop
001	Low
010	Between low and medium
011	Medium
100	Between medium and high
101	High
110	Prohibited
111	Prohibited

2) Polarity of Source Driver Output, Obtaining Gamma Characteristics, and Polarity Based on VCOM

Stored data in the GRAM will be reversed in the polarity reverse circuit so that the polarity will be opposite to the polarity of POL*signals.
At the time of normal display with DISPINV set to 0,
when POL* is set low, normal output will be turned on: No GRAM data bit change (i.e., the 3Fh bit will be output as 3Fh bit and the 00h bit will be output as the 00h bit);
when the POL* is set high, reversed output will be turned on: GRAM data will be reversed and output so that the 3Fh bit will be the 00h bit and the 00h bit will be the 3Fh bit.
At the time of reverse display with DISPINV set to 1,
when POL* is set low, reversed output will be turned on: GRAM data will be reversed and output so that the 3Fh bit will be the 00h bit and the 00h bit will be the 3Fh bit;
when the POL* is set high, normal output will be turned on: No GRAM data bit change (i.e., the 3Fh bit will be output as 3Fh bit and the 00h bit will be output as the 00h bit).
Gamma characteristics will not be influenced by the DISPINV.
When the POL polarity is normal (i.e., POL* is set low), signals will be converted into analog values in the gamma circuit (D/A conversion circuit) according to the gamma characteristics of the GMPn (n is set between 1 and 62) and output from the source driver.
When the POL polarity is reversed (i.e., POL* is set high), the signals are output from the source driver according to the gamma characteristics of the GMNn (n is set between 1 and 62).
As for gamma characteristics, refer to Section 6.5.4.
The information here is provided on condition that the POL* is the same as the VCOM in polarity.
If the DISPINV is set to 0 and host input data is 00h (black), the GRAM data will be displayed as follows when the polarity is normal:
GRAM data 00h => After conversion: 00h => With VREFH selected, VCOM: Displayed black on the LCD at the VCOML potential.
When the polarity is reversed,
GRAM data 00h => After conversion: 3Fh => With VREFL selected, VCOM: Displayed black on the LCD at the VCOMH potential.
With the DISPINV set to 1,
At the time of normal operation after conversion: 3Fh => With VREFL selected, VCOM: Displayed white on the LCD at the VCOML potential.
When the polarity is reversed,
At the time of reverse operation after conversion: 00h => With VREFH selected, VCOM: Displayed white on the LCD at the VCOMH potential.
The DISPINV is disabled for refresh white display while in partial display mode.

6.5.4 Gamma Correction Function

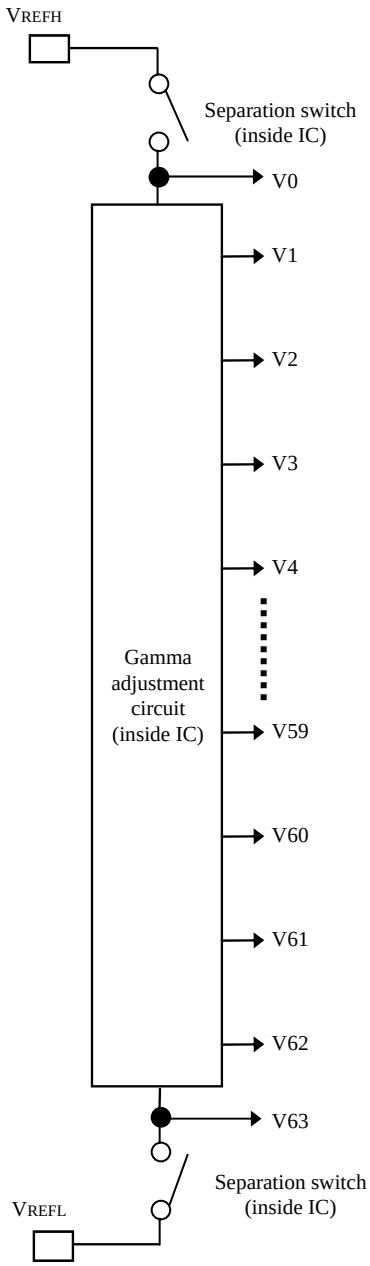
(1) Gamma Adjustment Command

The 62 gamma adjustment commands in addresses 31h to 6Eh make it possible to make gamma adjustments to the 1- to 62-step gradation voltages. (Here, gradation 0 and gradation 63 are fixed at the VREFH or VREFL.)

Eight gamma adjustments are possible for the positive drive and negative drive of each gradation step.

(2) Built-in Resistor for Gamma Correction

The output voltage of the IC is determined by the externally input VREFH, VREFL, gamma selector value, and input data value in the following gamma adjustment circuit.



The output voltage of the gamma adjustment circuit is determined by the formula shown in table 6.5.4 according to the selector value (see note 1).

Resistive divider is applied to the internal circuit of the IC. Therefore, it is recommended to apply low-impedance voltage input into the VREFH and VREFL pins by using an operation amplifier.

The separation switch will separate the resistor in the gamma adjustment circuit, thus cutting the current flow between the VREFH and VREFL and saving power consumption.

Note 1)

The following condition must be kept when applying voltage to the VREFH and VREFL.

$$V_{REFH} \geq V_{REFL}$$

Fix the VREFH and VREFL voltages during operation of the IC.

Fig. 6.5.4 Built-in Resistor for Gamma Correction

(3) Relationship of Gamma Selector Value, Input Data, and Output Voltage

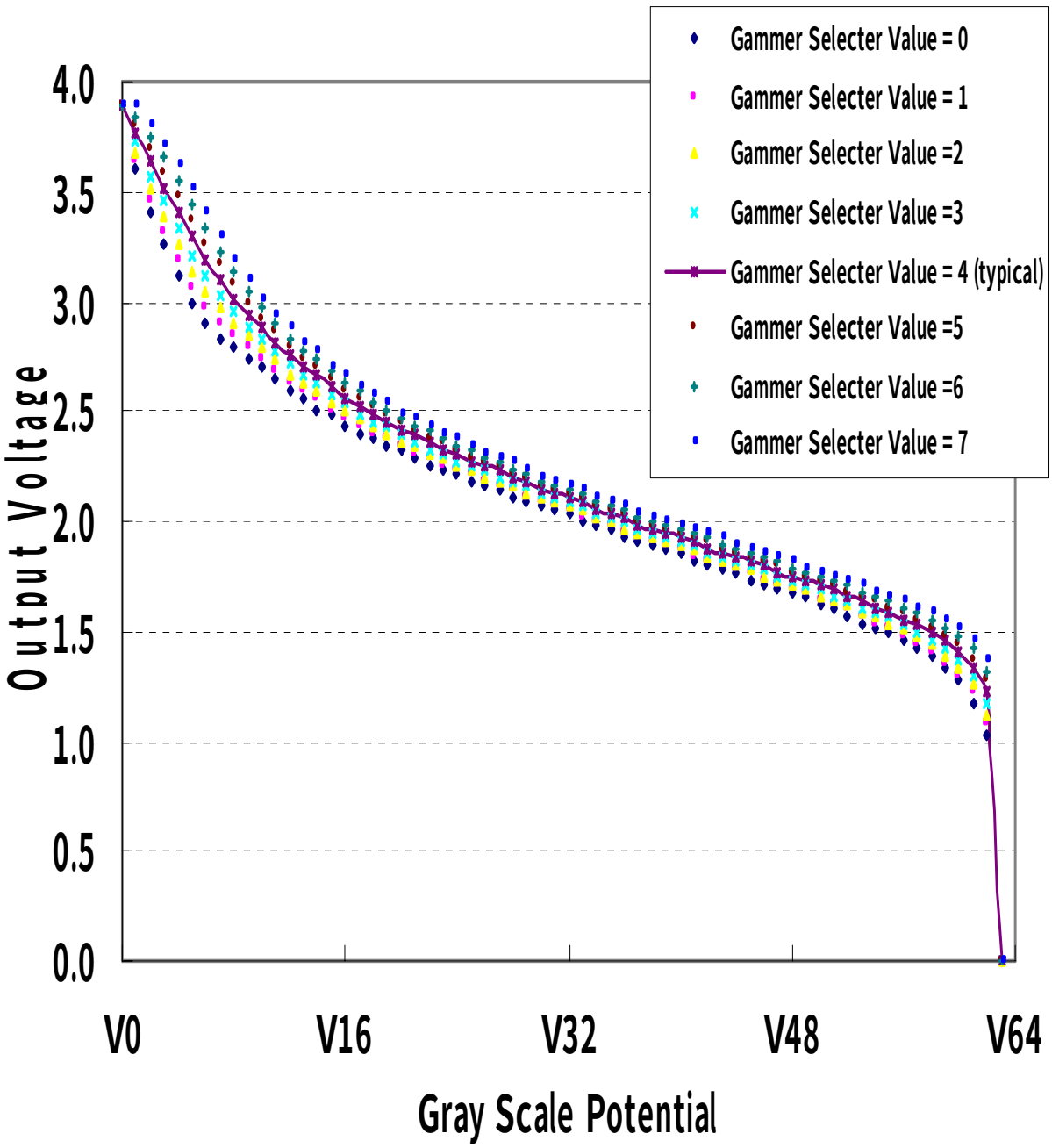
Table 6.5.4 Relationship of Gamma Selector Value, Input Data, and Output Voltage

Input Data	Gradation Potential	Output voltage calculation formula							
		Gamma Selector Value (GMPn[2:0], GMNn[2:0] n=1 to 62)							
		0	1	2	3	4 (criterion)	5	6	7
00h	V_0					V_{REFH}			
01h	V_1	$V_{R01}-V_{RHL}\times4/100$	$V_{R01}-V_{RHL}\times3/100$	$V_{R01}-V_{RHL}\times2/100$	$V_{R01}-V_{RHL}\times1/100$	$V_{R01}=V_{REFL}+V_{RHL}\times0.96539$	$V_{R01}+V_{RHL}\times1/100$	$V_{R01}+V_{RHL}\times2/100$	$V_{R01}+V_{RHL}\times3/100$
02h	V_2	$V_{R02}-V_{RHL}\times4/70$	$V_{R02}-V_{RHL}\times3/70$	$V_{R02}-V_{RHL}\times2/70$	$V_{R02}-V_{RHL}\times1/70$	$V_{R02}=V_{REFL}+V_{RHL}\times0.93180$	$V_{R02}+V_{RHL}\times1/70$	$V_{R02}+V_{RHL}\times2/70$	$V_{R02}+V_{RHL}\times3/70$
03h	V_3	$V_{R03}-V_{RHL}\times4/60$	$V_{R03}-V_{RHL}\times3/60$	$V_{R03}-V_{RHL}\times2/60$	$V_{R03}-V_{RHL}\times1/60$	$V_{R03}=V_{REFL}+V_{RHL}\times0.90285$	$V_{R03}+V_{RHL}\times1/60$	$V_{R03}+V_{RHL}\times2/60$	$V_{R03}+V_{RHL}\times3/60$
04h	V_4	$V_{R04}-V_{RHL}\times4/55$	$V_{R04}-V_{RHL}\times3/55$	$V_{R04}-V_{RHL}\times2/55$	$V_{R04}-V_{RHL}\times1/55$	$V_{R04}=V_{REFL}+V_{RHL}\times0.87212$	$V_{R04}+V_{RHL}\times1/55$	$V_{R04}+V_{RHL}\times2/55$	$V_{R04}+V_{RHL}\times3/55$
05h	V_5	$V_{R05}-V_{RHL}\times4/55$	$V_{R05}-V_{RHL}\times3/55$	$V_{R05}-V_{RHL}\times2/55$	$V_{R05}-V_{RHL}\times1/55$	$V_{R05}=V_{REFL}+V_{RHL}\times0.84357$	$V_{R05}+V_{RHL}\times1/55$	$V_{R05}+V_{RHL}\times2/55$	$V_{R05}+V_{RHL}\times3/55$
06h	V_6	$V_{R06}-V_{RHL}\times4/55$	$V_{R06}-V_{RHL}\times3/55$	$V_{R06}-V_{RHL}\times2/55$	$V_{R06}-V_{RHL}\times1/55$	$V_{R06}=V_{REFL}+V_{RHL}\times0.81978$	$V_{R06}+V_{RHL}\times1/55$	$V_{R06}+V_{RHL}\times2/55$	$V_{R06}+V_{RHL}\times3/55$
07h	V_7	$V_{R07}-V_{RHL}\times4/60$	$V_{R07}-V_{RHL}\times3/60$	$V_{R07}-V_{RHL}\times2/60$	$V_{R07}-V_{RHL}\times1/60$	$V_{R07}=V_{REFL}+V_{RHL}\times0.79502$	$V_{R07}+V_{RHL}\times1/60$	$V_{R07}+V_{RHL}\times2/60$	$V_{R07}+V_{RHL}\times3/60$
08h	V_8	$V_{R08}-V_{RHL}\times4/70$	$V_{R08}-V_{RHL}\times3/70$	$V_{R08}-V_{RHL}\times2/70$	$V_{R08}-V_{RHL}\times1/70$	$V_{R08}=V_{REFL}+V_{RHL}\times0.77361$	$V_{R08}+V_{RHL}\times1/70$	$V_{R08}+V_{RHL}\times2/70$	$V_{R08}+V_{RHL}\times3/70$
09h	V_9	$V_{R09}-V_{RHL}\times4/80$	$V_{R09}-V_{RHL}\times3/80$	$V_{R09}-V_{RHL}\times2/80$	$V_{R09}-V_{RHL}\times1/80$	$V_{R09}=V_{REFL}+V_{RHL}\times0.75426$	$V_{R09}+V_{RHL}\times1/80$	$V_{R09}+V_{RHL}\times2/80$	$V_{R09}+V_{RHL}\times3/80$
0Ah	V_{10}	$V_{R10}-V_{RHL}\times4/90$	$V_{R10}-V_{RHL}\times3/90$	$V_{R10}-V_{RHL}\times2/90$	$V_{R10}-V_{RHL}\times1/90$	$V_{R10}=V_{REFL}+V_{RHL}\times0.73785$	$V_{R10}+V_{RHL}\times1/90$	$V_{R10}+V_{RHL}\times2/90$	$V_{R10}+V_{RHL}\times3/90$
0Bh	V_{11}	$V_{R11}-V_{RHL}\times4/95$	$V_{R11}-V_{RHL}\times3/95$	$V_{R11}-V_{RHL}\times2/95$	$V_{R11}-V_{RHL}\times1/95$	$V_{R11}=V_{REFL}+V_{RHL}\times0.72244$	$V_{R11}+V_{RHL}\times1/95$	$V_{R11}+V_{RHL}\times2/95$	$V_{R11}+V_{RHL}\times3/95$
0Ch	V_{12}	$V_{R12}-V_{RHL}\times4/100$	$V_{R12}-V_{RHL}\times3/100$	$V_{R12}-V_{RHL}\times2/100$	$V_{R12}-V_{RHL}\times1/100$	$V_{R12}=V_{REFL}+V_{RHL}\times0.70671$	$V_{R12}+V_{RHL}\times1/100$	$V_{R12}+V_{RHL}\times2/100$	$V_{R12}+V_{RHL}\times3/100$
0Dh	V_{13}	$V_{R13}-V_{RHL}\times4/110$	$V_{R13}-V_{RHL}\times3/110$	$V_{R13}-V_{RHL}\times2/110$	$V_{R13}-V_{RHL}\times1/110$	$V_{R13}=V_{REFL}+V_{RHL}\times0.69345$	$V_{R13}+V_{RHL}\times1/110$	$V_{R13}+V_{RHL}\times2/110$	$V_{R13}+V_{RHL}\times3/110$
0Eh	V_{14}	$V_{R14}-V_{RHL}\times4/110$	$V_{R14}-V_{RHL}\times3/110$	$V_{R14}-V_{RHL}\times2/110$	$V_{R14}-V_{RHL}\times1/110$	$V_{R14}=V_{REFL}+V_{RHL}\times0.68186$	$V_{R14}+V_{RHL}\times1/110$	$V_{R14}+V_{RHL}\times2/110$	$V_{R14}+V_{RHL}\times3/110$
0Fh	V_{15}	$V_{R15}-V_{RHL}\times4/120$	$V_{R15}-V_{RHL}\times3/120$	$V_{R15}-V_{RHL}\times2/120$	$V_{R15}-V_{RHL}\times1/120$	$V_{R15}=V_{REFL}+V_{RHL}\times0.66979$	$V_{R15}+V_{RHL}\times1/120$	$V_{R15}+V_{RHL}\times2/120$	$V_{R15}+V_{RHL}\times3/120$
10h	V_{16}	$V_{R16}-V_{RHL}\times4/120$	$V_{R16}-V_{RHL}\times3/120$	$V_{R16}-V_{RHL}\times2/120$	$V_{R16}-V_{RHL}\times1/120$	$V_{R16}=V_{REFL}+V_{RHL}\times0.65847$	$V_{R16}+V_{RHL}\times1/120$	$V_{R16}+V_{RHL}\times2/120$	$V_{R16}+V_{RHL}\times3/120$
11h	V_{17}	$V_{R17}-V_{RHL}\times4/130$	$V_{R17}-V_{RHL}\times3/130$	$V_{R17}-V_{RHL}\times2/130$	$V_{R17}-V_{RHL}\times1/130$	$V_{R17}=V_{REFL}+V_{RHL}\times0.64742$	$V_{R17}+V_{RHL}\times1/130$	$V_{R17}+V_{RHL}\times2/130$	$V_{R17}+V_{RHL}\times3/130$
12h	V_{18}	$V_{R18}-V_{RHL}\times4/140$	$V_{R18}-V_{RHL}\times3/140$	$V_{R18}-V_{RHL}\times2/140$	$V_{R18}-V_{RHL}\times1/140$	$V_{R18}=V_{REFL}+V_{RHL}\times0.63791$	$V_{R18}+V_{RHL}\times1/140$	$V_{R18}+V_{RHL}\times2/140$	$V_{R18}+V_{RHL}\times3/140$
13h	V_{19}	$V_{R19}-V_{RHL}\times4/150$	$V_{R19}-V_{RHL}\times3/150$	$V_{R19}-V_{RHL}\times2/150$	$V_{R19}-V_{RHL}\times1/150$	$V_{R19}=V_{REFL}+V_{RHL}\times0.62916$	$V_{R19}+V_{RHL}\times1/150$	$V_{R19}+V_{RHL}\times2/150$	$V_{R19}+V_{RHL}\times3/150$
14h	V_{20}	$V_{R20}-V_{RHL}\times4/160$	$V_{R20}-V_{RHL}\times3/160$	$V_{R20}-V_{RHL}\times2/160$	$V_{R20}-V_{RHL}\times1/160$	$V_{R20}=V_{REFL}+V_{RHL}\times0.61981$	$V_{R20}+V_{RHL}\times1/160$	$V_{R20}+V_{RHL}\times2/160$	$V_{R20}+V_{RHL}\times3/160$
15h	V_{21}	$V_{R21}-V_{RHL}\times4/160$	$V_{R21}-V_{RHL}\times3/160$	$V_{R21}-V_{RHL}\times2/160$	$V_{R21}-V_{RHL}\times1/160$	$V_{R21}=V_{REFL}+V_{RHL}\times0.61281$	$V_{R21}+V_{RHL}\times1/160$	$V_{R21}+V_{RHL}\times2/160$	$V_{R21}+V_{RHL}\times3/160$
16h	V_{22}	$V_{R22}-V_{RHL}\times4/160$	$V_{R22}-V_{RHL}\times3/160$	$V_{R22}-V_{RHL}\times2/160$	$V_{R22}-V_{RHL}\times1/160$	$V_{R22}=V_{REFL}+V_{RHL}\times0.60476$	$V_{R22}+V_{RHL}\times1/160$	$V_{R22}+V_{RHL}\times2/160$	$V_{R22}+V_{RHL}\times3/160$
17h	V_{23}	$V_{R23}-V_{RHL}\times4/160$	$V_{R23}-V_{RHL}\times3/160$	$V_{R23}-V_{RHL}\times2/160$	$V_{R23}-V_{RHL}\times1/160$	$V_{R23}=V_{REFL}+V_{RHL}\times0.59755$	$V_{R23}+V_{RHL}\times1/160$	$V_{R23}+V_{RHL}\times2/160$	$V_{R23}+V_{RHL}\times3/160$
18h	V_{24}	$V_{R24}-V_{RHL}\times4/170$	$V_{R24}-V_{RHL}\times3/170$	$V_{R24}-V_{RHL}\times2/170$	$V_{R24}-V_{RHL}\times1/170$	$V_{R24}=V_{REFL}+V_{RHL}\times0.59029$	$V_{R24}+V_{RHL}\times1/170$	$V_{R24}+V_{RHL}\times2/170$	$V_{R24}+V_{RHL}\times3/170$
19h	V_{25}	$V_{R25}-V_{RHL}\times4/180$	$V_{R25}-V_{RHL}\times3/180$	$V_{R25}-V_{RHL}\times2/180$	$V_{R25}-V_{RHL}\times1/180$	$V_{R25}=V_{REFL}+V_{RHL}\times0.58331$	$V_{R25}+V_{RHL}\times1/180$	$V_{R25}+V_{RHL}\times2/180$	$V_{R25}+V_{RHL}\times3/180$
1Ah	V_{26}	$V_{R26}-V_{RHL}\times4/190$	$V_{R26}-V_{RHL}\times3/190$	$V_{R26}-V_{RHL}\times2/190$	$V_{R26}-V_{RHL}\times1/190$	$V_{R26}=V_{REFL}+V_{RHL}\times0.57643$	$V_{R26}+V_{RHL}\times1/190$	$V_{R26}+V_{RHL}\times2/190$	$V_{R26}+V_{RHL}\times3/190$
1Bh	V_{27}	$V_{R27}-V_{RHL}\times4/190$	$V_{R27}-V_{RHL}\times3/190$	$V_{R27}-V_{RHL}\times2/190$	$V_{R27}-V_{RHL}\times1/190$	$V_{R27}=V_{REFL}+V_{RHL}\times0.57074$	$V_{R27}+V_{RHL}\times1/190$	$V_{R27}+V_{RHL}\times2/190$	$V_{R27}+V_{RHL}\times3/190$
1Ch	V_{28}	$V_{R28}-V_{RHL}\times4/190$	$V_{R28}-V_{RHL}\times3/190$	$V_{R28}-V_{RHL}\times2/190$	$V_{R28}-V_{RHL}\times1/190$	$V_{R28}=V_{REFL}+V_{RHL}\times0.56439$	$V_{R28}+V_{RHL}\times1/190$	$V_{R28}+V_{RHL}\times2/190$	$V_{R28}+V_{RHL}\times3/190$
1Dh	V_{29}	$V_{R29}-V_{RHL}\times4/200$	$V_{R29}-V_{RHL}\times3/200$	$V_{R29}-V_{RHL}\times2/200$	$V_{R29}-V_{RHL}\times1/200$	$V_{R29}=V_{REFL}+V_{RHL}\times0.55778$	$V_{R29}+V_{RHL}\times1/200$	$V_{R29}+V_{RHL}\times2/200$	$V_{R29}+V_{RHL}\times3/200$
1Eh	V_{30}	$V_{R30}-V_{RHL}\times4/210$	$V_{R30}-V_{RHL}\times3/210$	$V_{R30}-V_{RHL}\times2/210$	$V_{R30}-V_{RHL}\times1/210$	$V_{R30}=V_{REFL}+V_{RHL}\times0.55127$	$V_{R30}+V_{RHL}\times1/210$	$V_{R30}+V_{RHL}\times2/210$	$V_{R30}+V_{RHL}\times3/210$
1Fh	V_{31}	$V_{R31}-V_{RHL}\times4/210$	$V_{R31}-V_{RHL}\times3/210$	$V_{R31}-V_{RHL}\times2/210$	$V_{R31}-V_{RHL}\times1/210$	$V_{R31}=V_{REFL}+V_{RHL}\times0.54623$	$V_{R31}+V_{RHL}\times1/210$	$V_{R31}+V_{RHL}\times2/210$	$V_{R31}+V_{RHL}\times3/210$
20h	V_{32}	$V_{R32}-V_{RHL}\times4/210$	$V_{R32}-V_{RHL}\times3/210$	$V_{R32}-V_{RHL}\times2/210$	$V_{R32}-V_{RHL}\times1/210$	$V_{R32}=V_{REFL}+V_{RHL}\times0.54103$	$V_{R32}+V_{RHL}\times1/210$	$V_{R32}+V_{RHL}\times2/210$	$V_{R32}+V_{RHL}\times3/210$
21h	V_{33}	$V_{R33}-V_{RHL}\times4/210$	$V_{R33}-V_{RHL}\times3/210$	$V_{R33}-V_{RHL}\times2/210$	$V_{R33}-V_{RHL}\times1/210$	$V_{R33}=V_{REFL}+V_{RHL}\times0.53432$	$V_{R33}+V_{RHL}\times1/210$	$V_{R33}+V_{RHL}\times2/210$	$V_{R33}+V_{RHL}\times3/210$
22h	V_{34}	$V_{R34}-V_{RHL}\times4/210$	$V_{R34}-V_{RHL}\times3/210$	$V_{R34}-V_{RHL}\times2/210$	$V_{R34}-V_{RHL}\times1/210$	$V_{R34}=V_{REFL}+V_{RHL}\times0.52788$	$V_{R34}+V_{RHL}\times1/210$	$V_{R34}+V_{RHL}\times2/210$	$V_{R34}+V_{RHL}\times3/210$
23h	V_{35}	$V_{R35}-V_{RHL}\times4/210$	$V_{R35}-V_{RHL}\times3/210$	$V_{R35}-V_{RHL}\times2/210$	$V_{R35}-V_{RHL}\times1/210$	$V_{R35}=V_{REFL}+V_{RHL}\times0.52134$	$V_{R35}+V_{RHL}\times1/210$	$V_{R35}+V_{RHL}\times2/210$	$V_{R35}+V_{RHL}\times3/210$
24h	V_{36}	$V_{R36}-V_{RHL}\times4/210$	$V_{R36}-V_{RHL}\times3/210$	$V_{R36}-V_{RHL}\times2/210$	$V_{R36}-V_{RHL}\times1/210$	$V_{R36}=V_{REFL}+V_{RHL}\times0.51568$	$V_{R36}+V_{RHL}\times1/210$	$V_{R36}+V_{RHL}\times2/210$	$V_{R36}+V_{RHL}\times3/210$
25h	V_{37}	$V_{R37}-V_{RHL}\times4/210$	$V_{R37}-V_{RHL}\times3/210$	$V_{R37}-V_{RHL}\times2/210$	$V_{R37}-V_{RHL}\times1/210$	$V_{R37}=V_{REFL}+V_{RHL}\times0.50976$	$V_{R37}+V_{RHL}\times1/210$	$V_{R37}+V_{RHL}\times2/210$	$V_{R37}+V_{RHL}\times3/210$
26h	V_{38}	$V_{R38}-V_{RHL}\times4/210$	$V_{R38}-V_{RHL}\times3/210$	$V_{R38}-V_{RHL}\times2/210$	$V_{R38}-V_{RHL}\times1/210$	$V_{R38}=V_{REFL}+V_{RHL}\times0.50346$	$V_{R38}+V_{RHL}\times1/210$	$V_{R38}+V_{RHL}\times2/210$	$V_{R38}+V_{RHL}\times3/210$
27h	V_{39}	$V_{R39}-V_{RHL}\times4/220$	$V_{R39}-V_{RHL}\times3/220$	$V_{R39}-V_{RHL}\times2/220$	$V_{R39}-V_{RHL}\times1/220$	$V_{R39}=V_{REFL}+V_{RHL}\times0.49815$	$V_{R39}+V_{RHL}\times1/220$	$V_{R39}+V_{RHL}\times2/220$	$V_{R39}+V_{RHL}\times3/220$
28h	V_{40}	$V_{R40}-V_{RHL}\times4/220$	$V_{R40}-V_{RHL}\times3/220$	$V_{R40}-V_{RHL}\times2/220$	$V_{R40}-V_{RHL}\times1/220$	$V_{R40}=V_{REFL}+V_{RHL}\times0.49316$	$V_{R40}+V_{RHL}\times1/220$	$V_{R40}+V_{RHL}\times2/220$	$V_{R40}+V_{RHL}\times3/220$
29h	V_{41}	$V_{R41}-V_{RHL}\times4/210$	$V_{R41}-V_{RHL}\times3/210$	$V_{R41}-V_{RHL}\times2/210$	$V_{R41}-V_{RHL}\times1/210$	$V_{R41}=V_{REFL}+V_{RHL}\times0.48798$	$V_{R41}+V_{RHL}\times1/210$	$V_{R41}+V_{RHL}\times2/210$	$V_{R41}+V_{RHL}\times3/210$
2Ah	V_{42}	$V_{R42}-V_{RHL}\times4/200$	$V_{R42}-V_{RHL}\times3/200$	$V_{R42}-V_{RHL}\times2/200$	$V_{R42}-V_{RHL}\times1/200$	$V_{R42}=V_{REFL}+V_{RHL}\times0.48255$	$V_{R42}+V_{RHL}\times1/200$	$V_{R42}+V_{RHL}\times2/200$	$V_{R42}+V_{RHL}\times3/200$
2Bh	V_{43}	$V_{R43}-V_{RHL}\times4/200$	$V_{R43}-V_{RHL}\times3/200$	$V_{R43}-V_{RHL}\times2/200$	$V_{R43}-V_{RHL}\times1/200$	$V_{R43}=V_{REFL}+V_{RHL}\times0.47716$	$V_{R43}+V_{RHL}\times1/200$	$V_{R43}+V_{RHL}\times2/200$	$V_{R43}+V_{RHL}\times3/200$
2Ch	V_{44}	$V_{R44}-V_{RHL}\times4/200$	$V_{R44}-V_{RHL}\times3/200$	$V_{R44}-V_{RHL}\times2/200$	$V_{R44}-V_{RHL}\times1/200$	$V_{R44}=V_{REFL}+V_{RHL}\times0.47143$	$V_{R44}+V_{RHL}\times1/200$	$V_{R44}+V_{RHL}\times2/200$	$V_{R44}+V_{RHL}\times3/200$
2Dh	V_{45}	$V_{R45}-V_{RHL}\times4/200$	$V_{R45}-V_{RHL}\times3/200$	$V_{R45}-V_{RHL}\times2/200$	$V_{R45}-V_{RHL}\times1/200$	$V_{R45}=V_{REFL}+V_{RHL}\times0.46609$	$V_{R45}+V_{RHL}\times1/200$	$V_{R45}+V_{RHL}\times2/200$	$V_{R45}+V_{RHL}\times3/200$
2Eh	V_{46}	$V_{R46}-V_{RHL}\times4/200$	$V_{R46}-V_{RHL}\times3/200$	$V_{R46}-V_{RHL}\times2/200$	$V_{R46}-V_{RHL}\times1/200$	$V_{R46}=V_{REFL}+V_{RHL}\times0.46060$	$V_{R46}+V_{RHL}\times1/200$	$V_{R46}+V_{RHL}\times2/200$	$V_{R46}+V_{RHL}\times3/200$
2Fh	V_{47}	$V_{R47}-V_{RHL}\times4/200$	$V_{R47}-V_{RHL}\times3/200$	$V_{R47}-V_{RHL}\times2/200$	$V_{R47}-V_{RHL}\times1/200$	$V_{R47}=V_{REFL}+V_{RHL}\times0.45484$	$V_{R47}+V_{RHL}\times1/200$	$V_{R47}+V_{RHL}\times2/200$	$V_{R47}+V_{RHL}\times3/200$
30h	V_{48}	$V_{R48}-V_{RHL}\times4/200$	$V_{R48}-V_{RHL}\times3/200$	$V_{R48}-V_{RHL}\times2/200$	$V_{R48}-V_{RHL}\times1/200$	$V_{R48}=V_{REFL}+V_{RHL}\times0.44927$	$V_{R48}+V_{RHL}\times1/200$	$V_{R48}+V_{RHL}\times2/200$	$V_{R48}+V_{RHL}\times3/200$
31h	V_{49}	$V_{R49}-V_{RHL}\times4/200$	$V_{R49}-V_{RHL}\times3/200$	$V_{R49}-V_{RHL}\times2/200$	$V_{R49}-V_{RHL}\times1/200$	$V_{R49}=V_{REFL}+V_{RHL}\times0.44382$	$V_{R49}+V_{RHL}\times1/200$	$V_{R49}+V_{RHL}\times2/200$	$V_{R49}+V_{RHL}\times3/200$
32h	V_{50}	$V_{R50}-V_{RHL}\times4/190$	$V_{R50}-V_{RHL}\times3/190$	$V_{R50}-V_{RHL}\times2/190$	$V_{R50}-V_{RHL}\times1/190$	$V_{R50}=V_{REFL}+V_{RHL}\times0.43807$	$V_{R50}+V_{RHL}\times1/190$	$V_{R50}+V_{RHL}\times2/190$	$V_{R50}+V_{RHL}\times3/190$
33h	V_{51}	$V_{R51}-V_{RHL}\times4/190$	$V_{R51}-V_{RHL}\times3/190$	$V_{R51}-V_{RHL}\times2/190$	$V_{R51}-V_{RHL}\times1/190$	$V_{R51}=V_{REFL}+V_{RHL}\times0.43216$	$V_{R51}+V_{RHL}\times1/190$	$V_{R51}+V_{RHL}\times2/190$	$V_{R51}+V_{RHL}\times3/190$
34h	V_{52}	$V_{R52}-V_{RHL}\times4/180$	$V_{R52}-V_{RHL}\times3/180$	$V_{R52}-V_{RHL}\times2/180$	$V_{R52}-V_{RHL}\times1/180$	$V_{R52}=V_{REFL}+V_{RHL}\times0.42606$	$V_{R52}+V_{RHL}\times1/180$	$V_{R52}+V_{RHL}\times2/180$	$V_{R52}+V_{RHL}\times3/180$
35h	V_{53}	$V_{R53}-V_{RHL}\times4/170$	$V_{R53}-V_{RHL}\times3/170$	$V_{R53}-V_{RHL}\times2/170$	$V_{R53}-V_{RHL}\times1/170$	$V_{R53}=V_{REFL}+V_{RHL}\times0.41858$	$V_{R53}+V_{RHL}\times1/170$	$V_{R53}+V_{RHL}\times2/170$	$V_{R53}+V_{RHL}\times3/170$
36h	V_{54}	$V_{R54}-V_{RHL}\times4/170$	$V_{R54}-V_{RHL}\times3/170$	$V_{R54}-V_{RHL}\times2/170$	$V_{R54}-V_{RHL}\times1/170$	$V_{R54}=V_{REFL}+V_{RHL}\times0.41224$	$V_{R54}+V_{RHL}\times1/170$	$V_{R54}+V_{RHL}\times2/170$	$V_{R54}+V_{RHL}\times3/170$
37h	V_{55}	$V_{R55}-V_{RHL}\times4/170$	$V_{R55}-V_{RHL}\times3/170$	$V_{R55}-V_{RHL}\times2/170$	$V_{R55}-V_{RHL}\times1/170$	$V_{R55}=V_{REFL}+V_{RHL}\times0.40605$	$V_{R55}+V_{RHL}\times1/170$	$V_{R55}+V_{RHL}\times2/170$	$V_{R55}+V_{RHL}\times3/170$
38h	V_{56}	$V_{R56}-V_{RHL}\times4/160$	$V_{R56}-V_{RHL}\times3/160$	$V_{R56}-V_{RHL}\times2/160$	$V_{R56}-V_{RHL}\times1/160$	$V_{R56}=V_{REFL}+V_{RHL}\times0.39911$	$V_{R56}+V_{RHL}\times1/160$	$V_{R56}+V_{RHL}\times2/160$	$V_{R56}+V_{RHL}\times3/160$
39h	V_{57}	$V_{R57}-V_{RHL}\times4/150$	$V_{R57}-V_{RHL}\times3/150$	$V_{R57}-V_{RHL}\times2/150$	$V_{R57}-V_{RHL}\times1/150$	$V_{R57}=V_{REFL}+V_{RHL}\times0.39145$	$V_{R57}+V_{RHL}\times1/150$	$V_{R57}+V_{RHL}\times2/150$	$V_{R57}+V_{RHL}\times3/150$
3Ah	V_{58}	$V_{R58}-V_{RHL}\times4/140$	$V_{R58}-V_{RHL}\times3/140$	$V_{R58}-V_{RHL}\times2/140$	$V_{R58}-V_{RHL}\times1/140$	$V_{R58}=V_{REFL}+V_{RHL}\times0.38271$	$V_{R58}+V_{RHL}\times1/140$	$V_{R58}+V_{RHL}\times2/140$	$V_{R58}+V_{RHL}\times3/140$
3Bh	V_{59}	$V_{R59}-V_{RHL}\times4/130$	$V_{R59}-V_{RHL}\times3/130$	$V_{R59}-V_{RHL}\times2/130$	$V_{R59}-V_{RHL}\times1/130$	$V_{R59}=V_{REFL}+V_{RHL}\times0.37224$	$V_{R59}+V_{RHL}\times1/130$	$V_{R59}+V_{RHL}\times2/130$	$V_{R59}+V_{RHL}\times3/130$
3Ch	V_{60}	$V_{R60}-V_{RHL}\times4/120$	$V_{R60}-V_{RHL}\times3/120$	$V_{R60}-V_{RHL}\times2/120$	$V_{R60}-V_{RHL}\times1/120$	$V_{R60}=V_{REFL}+V_{RHL}\times0.36042$	$V_{R60}+V_{RHL}\times1/120$	$V_{R60}+V_{RHL}\times2/120$	$V_{R60}+V_{RHL}\times3/120$
3Dh	V_{61}	$V_{R61}-V_{RHL}\times4/100$	$V_{R61}-V_{RHL}\times3/100$	$V_{R61}-V_{RHL}\times2/100$	$V_{R61}-V_{RHL}\times1/100$	$V_{R61}=V_{REFL}+V_{RHL}\times0.34276$	$V_{R61}+V_{RHL}\times1/100$	$V_{R61}+V_{RHL}\times2/100$	$V_{R61}+V_{RHL}\times3/100$
3Eh	V_{62}	$V_{R62}-V_{RHL}\times4/80$	$V_{R62}-V_{RHL}\times3/80$	$V_{R62}-V_{RHL}\times2/80$	$V_{R62}-V_{RHL}\times1/80$	$V_{R62}=V_{REFL}+V_{RHL}\times0.31375$	$V_{R62}+V_{RHL}\times1/80$	$V_{R62}+V_{RHL}\times2/80$	$V_{R62}+V_{RHL}\times3/80$
3Fh	V_{63}					V_{REFL}			

V_{RHL} value shown in the above is specified as follows:

● $V_{RHL}=V_{REFH}-V_{REFL}$

(4) Relationship of Input Data Values and Output Voltage Changes (with VREFH Set to 3.5 V and VREFL Set to 0 V)



6.6 Gate Driver Settings

6.6.1 Setting Number of Gate Driver Outputs

The IC has a GRAM that supports a maximum of 176 pixels (× RGB) × 240 lines to be displayed.
On the other hand, the MN863480 gate driver used in combination supports 160-, 176-, 192-, 220-, or 240-line output.
The IC generates drive signals supporting 192, 220, or 240 lines.
The settings are made in the GSL (gate driver scan line) [2:0] bits of the driver setting 1 register.
Note1) Gate driver (MN863480) settings will be reflected by specifying the transfer of corresponding commands to the gate driver.
Refer to Section 6.7.2 for the specifications of command transfer.
Note2) For MN838893, GSL[2] set to 1

GSL[2:0]	MN863480	MN838892	MN838893
	Gate driver output	Controller setting	Controller setting
00x	160 outputs	160 outputs	Setting prohibited
01x	176 outputs	176 outputs	
10x	192 outputs	Setting prohibited	192 outputs
110	220 outputs		220 outputs
111	240 outputs		240 outputs

* Initial value: GSL[2:0] = 110 (220-line output)

6.6.2 Gate Driver Scan Operation Settings

The gate driver shift direction is set in the GDIR bit of the driver setting 1 register.
The scan method of the output pins of the gate driver is set according to the mounting method in the GSCN and GCHS[1:0] bits.
Note) Gate driver (MN863480) settings will be reflected by specifying the transfer of corresponding commands to the gate driver.
Refer to Section 6.7.2 for the specifications of command transfer.

GDIR	MN863480
	Shift direction
0	1→240
1	240→1

* Initial value: GDIR=0 (1→240 shift)

GSCN	MN863480
	Scan mode
0	Single-side connection mode
1	Both-side connection mode

* Initial value: GSCN=0

GCHS [1:0]	MN863480					
	Disabled output channel					
	Mode	240 output	220 output	192 output	176 output	160 output
00	Center output disabled	All enabled	X111 to X130	X97 to X144	X89 to X152	X81 to X160
01	X240-side output disabled	Setting prohibited	X221 to X240	X193 to X240	X177 to X240	X161 to X240
10	X1-side output disabled	Setting prohibited	X1 to X20	X1 to X48	X1 to X64	X1 to X80
11	Setting prohibited					

* Initial value: GCHS=00

• The GCHS bit is enabled when the GSCN is set to 0. When the GSCN is set to 1, set the GCHS[1:0] to 00.

• See the Specifications of the MN863480 for the detailed operation of the gate driver in the above combinations.

6.7 Power Supply IC Settings

The power supply circuit of the MN863480, which is used together, will be set by executing command transfer to the MN863480 after command register settings are made in this IC.
The following section describes the outline of the settings. For details, see Section 7 Command Function and the Specifications of the MN863480.

6.7.1 Voltage Step-up Clock Control

(1) Generation of Voltage Step-up Clock Pulses

Voltage step-up clock DDCK pulses are generated from the internal oscillation circuit.
The frequency of the clock is adjustable by the operating mode set command DDCKF[1:0] for the power supply system.

Table 6.7.1 Frequency Settings for Voltage Step-up Clock

DDCKF[1:0]	DDCK cycle (1H: 11 clock pulses)
00	1H (18.8 kHz)
01	Standard value × 1/4 (51.7 kHz)
10	Standard value × 1/2 (103.3 kHz)
11	Standard value × 1 (206.6 kHz)

<Reference>
If the standard oscillator frequency (206.6 kHz) is used and 1H is 11 clock pulses according to the HCNT bit, the following frequency will be obtained.
1H = 206 kHz ÷ 11 = 18.78 kHz

If the DDCKF is set to 00 and the number of clock pulses for each 1H period is an odd number (2n + 1), the high-level duty period of the DDCK clock toggles between (n +1) and (n) clock pulses between lines.
Both the high- and low-level periods will have n clock pulses when the number of clock pulses for a 1H period is an even number (2n).

(2) Voltage Step-up Clock Adjustments in Power Supply IC

The voltage step-up clock DDCK is adjusted by making usage settings in the DDC[2:0] bits in power supply IC.

6.7.2 Power Supply Circuit Operation/Stop Control

(1) Power Control Register

The power supply IC operation/adjustment command is executed to change the voltage step-up rate and operational amplifier capability adjustment along with the start and stop of the four-line power supply circuits.

Table 6.7.2 (1) Power Supply Circuit Start Control

Control bit	DDCK cycle
CPA[1:0]	Voltage step-up circuit 1
CPB[1:0]	Voltage step-up circuits 2 to 5
AMP[3:0]	Operational amplifier capability settings

If each control bit is set to 0, the power supply circuit will stop. For details, refer to Section 7 Command Function and the Specifications of the MN863480.

(2) Stop Control Commands for Power Supply Circuit

The bits explained below are prepared in the MN863480 command transfer register in address 71h to control the power supply after the operation of the power supply is interrupted. The following control is possible by using the bits in combination while executing command transfer.

Table 6.7.2 (2) Control at the Time of Power Supply Circuit Interruption

Control bit	Explanation
SLP	Used to transfer commands while the power supply circuit is not operating. The DDCK will stop with the SLP set to 1. Command transfer is possible with a single register access. The register value will be kept on hold.
DSCG	Used to perform command transfer to stop the operation of the power supply circuit and discharge electricity from the output pin of the power supply IC. The DDCK will stop with the DSCG set to 1.
XDON	Used to turn on the whole gate driver. After register settings, the command will be issued from the XDON pin. The DDCK will stop with the XDON set to 1. The electricity of the LCD panel will be instantaneously discharged. Therefore, this bit may be used to take immediate countermeasures against the dropping out of the battery.

6.7.3 Each Voltage Setting

The following voltage settings are made for the MN863480.

Table 6.7.3 (1) Each Voltage Setting 1

Name	Explanation	Control bit		Possible voltage range
AV_{DD}	Power source for source driver LCD drive system	CPA[1:0]	Used to set the voltage step-up rate for AV_{DD} generation	3.5 V to 5.5 V
		AVD[3:0]	Fine voltage adjustment for AV_{DD} generation	
V_{REFH}	Reference voltage to drive source driver gradation	VRFH[4:0]	V_{REFH} voltage adjustment	3.0 V to AV_{DD} - 0.5 V
VCOM	Opposite electrode (set high-level voltage and amplitude because the current alternates)	VCMH[5:0]	VCOMH voltage adjustment	<VCOMH> 1.0 V to V_{REFH} <Amplitude> 2.0 V to 6.0 V
		VCMPL[4:0]	VCOM amplitude adjustment	
VOFF	Gate driver OFF potential (set intermediate voltage and amplitude because the current alternates)	VOFFL[4:0]	VOFFL voltage adjustment	<VOFFL> -4 V to VEE + 0.5 V <Amplitude> 2.0 V to 9.0 V Provided, VOFFH ≤ –2 V
		VOFFPL[5:0]	VOFF amplitude adjustment	
VGG	VGG/VEE potential of gate driver	CPB[1:0]	VGG/VEE step-up voltage multiplication rate setting	± 9.4 V to 17.5 V

Table 6.7.3 (2) Each Voltage Setting 2

Name	Explanation	Control bit		Possible voltage range
VCOM	Opposite electrode	VCMG	VCOM/VOFF operation settings	Both fixed at ground level when both VCOM and VOFF set to 0.
VOFF	Gate driver OFF potential			
VCOM VOFF	Amplifier capability specifications	LPM[2:0]	Capability adjustments	See the specifications of the gate driver.

6.8 Command Transfer to MN863480 (Gate Driver/Power Supply IC)

The MN863480 (gate driver/power supply IC), which is used in combination with this IC, is controlled as specified below.

(1) Set the gate driver/power supply IC control register of the IC.

(2) Set 1 to the DTRN bit for serial transfer of commands.

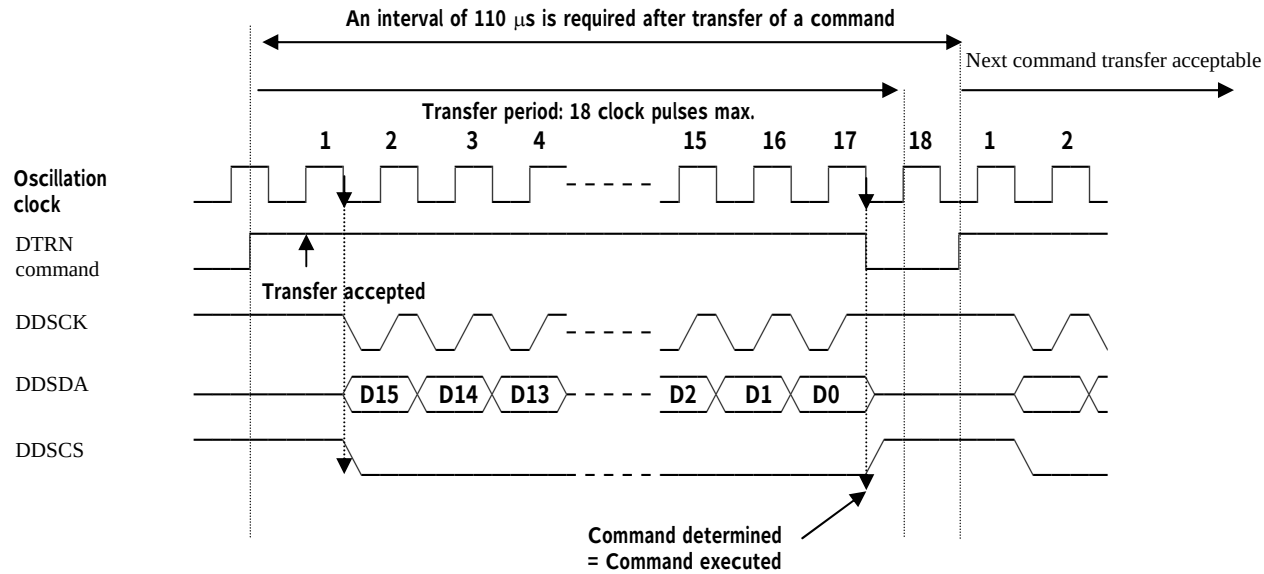
Command transfer is performed with the clock of the built-in oscillation circuit as explained below. The completion of command transfer requires a maximum of 18 clock pulses. On completion of command transfer, the DTRN bit will be automatically cleared and set to 0.

Note:

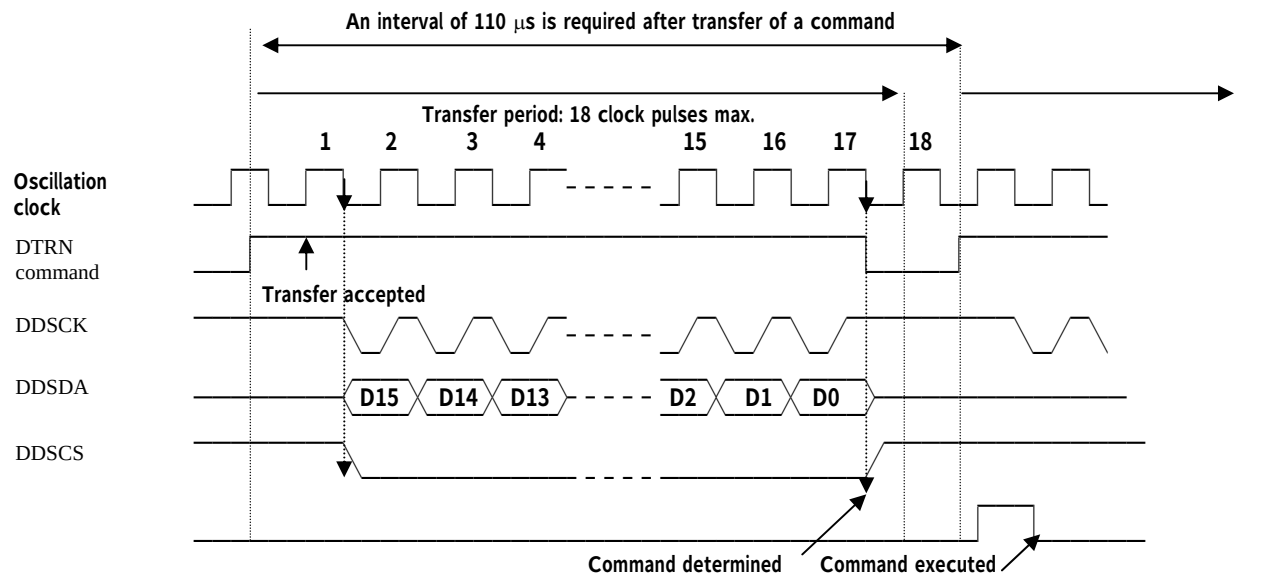
The next command can be transferred after a minimum interval of 110 μs, otherwise the command will not be transferred.

If the DTRN bit is set to 0 while in transfer, nothing will be transferred.

<Command, except Index(100)>



<Command for Index(100)>



7. Command Function

7.1 List of Command

7.1.1 Memory Control Command

Memory Control Command (1)

Address	Function	RW	Data		Description			Default
00h	Memory operation mode	RW	D7	ADIR	Address increment direction	0	X direction	0
						1	Y direction	
			D6	XDIR	X address direction	0	Non-reverse	0
						1	Reverse	
			D5	YDIR	Y address direction	0	Non-reverse	0
						1	Reverse	
			D4	BODR	Used to specify GRAM write data in 16-bit, 260000-color mode.	0	16 bits × 2: Right aligned	0
						1	16 bits × 2: Left aligned	
			D3	AEMODE	Access range end-point specification mode	0	Specify end address	0
						1	Specify access width less 1	
			D2	**SDIR**	**Source driver direction (in correspondence of GRAM X address "0" to "175" to driver output pin)**	**0**	**0→175**	**0**
						1	**175→0**	
			D[1:0]	Not used				
01h	Memory control command	RW	D7	WM	Used to execute window mask write	0	Normal	0
						1	Window mask mode	
			D6	WMMODE	Window mask mode	0	Inside window mask	0
						1	Outside window mask	
			D[5:4]	Not used				
			D3	RAMCLR	Used to clear the RAM. This bit will be automatically cleared after the RAM is cleared.	0	Normal	0
						1	Used to clear the RAM.	
			D[2:0]	CLR_COL [2:0]	Used to specify RAM clear color.	D[2]: R data		7h
						D[1]: G data		
						D[0]: B data		
02h	X start point of memory access range	RW	D[7:0]	XAS[7:0]	X start point	<AEMODE set to 0> The rectangular range of access to the GRAM is designated by the start point specified by XAS and YAS and the end-point specified by XAE and YAE. The following conditions must be satisfied. XAS < XAE YAS < YAE <AEMODE set to 1> The rectangular range of access to the GRAM is designated by the start point specified by XAS and YAS and the access width specified by XAE and YAE. In any case, the range must be within the effective range of the GRAM.		00h
03h	Y start point of memory access range	RW	D[7:0]	YAS[7:0]	Y start point			00h
04h	X end point of memory access range	RW	D[7:0]	XAE[7:0]	X end point			FEh
05h	Y end point of memory access range	RW	D[7:0]	YAE[7:0]	Y end point			FEh

Memory Control Command (2)

Address	Function	RW	Data		Description			Default
O6h	X start point of window mask range	RW	D[7:0]	WMXS[7:0]	X start address of window mask	The rectangular mask range of the GRAM is designated by the start point specified by the WMXS and WMYS and the end-point specified by the WMXE and WMYE. The WMXS, WMXE, WMYS, and WMYE must satisfy the following conditions. WMXS < WMXE WMYS < WMYE The range must be within the GRAM access range, otherwise the GRAM will not be masked correctly.		FFh
O7h	Y start point of window mask range	RW	D[7:0]	WMYS[7:0]	Y start address of window mask			FFh
O8h	X end point of window mask range	RW	D[7:0]	WMXE[7:0]	X end address of window mask			FFh
O9h	Y end point of window mask range	RW	D[7:0]	WMYE[7:0]	Y end address of window mask			FFh
OAh	Bit mask function 1	RW	D[7:6]	Not used				
			D[5:0]	BMSKR[5:0]	Bit mask setting R	0	Not masked	00h
						1	Masked	
OBh	Bit mask function 2	RW	D[7:6]	Not used				
			D[5:0]	BMSKG[5:0]	Bit mask setting G	0	Not masked	00h
						1	Masked	
OCh	Bit mask function 3	RW	D[7:6]	Not used				
			D[5:0]	BMSKB[5:0]	Bit mask setting B	0	Not masked	00h
						1	Masked	
ODh	GRAM interface mode	RW	**D[7:4]**	Not used				
			D3	**RGBSW**	**This bit assigns alignment swap for writing data from Host and RGB of source driver output.**	**0**	**Without swap (correspondence of R,G,B→YR,YG,YB)**	**0**
						1	**With swap (correspondence of R,G,B→YB,YG,YR)**	
			D2	RMWR	GRAM write port selection. Used to select the RGB or CPU interface as a write port to the GRAM	0	CPU interface mode	0
						1	RGB interface mode	
			D1	RGBIF	Used to set the bus width of the data pin for GRAM access when the RGB interface is used.	0	18-/16-bit mode	0
						1	8-/6-bit mode	
			D0	RMIF	GRAM transfer mode setting. Used to specify the number of bits of GRAM transfer data from the host. The method of data transfer from the host to the GRAM will be determined by this bit in combination with the IFMODE[1:0] pin or RGBIF bit setting.	0	18 bits (260,000 colors)	0
						1	16 bits (65,000 colors)	
OEh	Memory write	W	Display RAM write					
OFh	Memory read	RW	Display RAM read					

7.1.2 Display Control Command

10h	Display mode control	–	D[7:2]	Not used				
		RW	D[1:0]	DISP	Display mode	00	Display OFF (stop)	0
						01	All white display	
						10	Normal display	
						11	Partial display	
11h	Display system V sync mode	RW	D7	VSYMODE	Display system V sync mode	0	Internal V sync (self-running)	0
						1	External V sync	
		–	D[6:0]	Not used				
12h	Display data reversion	–	D[7:1]	Not used				
		RW	D0	DISPINV	Display data reversion	0	Normal	0
						1	Display data reversed	
13h	Partial scroll display	–	D[7:1]	Not used				
		RW	D0	SCRON	Partial scroll display ON	0	Normal	0
						1	Partial scroll display	
14h	Gradation LSB control	–	D[7:4]	Not used				
		RW	D[3:2]	RLSB[1:0]	RLSB control	00	RMSB is used	0
						01	Non-reverse/reverse pattern phase fixed	
						10	Reverse/non-reverse pattern phase fixed	
						11	Reverse/non-reverse pattern : Phase reversed frame by frame	
			D[1:0]	BLSB[1:0]	BLSB control	00	BMSB is used	0
						01	Non-reverse/reverse pattern phase fixed	
						10	Reverse/non-reverse pattern phase fixed	
						11	Reverse/non-reverse pattern : Phase reversed frame by frame	
15h	Display start line address	RW	D[7:0]	LAS[7:0]	Display start line address			00h
16h	Partial scroll setting 1	RW	D[7:0]	SCRN[7:0]	Number of scrolled lines setting			00h
17h	Partial scroll setting 2	RW	D[7:0]	SCRS[7:0]	Scroll area start point setting	Not enabled in FF mode		FFh
18h	Partial scroll setting 3	RW	D[7:0]	SCRE[7:0]	Scroll area end point setting			FFh
19h	Partial display setting 1	RW	D[7:0]	MASKS1[7:0]	Non-display area start point 1	Outside display area disabled		FFh
1Ah	Partial display setting 2	RW	D[7:0]	MASKE1[7:0]	Non-display area end point 1	Outside display area disabled		FFh
1Bh	Partial display setting 3	RW	D[7:0]	MASKS2[7:0]	Non-display area start point 2	Outside display area disabled		FFh
1Ch	Partial display setting 4	RW	D[7:0]	MASKE2[7:0]	Non-display area end point 2	Outside display area disabled		FFh
1Dh	Partial display setting 5	RW	D[7:0]	RFR[7:0]	Partial display refresh cycle	Cycle - 1 is set Initial value: 15 frames FFh: No refresh		0Eh
1Eh	H-cycle setting	–	D[7:5]	Not used				
		RW	D[4:0]	HCNT[4:0]	Setting number of 1H clock pulses - 1	Default value: 08h => 12 clock pulses		0Bh
1Fh	V-cycle setting	RW	D[7:0]	VCNT[9:2]	•Corresponds to the upper 8 bits of the V count •00h to FFh settings correspond to 4 to 1024 lines.	1V = (VCNT + 1) × 4H Default value: 1V = 300 lines		4Ah

7.1.3 LCD Driver Control Command

Address	Function	RW	Data		Description			Default
20h	Driver setting 1 (Usually used for initialization)	RW	D[7:5]	GSL[2:0]	Used to set the number of output points of the gate driver. Set 1 to the GSL[2].	10×	192 outputs	110
						110	220 outputs	
						111	240 outputs	
		RW	D4	GDIR	Gate driver shift direction	0	Non-reverse (1 to 240)	0
						1	Reverse (240 to 1)	
		RW	D[3]	GSCN	Used to set the scan mode of the gate driver according to the mounting method.	0	Panel single-side connection scan	0
						1	Panel both-side connection scan	
		RW	D[2:1]	GCHS[1:0]	Used to set the output channel point of the gate driver according to the mounting method. • Enabled when the GSCN is set to 0. Set the value to 00 when the GSCN is set to 1.	00	Center output disabled	00
						01	X240-side output disabled	
						10	X1-side output disabled	
						11	Setting prohibited	
		-	D[0]	Not used				1
21h	Driver setting 2 (Used to set the desired drive mode)	RW	D7	FRPOL	Used to set the alternation drive mode.	0	1H line alternation drive	0
						1	Frame alternation drive	
		RW	D[6:4]	SAMP[2:0]	Used to set the drive capability of the operation amplifier of the source driver.	000: Stop		011
						001 (lowest) to 101 (highest) Setting to 110 or 111 is prohibited.		
		RW	D[3]	AMPSWON	Used to control the output timing of the source driver at the time of gradation driving	0	1H before display	0
						1	4H before display	
		RW	D2	AMPON	Used to control amplifier drive within a period of 1H.	0	Drive according to the OEH*	0
						1	Normally driven	
		RW	D1	COL	Used to select gradation drive or binary drive.	0	Binary drive	1
						1	Gradation drive	
		RW	D0	RSWON	Used to turn on the connection of VREF resistor to the source driver during blanking periods while in gradation drive mode.	0	Off	1
						1	On	
22h	OEV assertion timing	-	D[7:5]	Not used		Assertion or negation will not be possible if any set value is larger than that in the HCNT register set value (i.e., the number of clocks for a period of 1H). (If the initial value HCNT is set to 0Bh, the set value must be 0Bh or less.) If OE*A > OE*N, the waveform will be inverted. (Priority is given to negation if OE*A = CE*N.)			00h
		RW	D[4:0]	OEVA[4:0]	OEV assertion timing (Number of CKs)			
23h	OEV negation timing	-	D[7:5]	Not used				00h
		RW	D[4:0]	OEVN[4:0]	OEV negation timing (Number of CKs)			
24h	OEH assertion timing	-	D[7:5]	Not used				00h
		RW	D[4:0]	OEHA[4:0]	Source drive timing(Number of CKs)			
25h	OEH negation timing	-	D[7:5]	Not used				00h
		RW	D[4:0]	OEHN[4:0]	Source stop timing(Number of CKs)			
26h	Source driver drive (NOEH) expansion timing	RW	D7	BLKSD	Used to set drive data in continuous source driving during vertical blanking.	0	VREFH level	1
						1	VREFL level	
		RW	D6	OEHON	Used to control the source driver drive during vertical blanking.	0	Driven according to OEHE.	0
						1	NOEH: Always ON.	
		RW	D[5:0]	OEHE[5:0]	Number of continuous source drive lines (0 to 63 CKV) during vertical blanking. The initial value is 2 lines.			02h
27h	VCOM drive (VCOMEN) expansion timing	-	D7	Not used				
		RW	D6	VCOMON	Used to control the VCOM drive during vertical blanking.	0	Driven according to the VCOME.	0
						1	Normally driven	
		RW	D[5:0]	VCOME[5:0]	Number of continuous VCOM drive lines during vertical blanking (0 to 63 CKV) The initial value is 1 line.			01h

7.1.4 Image Quality Adjustment Command

Address	Function	RW	Data		Description			Default
28h	R color adjustment	-	D[7:6]	Not used				
		RW	D5	RADJ[5]	Used to specify data addition or subtraction.	1	Subtraction	0
						0	Addition	
			D[4:0]	RADJ[4:0]	Used to specify the quantity of data for red adjustment. The data will be added to or subtracted from R_RAM data R[5:0].			00h
29h	G color adjustment	-	D[7:6]	Not used				
		RW	D5	GADJ[5]	Used to specify data addition or subtraction.	1	Subtraction	0h
						0	Addition	
			D[4:0]	GADJ[4:0]	Used to specify the quantity of data for green adjustment. The data will be added to or subtracted from G_RAM data G[5:0].			00h
2Ah	B color adjustment	-	D[7:6]	Not used				
		RW	D5	BADJ[5]	Used to specify data addition or subtraction.	1	Subtraction	0h
						0	Addition	
			D[4:0]	BADJ[4:0]	Used to specify the quantity of data for blue adjustment. The data will be added to or subtracted from B_RAM data B[5:0].			00h
2Bh to 30h		-	D[7:0]	Not used				
31h to 6Eh	Gamma adjustment	-	D7	Not used				
		W	D[6:4]	GMPn	Gamma correction control during positive driving. n: 1 to 62n corresponds to addresses 30h + n.			04h
		-	D3	Not used				
		W	D[2:0]	GMNn	Gamma correction control during negative driving. n: 1 to 62n corresponds to addresses 30h + n.			04h
6Fh		-	D[7:0]	Not used				

7.1.5 Power Supply System Control Command

Power Supply System Control Command 1

Address	Function	RW	Data		Description			Default
70h	Power supply system operation mode	RW	D[7]	OSCON	Oscillation clock operation control	0	Stop	0
						1	Output	
		RW	D[6]	DDCKON	Voltage step-up clock output control (Fixed at low level when the clock stops).	0	Stop	0
						1	Output	
		RW	D[5:4]	DDCKF[1:0]	Used to set the frequency dividing ratio of the step-up clock DDCK.	00	1H	00
						01	Original oscillation clock × 1/4	
						10	Original oscillation clock x 1/2	
						11	Original oscillation clock x 1	
		RW	D[3]	VCMG	Used to set VCOM output and VOFF output operation of the MN863480.	0	Both fixed at ground level	0
						1	Normal operation	
		RW	D[2:0]	DDC[2:0]	Used to set the method of using the voltage step-up clock for the MN863480. Used to adjust the capability of the voltage step-up circuit. Set the value between 000 and 111.			000
71h	Command transfer to MN863480	–	D[7]		Not used			
		RW	D[6:4]	DIDX[2:0]	Used to specify command transfer data to the MN863480.			0h
			D[3]	XDON	Used to ON-control of the whole gate driver.	0	Normal	0
						1	Whole gate ON	
			D[2]	DSCG	Used to specify the discharging of the power supply IC.	0	Normal	0
						1	Discharge specified	
			D[1]	SLP	Used to control the sleep mode.	0	Normal	0
						1	Sleep mode specified	
			D[0]	DTRN	Used to transfer MN863480 control commands in series.	0	Standby	0
						1	Transfer	
72h	MN863480 Power control (Adjustments to the multiplication ratio, capability, operation/stop control of the voltage step-up circuit and operational amplifier)	RW	D[7:6]	CPA[1:0]	Setting of voltage step-up circuit 1. See Specifications of MN863480.	00	Voltage step-up stop	00
						01	Voltage step-up stop	
						10	See the Specifications of the MN863480.	
						11	See the Specifications of the MN863480.	
		RW	D[5:4]	CPB[1:0]	Setting of voltage step-up circuits 3 and 4. See Specifications of MN863480.	00	Voltage step-up stop	00
						01	See the Specifications of the MN863480.	
						10	See the Specifications of the MN863480.	
						11	See the Specifications of the MN863480.	
		RW	D[3:0]	AMP[3:0]	Used to specify the capability of the amplifier of the power supply IC.	0000: Amplifier stop		0000
						See the Specifications of the MN863480.		

Power Supply System Control Command 2

Address	Function	RW	Data		Description		Default
73h	Power supply setting 1	RW	D[7:4]	Not used			
		RW	D[3:0]	AVD[3:0]	AV_{DD} voltage setting	A voltage of 3.5 V to 5.5 V Refer to the explanation about the command.	0h
74h	Power supply setting 2	RW	D[7:5]				
		RW	D[4:0]	VRFH[4:0]	V_{REFH} voltage setting (setting 18h to 1Fh prohibited)	A voltage of 3.0 V to 5.0 V Refer to the explanation about the command.	3h
75h	Power supply setting 3	RW	D[7:6]	Not used			
		RW	D[5:0]	VCMH[5:0]	VCOMH voltage setting	A voltage of 1.0 V to 5.5 V Refer to the explanation about the command.	0h
76h	Power supply setting 4	RW	D[7:5]	Not used			
		RW	D[4:0]	VCMPL[4:0]	VCOM amplitude setting	An amplitude of 2.0 V to 6.0 V Refer to the explanation about the command.	1h
77h	Power supply setting 5	RW	D[7:5]	Not used			
		RW	D[4:0]	VOFFL[4:0]	VOFFL voltage setting	A voltage of VEE+0.5 V to -4 V Refer to the explanation about the command.	1h
78h	Power supply setting 6	RW	D[7:6]	Not used			
		RW	D[5:0]	VOFFPL[5:0]	VOFF amplitude setting	An amplitude of 2.0 V to 9.0 V (Within the following range. VOFFL $\geqq$ VEE + 0.5 V; VOFFH $\leqq$ -2V) Refer to the explanation about the command.	1h
79h	Power supply circuit capability adjustment	RW	D[7:4]	CKVPW	Used to make CKV pulse width adjustments	1 to Fh settings will set the CKV's H width between 1 and 15 clocks. Set the value to 4h.	4h
		-	D[3]	Not used			
		RW	D[2:0]	LPM	Used to make capability adjustments to the VOFF and VCOM power supply circuit.	See the Specifications of the MN863480.	0h
7Ah	Software reset	-	D[7:1]	Not used			
		W	D[0]	SRESET	Used to initialize the register value. The OSCON bit will not be influenced.	The bit will be automatically cleared and set to 0 after the register is initialized. Enabled only when the clock is oscillating.	0

7.1.6 Details of Gate Driver/Power Supply IC (MN863480) Command Transfer

After the control register of the gate driver/power supply IC (MN863480) is set, the command with the following details will be transferred with the transfer command specified by the DIDX[2:0] set value and the DTRN set to 1.

After the automatic transfer of the command, the DTRN bit will be cleared automatically.

Then, by setting DIDX[2:0] to 111, the command to initialize the MN863480 will be transferred.

Transfer data														
DIDX[2:0]			Command											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	CPA[1:0]		CPB[1:0]		AMP[3:0]				DDC[2:0]			-	DSCG
0	0	1	VRFH[4:0]					AVD[3:0]				LPM[2:0]			-
0	1	0	VCMH[5:0]						VCMPL[4:0]					-	VCMG
0	1	1	0	–	VOFFL[4:0]					VOFFPL[5:0]					
1	0	0	GSL[2:0]			GDIR	GSCN	GCHS [1:0]		-	-	-	-	-	-
1	1	1	1	1	0	-	-	-	-	-	-	-	-	-	-

The following bits can be set while the transfer command is transferred (with the DTRN set to 1).

SLP set to 1: The DIDX[2:0] will be fixed at 000. Then, data on the CPA, CPB, and AMP bits all set to 0 will be transferred (i.e., the command to stop the power supply circuit will be transferred). Transfer data on the DSCG bit depends on the setting in the DSCG bit.
In the above case, the voltage step-up clock DDCK will automatically stop.

DSCG set to 1: The DIDX[2:0] will be fixed at 000. Then data on the CPA, CAPB, and AMP bits all set to 0 and the DSCG bit set to 1 will be transferred (i.e., when the power supply circuit stops, the electricity of the output voltage of the power supply circuit will be discharged).
In the above case, the step-up clock DDCK will automatically stop.

XDON set to 1: The DIDX[2:0] will be fixed at 000. Then data on the CPA, CPB, and AMP bits all set to 0 will be transferred. Transfer data on the DSCG bit depends on the setting in the DSCG bit. Simultaneously, the XDON pin will be active (set high), the gate will be all ON, and the electricity of the LCD panel will be discharged instantly.
In the above case, the voltage step-up clock DDCK will automatically stop.

Notes:

(1) Command transfer will not be executed by just setting the above bits (SLP, DSCG, and XDON). Command transfer will be executed with the DTRN set to 1 as well.

(2) The setting of each of the above bits will not refresh any bit of the power control register. Only the register value on the gate driver side will be refreshed.

(3) After the power supply circuit is stopped by using the above setting, to start the power supply circuit again, set the value in the power control register as required and execute command transfer to start power supply circuit.
At that time, when DTRN is set to 1, set 0 to the above bits and execute command transfer.

Resetting Gate Driver/Power Supply IC (MN863480)

By transferring data on D12 and D11 set to 1 and D10 set to 0 with the DIDX[2:0] set to 111, the gate driver/power supply IC (M863480) will be reset and the resisters will be initialized.
D15 to D11 will be all set to 1 (i.e., D [15:11] will be set to 11111) to rest. The reset state will be canceled by setting 0 to D10.

7.1.7 Other Commands (Test and Other Registers)

Address	Function	RW	Data		Description			Default
80h	Read address register	RW	D[7:0]	RADR[7:0]	Used to set the address of the desired register to be read.			00h
*** The following addresses : 81h～84h 、90h～94h are used for IC tests.**								
81h	Oscillation circuit test 1	RW						00h
82h	Oscillation circuit test 2	RW						3Fh
83h	Operational amplifier test	RW						03h
84h	RAM test	RW						05h
85h	Arbitration mode	-	D[7:4]	Blank bit (vacant bit)				
		RW	D[3]	ARB_LD	Indicate previous line data when conflict happen.	0	Ignore conflict	0
						1	Refer to description	
		RW	D[2]	ARB_AUTO	Indicate arbitration by delay circuit when conflict happen. This mode can access to limited frequency.	0	Ignore conflict	1
						1	Refer to description	
		RW	D[1]	ARB_OEV	Indicate previous frame data when conflict happen.	0	Ignore conflict	0
						1	Refer to description	
		RW	D[0]	ARB_RTRY	Extend H cycle when conflict happen and re-driving after the conflict.	0	Ignore conflict	0
						1	Refer to description	
90h	Internal counter test 1	R						-
91h	Internal counter test 2	R						-
92h	Internal counter test 3	R						-
93h	Internal counter test 4	R						-
94h	Internal counter test 5	R						-
F0h	Device ID read	R	Able to read device ID					31h
F1h	Deveice REV read	R	Able to read device REV					00h

8. Commands

8.1 Memory Control Commands

8.1.1 Memory Operation Mode Specifications (00h)

Address	RW	Data							
00h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		ADIR	XDIR	YDIR	BODR	AEMODE	Unused	Unused	Unused
Initial value		0	0	0	0	0	–	–	–

- ADIR[D7]: Specifies Address Increment Direction
  This bit is used to specify the direction of address increment at the time of writing data to the GRAM.
  With this bit set to 0, addresses will be counted in the X direction (i.e., the scan direction of the source driver).
  With this bit set to 1, addresses will be counted in the Y direction (i.e., the scan direction of the gate driver).

- XDIR[D6]: Specifies the Method of Address Count in the X Direction
  This bit is used to specify the method of address count in the X direction at the time of writing data to the GRAM.
  With this bit set to 0, addresses will increase in the X direction.
  With this bit set to 1, addresses will decrease in the X direction.

- YDIR[D5]: Specifies the Method of Address Count in the Y Direction
  This bit is used to specify the method of address count in the Y direction at the time of writing data to the GRAM.
  With this bit set to 0, addresses will increase in the Y direction.
  With this bit set to 1, addresses will decrease in the Y direction.

  The above ADIR, XDIR, and YDIR bits specified are valid for GRAM write access.
  These bits have no influence on any data written to the GRAM.

  See Section 6.2.3 for details.

- BODR[D4]: Specifies GRAM Write Data Format in 16-bit, 260000-color Mode
  This bit is used to specify the reception of image data when the 18-bit data from the host is received through the 16-bit bus.
  With this bit set to 0, the data will be aligned to the right.
  It will be possible to specify the reception of image data in 16-bit, two-time transfer aligned to the right.
  With this bit set to 1, the data will be aligned to the left.
  It will be possible to specify the reception of image data in 16-bit, two-time transfer aligned to the left.

  See Section 6.1.5 for information on the CPU interface in 16-bit mode.

- AEMOD[D3]: Specifies Access Range End-point Specification Mode
  This bit is used to specify how to set address XAE data and address YAE data that specify the access range.
  With this bit set to 0, the GRAM access range will be specified by the start and end addresses.
  The start address is specified by the XAS and YAS, and the end address is specified by XAE and YAE based on the start point.
  With this bit set to 1, the access width will be specified.
  Set the address values XAE and YAE to access width – 1 to specify the access width in X direction and that in the Y direction. If 0 is set, a single dot will be overwritten.

  By using this function, when GRAM data in a certain width needs to be overwritten continuously, for example, the GRAM data can be overwritten by just specifying the start address. This will reduce the number of address specifying times.

  See Section 6.2.4.

- **SDIR [D2]** : Assign shift direction of source driver
  Bit which assign driver output pin support **GRAM X** direction address "**00**" to "**175**".

  SDIR is set to 0 : Normal ; When X address set "**00**" to "**175**", driver output is "**00**" to "**175**".
  SDIR is set to 1 : Reverse ; When X address set "**00**" to "**175**", driver output is "**175**" to "**00**".

  See Section 6.2.3.

8.1.2 Memory Control Command (01h)

Address	RW	Data							
01h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		WM	WMMODE	Unused	Unused	RAMCLR	CLR_COL [2:0]		
Initial value		0	0	—	—	0	1	1	1

- WM[D7]: Window Mask Function Enabled

  This bit is used to enable or disable the window function.

  This mask processing is valid for the whole bits of image data.

  Specify a bit mask when masking each bit of image data.

  With the bit set to 0, the window mask function will be disabled.

  With the bit set to 1, the window mask function will be enabled.

  Data to be written to the GRAM will be masked if the data is in the range specified by the window mask range registers (WMXS, WMYS, WMXE, and WMYE).

  See Section 6.2.5.

- WMMODE[D6]: Specifies Window Mask Mode

  This bit is used to switch the valid window mask range.

  With the bit set to 0, the IC will be in inside-window mask mode.

  Data to be written to the GRAM will be masked if the data is inside the range specified by the window mask range registers (WMXS, WMYS, WMXE, and WMYE) including the borderline.

  With the bit set to 1, the IC will be in outside-window mask mode.

  Data to be written to the GRAM will be masked if the data is outside the range specified by the window mask range registers (WMXS, WMYS, WMXE, and WMYE) including the borderline.

  See Section 6.2.5 for information on the window mask function.

- RAMCLR[D3]: Specified GRAM Clear

  This bit is used to specify GRAM clear.

  With the bit set to 0, the IC will be in normal mode.

  In this case, the GRAM will not be cleared.

  With the bit set to 1, the GRAM will be cleared.

  The bit specified by the CLR_COL[2:0] will clear the GRAM. When the GRAM is cleared, the bit will be cleared as well automatically and set to 0. While the GRAM is being cleared, the data in the GRAM will not be guaranteed if the host gains access to the GRAM. If the RAMCLR is set to 0 while the GRAM is being cleared, the GRAM clear operation will be interrupted. At that time, the contents of the display will not be guaranteed. The GRAM clear function is used together with the GRAM access area, window mask, and bit mask specification. The masked area will not be GRAM cleared.

  See Section 6.2.6.

- CLR_COL[D2:D0]: Specifies GRAM Clear Color

  This bit is used to specify which bit is used to clear the GRAM.

  D[2]: Corresponds to R data.

  When the bit is set to 0, R is OFF. When the bit is set to 1, R is ON.

  D[1]: Corresponds to G data.

  When the bit is set to 0, G is OFF. When the bit is set to 1, G is ON.

  D[0]: Corresponds to B data.

  When the bit is set to 0, B is OFF. When the bit is set to 1, B is ON.

  [D2:D0] in combination: The GRAM clear function can be executed with white, black, R, G, B, yellow, magenta, or cyan.

8.1.3 Memory Access Range

Address	RW	Data							
02h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		XAS [7:0]							
Initial value		0	0	0	0	0	0	0	0
03h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		YAS [7:0]							
Init t		0	0	0	0	0	0	0	0
04h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		XAE [7:0]							
Initial value		1	1	1	1	1	1	1	0
05h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		YAE [7:0]							
Initial value		1	1	1	1	1	1	1	0

- Memory Access Range X Start Point Specification Command (02h)
  XAS[D7:D0]
- Memory Access Range Y Start Point Specification Command (03h)
  YAS[D7:D0]
- Memory Access Range X End Point Specification Command (04h)
  XAE[D7:D0]
- Memory Access Range Y End Point Specification Command (05h)
  YAE[D7:D0]

These bits are used to specify the write/read range in the GRAM from the host by the XAS, YAS, XAE, and YAE. Do not specify the range outside the effective display range, otherwise the displayed contents on the LCD will not be guaranteed. Be sure to specify the range inside the effective display range.

<AEMODE Set to 0>
The rectangular range of access to the GRAM is designated by the coordinate points XAS and YAS together with XAE and YAE.
The following conditions must be satisfied.
XAS ≤ XAE ≤ Valid display value in X direction
YAS ≤ YAE ≤ Valid display value in Y direction

<AEMODE Set to 1>
The rectangular range of access to the GRAM is designated by the start address specified by the XAS and YAS and the access width specified by the XAE and YAE.
The following conditions must be satisfied.
XAS + XAE ≤ Valid display value in X direction
YAS + YAE ≤ Valid display value in Y direction

See Section 6.2.4.

8.1.4 Window Mask Range

Address	RW	Data							
06h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		WMXS [7:0]							
Initial value		1	1	1	1	1	1	1	1
07h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		WMYS [7:0]							
Initial value		1	1	1	1	1	1	1	1
08h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		WMXE [7:0]							
Initial value		1	1	1	1	1	1	1	1
09h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		WMYE [7:0]							
Initial value		1	1	1	1	1	1	1	1

- Window Mask X Start Point Specification Command (06h)
  WMXS[D7:D0]
- Window Mask Y Start Point Specification Command (07h)
  WMYS[D7:D0]
- Window Mask X End Point Specification Command (08h)
  WMXE[D7:D0]
- Window Mask Y End Point Specification Command (09h)
  WMYE[D7:D0]

Data to be written to the GRAM will be masked according to the rectangular mask range designated by the coordinate points WMXS and WMYS together with WMXE and WMYE.

- The mask specified range must be within the GRAM access range.
- The following conditions must be satisfied, otherwise the displayed contents on the LCD will not be guaranteed.
  $WMXS \leq WMXE$
  $WMYS \leq WMYE$

See Section 6.2.5 for information on the window mask function.

8.1.5 Bit Mask Function

Address	RW	Data							
0Ah	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	BMSKR [5:0]					
Initial value		—	—	0	0	0	0	0	0
0Bh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	BMSKG [5:0]					
Initial value		—	—	0	0	0	0	0	0
0Ch	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	BMSKB [5:0]					
Initial value		—	—	0	0	0	0	0	0

- Bit Mask Function 1 (0Ah)
  BMSKR[D5:D0]: Specifies bit masks for 6-bit R.
- Bit Mask Function 2 (0Bh)
  BMSKG[D5:D0]: Specifies bit masks for 6-bit G.
- Bit Mask Function 3 (0Ch)
  BMSKB[D5:D0]: Specifies bit masks for 6-bit B.

The mask control of each bit used for 18-bit data is possible independently at the time of GRAM access, provided that the data is within the GRAM access range.

Respective RGB bits are processed as explained below.

Set to 0: Not masked.
The GRAM will be refreshed.
Set to 1: Masked
The GRAM will be masked and no data will be overwritten.

The bit mask processing is OR-processed with masking by the WDMSK input pin or window masking.
The mask or window mask function to be executed through the WDMSK input pin is valid for all bits. In either one of the functions is executed, the bit mask function will not work on any bits.
The bit mask function is, however, valid for all the specified GRAM access area. Therefore, the bit mask function will work on bits in any part where the mask function through the WDMSK input pin or the window mask does not work in the specified GRAM access area.

See Section 6.2.5 for information on the bit mask function.

8.1.6 GRAM Interface Mode (0Dh)

Address	RW	Data							
0Dh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	Unused	RMWR	RGBIF	RMIF
Initial value		—	—	—	—	—	0	0	0

• **RGBSW [D3] :** Bit which assign writing data from Host and RGB alignment swap of source driver.
When swap assigned, data is swap at writing time to GRAM. So this command is reflected after GRAM is written.
When "0" is selected, "without swap" is assigned.
R,G,B which are written from Host corresponds to source driver output ;YR, YG, YB.

When "1" is selected, "with swap" is assigned.
R,G,B which are written from Host is swapped to source driver output ; YB, YG, YR.
When read active at swap assigned, it is swapped inversely and back into former writing data align. Then, it is read.
See Section 6.2.10 for information on the RGB swap function

• RMWR[D2]: Specifies GRAM Write Port
This bit is used to control interface mode selection for image write data to the GRAM.
With this bit set to 0, the IC will be in CPU interface input mode, thus allowing image data to be written to the GRAM from the I/O or serial port of the CPU interface.
Make the following settings to select the I/O or serial port of the CPU Interface.
HOSTYP[1:0] set to [0:*]: I/O port (Dxx pin) mode
HOSTYP[1:0] set to [1:*]: Serial port (SIDA pin) mode
With this bit set to 1, the IC will be in RGB interface mode, thus allowing image data to be written to the GRAM from the input port (RGBDxx pin) of the RGB interface.

See Section 6.1.1 for information on the CPU interface.

• RGBIF[D1]: Specifies bus width for RGB interface access
This bit is used to select the access width of image data from the host while in RGB interface mode.
The specifications of the RGB interface are determined in the combination with the RMIF bit.
With the bit set to 0, the IC will be in 18-bit, 260000-color, single-time access mode or 16-bit, 65000-color, single-time access mode.
With the bit set to 1, the IC will be in 8-bit, 65000-color, two-time access mode or 6-bit, 260000-color, three-time access mode.

See Section 6.1.1 for information on the RGB interface.

• RMIF[D0]: Specifies GRAM interface mode
This bit is used to select 260000 or 65000 colors for the number of colors in transfer data to the GRAM from the host. When the IC is in CPU interface mode, the number of colors in transfer data to the GRAM will be determined
by the setting in the IFMODE[1:0] pin. When the IC is in RGB interface mode, the number of colors in transfer data to the GRAM will be determined by the bit in combination with the RGBIF bit.
With the bit set to 0, the IC will be in 18-bit, 260000-color mode.
With the bit set to 1, the IC will be in 16-bit, 65000-color mode.
While in 65000-color mode, the gradation LSB generation function (*LSB[1:0]) will be enabled and dither processing will be performed to get quasi 260000 colors.
In 260000-color mode, the gradation LSB generation function will be ignored.

See Section 6.1.1 for information on the data bus width, interfacing with the GRAM and RGB.

See Section 6.2.8 for information on the gradation LSB function.

Binary display is valid only for R5, G5, and B5 GRAM data with no relationship to display color modes.

8.1.7 Memory Write (0Eh)

Address	RW	Data							
0Eh	W	D7	D6	D5	D4	D3	D2	D1	D0
		Display RAM write							

This register is used to write the display RAM data.

The register specifies GRAM write from the host in the CPU interface mode.
Added data will be written to GRAM.

See Section 6.1.6 for information on the GRAM write access.

8.1.8 Memory Read (0Fh)

Address	RW	Data							
0Fh	R	D7	D6	D5	D4	D3	D2	D1	D0
		Display RAM read							

This register is used to read the display RAM data.

The register initializes GRAM read operation to the host.
The added data will be the read data from GRAM.
Read operation through the RGB interface pin and serial interface pin is not possible.
Format of read data conforms to the bit configuration specifications like specifications of bus width.
The first read data is dummy read data. The valid data will be read at and after the second read command executed.

See Section 6.1.6 for information on the GRAM read access.
See Section 6.1.5 for the information on the data format for details of the data format used.

8.2 Display Control Command

8.2.1 Display Mode Control (10h)

Address	RW	Data							
10h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	Unused	Unused	DISP[1:0]	
Initial value		—	—	—	—	—	—	0	0

- DISP[D1:D0]: Specifies display mode
  This bit is used to control the display mode of the LCD.

D1	D0	Display mode
0	0	Display interruption: Stops control signals to the LCD driver block and LCD panel.
0	1	Whole screen white display: The whole screen of the LCD will be white (i.e., alternation is performed) regardless of GRAM data, partial display specification, or the GRAM access range. In this case, the LCD will always display white with DISPINV specification ignored.
1	0	Whole screen display: The whole screen will be displayed according to GRAM data.
0	0	Partial display: The designated range set by the MASK* will not be displayed. Any part other than the designated range will be displayed according to the GRAM data.

Precautions for Display Interruption

- NOEV* output from the gate driver block will be always set high and output from the gate driver will be at VOFF center voltage or VEE voltage.
- Output from the source driver block will be in Hi-Z output state with the NOEH set high.
- The output signal pin to the DC/DC block operates with valid register set value. If power supply is provided, there will be no power stoppage. The CKV*, POL*, and STV* signals are continuously output. The VCOMEN* output is fixed at low level.
- The NVSYNCO signal will be output continuously in internal or external sync mode specified.

All bit settings are reflected to the operation of the IC in V sync mode.

8.2.2 Display V Sync Mode Control (11h)

Address	RW	Data							
11h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		VSYMODE	Unused	Unused	Unused	Unused	Unused	Unused	Unused
Initial value		0	—	—	—	—	—	—	—

- VSYMODE[D7]: Specifies sync mode
  This bit is used to select the sync mode of the LCD in display operation.

With the bit set to 0, the IC will be in internal sync mode and in self-running operation.
With the bit set to 1, the IC will be in external sync mode and in synchronization with sync signal input through the NVSYNCI.

In external sync mode, the NVSYNCO will output the NVSYNCI sampled by the oscillation clock without any modification.

The bit must be set to 0 if the V sync signal is not provided from the external source.
If the V sync signal (NVSYNCI) is not provided while in external V sync mode, the vertical system counter will keep its status on hold and stop driving the LCD panel.
When setting this bit while the LCD is in display operation, the IC will stop driving the LCD panel temporarily for the reception of the V sync signal but not longer than a 1V period.
To set the IC operating in external sync mode to internal sync mode, this bit will reflect in synchronization with the V sync signal. Therefore, the bit must be set before the next V sync input is turned on. Stop the NVSYNCI after this bit is turned on and the V sync signal is input at least once.

See Section 6.3.5 for information on the control of synchronization with the host.

8.2.3 Display Data Reverse Control (12h)

Address	RW	Data							
12h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	Unused	Unused	Unused	DISPINV
Initial value		–	–	–	–	–	–	–	0

- DISPINV[D0]: Specifies the reversion of display data

This bit is used to select the reverse control of display data written to the GRAM.

With the bit set to 0, the IC will be in normal mode with data output without being reversed.

When the POL polarity is high, the source driver block will read reversed RGB data from the GRAM.

When the POL polarity is low, the data will be read as it is.

With the bit set to 1, the IC will be in reverse mode with reversed data output.

When the POL polarity is low, the source driver block will read reversed RGB data from the GRAM.

When the POL polarity is high, the data will be read as it is.

This bit is valid only for the stored data in the GRAM, and not valid for whole screen white or refresh white display. That is, at the time of partial display, the control of this bit enables the negative-to-positive reversion in the effective display part, but the white display in the non-display part will remain unchanged.

The source driver usually selects the LCD display of normally white.

When the source driver is in normally black mode, whole screen white display will change to whole screen black, while partial refresh white display will change to refresh black. The effective screen, however, enables negative-to-positive reversion, thus displaying correctly with proper settings.

The level of VCOM output will be low with the POL set low.

The level of VCOM output will be high with the POL set high.

Select VCOM output under these preconditions. The MN863480 abides by the preconditions.

8.2.4 Partial Scroll Display Control (13h)

Address	RW	Data							
13h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	Unused	Unused	Unused	SCRON
Initial value		–	–	–	–	–	–	–	0

- SCRON[D0]: Specifies partial scroll display

This bit is used to select partial scroll display.

With the bit set to 0, the IC will be in normal mode and no scroll is performed.

With the bit set to 1, the IC will be in partial scroll mode. Then the number of lines set in partial scroll setting 1 SCRN[7:0] will be scrolled.

If the number of SCRN lines is increased gradually per frame, the partial scroll area will look scrolled.

When this bit is cleared, the display will return to normal regardless of SCRN, SCRS, or SCRE settings. Bit settings will be reflected on the operation of the IC in synchronization with the V sync signal.

See Section 6.3.3 for the definitions of the validity, execution, and detailed operation of partial scrolling.

8.2.5 Gradation LSB Control (14h)

Address	RW	Data							
14h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	RLSB [1:0]		BLSB [1:0]	
Initial value		—	—	—	—	0	0	0	0

- RLSB[D3:D2]: Specifies R's LSB control
  This bit is used to select the function of dither processing the R's LSB (R0) data while in 65000-color mode. The bit will be enabled with the RMIF bit set to 1 (while in 65000-color mode). The bit will be ignored when the RMIF bit is set to 0 (while in 260000-color mode).

  D3 D2
  0 0 : The R0 value stored in the GRAM will be read as it is.
  0 1 : The stored R0 data in the GRAM will be non-reversed and reversed by turns.
  1 0 : The stored R0 data in the GRAM will be reversed and non-reversed by turns.
  1 1 : R0 data based on R5 data is non-reversed and reversed or reversed and non-reversed frame by frame.

- BLSB[D1:D0]: Specifies B's LSB control
  This bit is used to select the function of dither processing the B's LSB (B0) data while in 65000-color mode. The bit will be enabled with the RMIF bit set to 1 (while in 65000-color mode). The bit will be ignored when the RMIF bit is set to 0 (while in 260000-color mode).

  D1 D0
  0 0 : The B0 value stored in the GRAM will be read as it is.
  0 1 : The stored B0 data in the GRAM will be non-reversed and reversed by turns.
  1 0 : The stored B0 data in the GRAM will be reversed and non-reversed by turns.
  1 1 : The stored B0 data in the GRAM will be non-reversed and reversed or reversed and non-reversed frame by frame.

See Section 6.2.8.

8.2.6 Specification of Display Start Line Address (15h)

Address	RW	Data							
15h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		LAS [7:0]							
Initial value		0	0	0	0	0	0	0	0

- LAS[D7:D0]: Specifies display start line address
  This bit is used to specify in which line on the LCD the 0th-line display data of the GRAM should be displayed. The count increases from the specified register value. When the count reaches the register value (GSL) of the number of specified lines in the Y direction, the display line of the LCD will be looped back to 0.

  The following condition must be satisfied.
  $0 \leq$ LAS line position $<$ Number of GSL lines

See Section 6.2.7.

8.2.7 Partial Scroll Specification

Address	RW	Data							
16h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		SCRN [7:0]							
Initial value		0	0	0	0	0	0	0	0
17h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		SCRS [7:0]							
Initial value		1	1	1	1	1	1	1	1
18h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		SCRE [7:0]							
Initial value		1	1	1	1	1	1	1	1

- Partial Scroll Setting 1 (16h)
  SCRN[D7:D0]: Specifies number of scroll lines
- Partial Scroll Setting 1 (17h)
  SCRS[D7:D0]: Specifies line of scroll start position
- Partial Scroll Setting 1 (18h)
  SCRE[D7:D0]: Specifies line of scroll end position

The SCRN bit is used to specify the number of lines to be scrolled, the SCRS bit is used to specify the base line i.e. start line, and the SCRE bit is used to specify the end line.

The GRAM is read from a base line position obtained by adding the number of lines specified by the SCRN to the display line position on the LCD specified by the SCRS. When the GRAM reading reaches to the end line specified by the SCRE, the display of the LCD will be looped back to the base line.
The LCD will be scrolled in synchronization with the V sync signal when the SCRON is set.

If the SCRN is specified at certain frame intervals with the number of SCRN lines increased constantly, the screen will be displayed or scrolled between the SCRS and SCRE positions.

The following conditions must be satisfied.
LSA < SCRS < SCRE
SCRN ≤ SCRE - SCRS < Number of GSL lines

See Section 6.3.3 for the definitions of the validity and execution of partial scrolling.

8.2.8 Specification of Partial Display

Address	RW	Data							
19h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		MASKS1 [7:0]							
Initial value		1	1	1	1	1	1	1	1
1Ah	RW	D7	D6	D5	D4	D3	D2	D1	D0
		MASKE1 [7:0]							
Initial value		1	1	1	1	1	1	1	1
1Bh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		MASKS2 [7:0]							
Initial value		1	1	1	1	1	1	1	1
1Ch	RW	D7	D6	D5	D4	D3	D2	D1	D0
		MASKE2 [7:0]							
Initial value		1	1	1	1	1	1	1	1
1Dh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		RFR [7:0]							
Initial value		0	0	0	0	1	1	1	0

- Partial Display Specification 1 (19h)
  MASKS1[D7:D0]: Non-display start position 1
- Partial Display Specification 2 (1Ah)
  MASKE1[D7:D0]: Non-display end position 1
- Partial Display Specification 3 (1Bh)
  MASKS2[D7:D0]: Non-display start position 2
- Partial Display Specification 4 (1Ch)
  MASKE2[D7:D0]: Non-display end position 2
- Partial Display Specification 5 (1Dh)
  RFR[D7:D0]: Specifies refresh cycle of partial display

1) The MASKS1, MASKE1, MASKS2, and MASKE2 bits are used to specify the start and end points of the non-display area on the LCD.
   Settings on these registers will be enabled in synchronization with the (internal or external) V sync signal, provided that the MASKE1 register has been set. Settings only in the other registers will not be reflected.
   After the other registers (i.e., MASKS1, MASKE1, MASKS2, and MASKE2) are set, make settings in the MASKE1 register

2) The RFR bits are used to set the refresh cycle of partial display.
   The refresh rate is set to 0 to FEh (254) + 1.
   The register set value must be always an even number.
   If odd numbers are used, the refresh portion will not be alternated.

   Example: If the set value is 0Eh, refresh white (alternated white display) will be written to the non-display lines in the partial display at 15-frame intervals. (0Eh + 1 = 15 frames)
   Like blanking periods, no data will be written to the LCD from the source or gate to the LCD during non-display periods, but the source and gate will operate according to the instructions of the OEHE and VCOME. Therefore, if even numbers are specified, the polarity of refresh white to be written will not be alternated between frames, which will result in the deterioration of image quality.

If partial display is selected in the display control bit DISP, the display will be performed in synchronization with the V sync signal. Then, the refresh white display of the effective display and non-display part will be reflected on the first frame. The effective display and non-display processing of data will be repeated from the second frame according to the specified number of frames and displayed at the RFR-specified refresh times.

FFh is a special value for LCD panel evaluation if it is set in the RFR bits.
In that case, the LCD will not be refreshed in the partial display mode.

See Section 6.3.2.

8.2.9 H Cycle Specification (1Eh)

Address	RW	Data							
1Eh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	HCNT [4:0]				
Initial value		–	–	–	0	1	0	1	1

- HCNT[D4:D0]: Specifies number of 1H clock pulses

This bit is used to specify the number of clock pulses for every 1H period.

HCNT bit: Set to the number of desired 1H clock pulses – 1

To set 11 clock pulses (1/206.6 kHz × 11 = 53.2 μs) for the 1H period, specify the HCNT to 0Ah.

Eight to 24 clock pulses can be specified.

While in external sync mode, however, the display of the LCD will not be guaranteed unless the number of vertical lines specified by the HCNT is the same as or larger than the number of GSL-specified lines plus 8H.

Example: HCNT value while in external sync mode with GSL set to 240 lines at 60 Hz is determined as follows.

$$HCNT < (206.6\ kHz \times 0.9) / \{60\ Hz \times (GSL: 240H + 8H)\}$$
$$< 12.5$$

Therefore, the HCNT will be 13 clock pulses or less.

The above calculation does not take the fluctuation of clock pulses into consideration. For practical calculation, consider the fluctuation of clock pulses and temperature changes.

8.2.10 V Cycle Specification (1Fh)

Address	RW	Data							
1Fh	RW	D7	D6	D5	D4	D3	D2	D1	D0
		VCNT [9:2]							
Initial value		0	1	0	0	1	0	1	0

- VCNT[D7:D0]: Specifies number of H's for 1V periods

This bit is used to specify the length of blanking during vertical periods while the IC is self-running.

While in external sync mode, the set value will be ignored. Instead, the V sync length will be specified by the external sync cycle. This counter is a 10-bit counter with the upper eight bits set.

1V=(VCNT+1H)×4

Specify between 00h and FFh with a variable range between 4H and 1024H.

The display of the LCD will not be guaranteed unless the number of lines specified is the same as or larger than the number of GSL-specified lines plus 8H.

VCNT values specified while in self-running mode

GSL specification	VCNT specification	V cycle
160 lines	29h min.	168H min.
176 lines	2Dh min.	184H min.
192 lines	31h min.	200H min.
220 lines	38h min.	228H min.
240 lines	3Dh min.	248H min.

8.3 LCD Driver Control Command

8.3.1 Driver Operation Setting 1 (20h)

Address	RW	Data							
20h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		GSL [2:0]			GDIR	GSCN	GCHS [1:0]		Unused
Initial value		1	1	0	0	0	0	0	1

- GSL[D7:D5]: Sets number of output pins of gate driver

These bits are used to set the number of output pins of the gate driver according to the GSL bit setting.

Set 1 to the [D7] of GSL[2] of the MN838893.

MN8388893				MN838892			
D7	D6	D5		D7	D6	D5	
1	0	x	192 outputs	0	0	x	160 outputs
1	1	0	220 outputs	0	1	x	176 outputs
1	1	1	240 outputs				

- GDIR[D4]: Shift direction of gate driver

This bit is used to specify the scan direction of the gate driver of the MN863480 according to the GDIR bit setting.

With the bit set to 0, the shift direction in the normal scan direction of the gate driver will be specified.

The gate driver will shift in the direction of Channel 240 from Channel 1.

With the bit set to 1, the shift direction in the reverse scan direction of the gate driver will be specified.

The gate driver will shift in the direction of Channel 1 from Channel 240.

- GSCN[D3]: Specifies scan mode of gate driver

This bit is used to specify the scan method of the gate driver.

With the bit set to 0, the single-side of panel connection mode will be specified.

With the bit set to 1, the both-side of panel connection mode will be specified.

- GCHS[D2:D1]: Specifies output channel position of gate driver

These bits are used to specify the output channel position of the gate driver.

These bits are enabled only when the GSCN is set to 0. When the GSCN is set to 1, set these bits to 00.

The output pin of the gate varies with the GSL bit setting.

For details, see the output position settings for the gate driver.

D2	D1	
0	0	Center output disabled
0	1	X240-side output disabled
1	0	X1-side output disabled
1	1	Setting prohibited (Disabled pins output VEE or VOFF according to the setting.)

8.3.2 Driver Operation Setting 2 (21h)

Address	RW	Data							
21h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		FRPOL	SAMP [2:0]			AMPSWON	AMPON	COL	RSWON
Initial value		0	0	1	1	0	0	1	1

- FRPOL[D7]: Specifies alternation drive mode

  This bit is used to set the LCD drive method to frame reversion or 1H/1F reversion.

  With the bit set to 0, the drive method will be set to 1H/1F reversion alternation drive.

  With the bit set to 1, the drive method will be set to frame reversion alternation drive. Alternation driving at 1H intervals will not be performed.

  1H/1F Reverse Alternation Drive Operation
  - The POL* signal is a signal output that alternates at 1H/1F intervals based on the POL polarity.
  - The VCOMEN* signal operates according to the VCOMON and VCOME bit settings.

  Frame Reversion Alternation Drive Operation
  - The POL* signal is a signal output that alternates based on the POL polarity with a single frame reversed.
  - The VCOMEN* signal operates according to the VCOMON and VCOME bit settings.

- SAMP[D6:D4]: Sets drive capability of operation amplifier of source driver

  These bits are used to specify the capability of the operation amplifier of the source driver.

  D6 : D5 : D4 = "000" : Stops operational amplifier
  "001" : Capability <Low>
  "010" : ↑
  ' ' ' '
  "100" : ↓ Standard setting is 011.
  "101" : Capability <High> Settings of 110 and 111 are prohibited.

  Select the best level according to the load of the LCD.

- AMPSWON[D3]: Drive timing control of source driver during gradation drive

  The drive timing of the LCD panel is controlled by the output amplifier circuit of the source driver when starting display in gradation drive control.

  With the bit set to 0, the LCD will be driven 1H before the LCD starts displaying.

  With the bit set to 1, the LCD will be driven 4H before the LCD starts displaying.

  The output of the source driver is in Hi-Z state before the source driver comes into drive operation.

- AMPON[D2]: Amplifier control of source driver

  This bit is used to stop the output amplifier circuit of the source driver while the NOEH signal is at high level or let the amplifier operate continuously regardless of the NOEH signal.

  With the bit set to 0, the amplifier circuit of the source driver will stop according to the NOEH signal.

  The output of the source driver will be in Hi-Z state at that time.

  With the bit set to 1, the amplifier circuit of the source driver will not stop regardless of the NOEH signal. The amplifier circuit will operate continuously.

  While the NOEH is at high level, however, only the output of the source driver will be in Hi-Z state.

- COL[D1]: Specifies gradation of the source driver

  This bit is used to set the output of the source driver to multi-valued gradation drive output or binary drive output.

  With the bit set to 0, the binary drive control of the source driver will be performed.

  At that time, the image data of only the uppermost GRAM bits (R5, G5, and B5) will be set to ON (1) and OFF (0).

  At that time, the D/A converter and amplifier circuit of the source driver will be stopped.

  With the bit set to 1, the multi-valued gradation drive control of the source driver with all GRAM bits used will be performed for 6-bit RGB gradation display.

- RSWON[D0]: Specifies connection of VREF resistor of source driver

  This bit is used to control the connection of the source driver to the VREF resistor during blanking periods while in gradation drive operation. This bit will be ignored while in binary display mode with the COL bit set to 0.

  With the bit set to 0, the connection of the source driver to the VREF resistor will be cut off during blanking periods with the NOEH signal set high.

  With the bit set to 1, the connection of the source driver to the VREF resistor will be turned on while in gradation display mode.

8.3.3 NOEV Control Settings

Address	RW	Data							
22h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	OEVA [4:0]				
Initial value		—	—	—	0	0	0	0	0
23h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	OEVN [4:0]				
Initial value		—	—	—	0	0	0	0	0

- NOEV Assertion Timing Setting (22h)

OEVA[D4:D0]: Specifies NOEV assertion timing

- NOEV negation timing setting (23h)

OEVN[D4:D0]: Specifies NOEV negation timing

These bits are used to set the control signal timing in the ON periods of the gate driver.

The timing is set by the number of internal oscillation clock pulses. If the number of clock pulses is not set within the number of clock pulses corresponding to a 1H period, no assertion or negation will be possible.

OEVA > OEVN: Waveform will be reversed.

OEVA = OEVN: Priority will be given to negation, and NOEV* will be high-level output.

OEVN ≥ HCNT bit value + 1: Negation will not be possible. The NOEV* will be low-level output.

OEVA ≥ HCNT bit value + 1: Assertion will not be possible. The NOEV* will be high-level output.

Both OEVA and OEVN ≥ HCNT bit value + 1: Assertion or negation will not be possible. The NOEV* will keep the previous status on hold.

During the blanking periods, however, high-level output will be turned on regardless of the OEV* setting for the non-display periods of partial display (except for refresh white display periods).

8.3.4 NOEH Control Settings

Address	RW	Data							
24h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	OEHA [4:0]				
Initial value		—	—	—	0	0	0	0	0
25h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	OEHN [4:0]				
Initial value		—	—	—	0	0	0	0	0

- NOEH Assertion Timing Setting (24h)

OEHA[D4:D0]: Specifies NOEH assertion timing

- NOEH negation timing setting (25h)

OEHN[D4:D0]: Specifies NOEH negation timing

These bits are used to set the control signal timing in the ON periods of the source driver.

The timing is set by the number of internal oscillation clock pulses.

If the number of clock pulses is not set within the number of clock pulses corresponding to a 1H period, no assertion or negation will be possible.

OEHA > OEHN: Waveform will be reversed.

OEHA = OEHN: Priority will be given to negation, and NOEH* will be high-level output.

OEHN ≥ HCNT bit value + 1: Negation will not be possible. The NOEH* will be low-level output.

OEHA ≥ HCNT bit value + 1: Assertion will not be possible. The NOEH* will be high-level output.

Both OEHA and OEHN ≥ HCNT bit value + 1: Assertion or negation will not be possible. The NOEH* will keep the previous status on hold.

During the blanking periods, however, NOEH control will be processed according to the OEHON/OEHE bit settings regardless of the OEH* setting for the non-display periods of partial display (except for refresh white display periods). During the extension period by the OEHE bit setting, NOEH control will be performed according to the above OEHA/OEHN settings. In other periods, high-level output will be obtained.

8.3.5 Source Driver Drive Expansion Settings (26h)

Address	RW	Data							
26h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		BLKSD	OEHON	OEHE [5:0]					
Initial value		1	0	0	0	0	0	1	0

- BLKSD[D7]: Drive data setting while in continuous source drive operation during V blanking periods (including non-display periods of partial display)

  With the bit set to 0, the source driver will output drive data at VREFH level.

  With the bit set to 1, the source driver will output drive data at VREFL level.

- OEHON[D6]: Specifies source driver driving during V blanking periods (including non-display periods of partial display)

  This bit is used to specify source driver driving during V blanking periods (including non-display periods of partial display).

  With the bit set to 0, during the transition from the effective display area to the V blanking period and to the non-display period, expansion processing is performed to drive the LCD according to the OEHE specification. After completion of expansion processing, the NOEH will be fixed at high-level output regardless of OEHA or OEHN bit settings.

  With the bit set to 1, output from the source driver will be always turned on. The NOEH will be output according to OEH* bit setting regardless of V blanking period setting or non-display area setting in partial display mode.

- OEHE[5:0]: Specifies number of continuous lines of source driving during V blanking periods

  This bit is used to specify the number of continuous lines of source driving during the V blanking period (including the non-display period in partial display mode).

  The extension of the drive period of source driver will be set between 0 and 63 lines after writing data in the last display line in whole screen display mode (or the refresh display period in partial display mode) or after writing data in the last display line in each display area when shifting from the display area to the non-display area in partial display mode.
  This specification will be ignored when the OEHON bit is turned on.

  A single line is a 1H period specified by the number of CKV* clock pulses.

  If drive extension by the OEHE, the display start point of the next frame, and the start of display from the state of non-display in partial display mode overlap due to V cycle condition, extension processing will be interrupted and image display will take precedence.

  In the above explanation, non-display in partial display mode refers to any period of non-display or display interruption. There is no difference in IC control between the refresh operation and whole screen display operation of the IC.

8.3.6 VCOM Drive Expansion Settings (27h)

Address	RW	Data							
27h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	VCOMON	VCOME [5:0]					
Initial value		—	0	0	0	0	0	0	1

- VCOMON[D6]: Specifies VCOM drive method during V blanking

  This bit is used to select the VCOM center voltage output by specifying the VCOME for VCOM driving during the V blanking period or continuous VCOM driving with the VCOMEN* fixed at low-level output.

  With the bit set to 0, the VCOM will be driven according to the VCOME setting.

  With the bit set to 1, the VCOM will be driven continuously.

- VCOME[D5:D0]: Specifies number of continuous lines of VCOM driving during V blanking periods

  This bit is used to specify the number of continuous lines of VCOM driving during the V blanking period.

  The extension of the VCOM drive period after writing data in the last display line can be set between 0 and 63 lines. That is, the VCOMEN* cancel line position after the end display line is written can be specified.
  A single line is a 1H period specified by the number of CKV* clock pulses.

  If drive extension by the VCOME, the display start point of the next frame, and the start of display from the state of non-display in partial display mode overlap due to V cycle condition, extension processing will be interrupted and image display will take precedence.

8.4 Image Quality Adjustment Command

8.4.1 RGB Brightness Adjustments

Address	RW	Data							
28h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	RADJ [5:0]					
Initial value		—	—	0	0	0	0	0	0
29h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	GADJ [5:0]					
Initial value		—	—	0	0	0	0	0	0
2Ah	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	BADJ [5:0]					
Initial value		—	—	0	0	0	0	0	0

- R Adjustments (28h)
  RADJ[D5]: Specifies data addition and subtraction
  RADJ[D4:D0]: Specifies the quantity of data for R adjustments

- G Adjustments (29h)
  GADJ[D5]: Specifies data addition and subtraction
  GADJ[D4:D0]: Specifies the quantity of data for G adjustments

- B Adjustments (2Ah)
  BADJ[D5]: Specifies data addition and subtraction
  BADJ[D4:D0]: Specifies the quantity of data for B adjustments

This bit is used to perform addition and subtraction processing of R, G, and B independently when reading RGB display data stored in the GRAM. Therefore, the contents of the GRAM will keep saved write values. This bit enables white balance adjustments and brightness adjustments to the LCD.

The D5 bit is specified as follows:
With the bit set to 1, the bit value specified by [D4:D0] will be subtracted from GRAM data and displayed.
With the bit set to 0, the bit value specified by [D4:D0] will be added to GRAM data and displayed.

The result of addition or subtraction will be a maximum of 3Fh or a minimum of 00h regardless of whether the actual value is larger than 3Fh or smaller than 00h.

See Section 6.3.4.

8.4.2 RGB Gamma Adjustments

		D7	D6	D5	D4	D3	D2	D1	D0
31h	W	Unused	GMP1 [2:0]			Unused	GMN1 [2:0]		
Initial value		—	1	0	0	—	1	0	0
32h	W	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	GMP2 [2:0]			Unused	GMN2 [2:0]		
Initial value		—	1	0	0	—	1	0	0
. . . . .									
**h	W	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	GMPn [2:0] n=1 to 62			Unused	GMNn [2:0] n=1 to 62		
Initial value		—	1	0	0	—	1	0	0
. . . . .									
6Dh	W	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	GMP61 [2:0]			Unused	GMN61 [2:0]		
Initial value		—	1	0	0	—	1	0	0
6Eh	W	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	GMP62 [2:0]			Unused	GMN62 [2:0]		
Initial value		—	1	0	0	—	1	0	0

- Gamma Adjustments (31h to 6Eh)
  GMPn [D6:D4]: Gamma correction control while in positive polarity drive operation (with the POL set low).
  GMNn [D2:D0]: Gamma correction control while in negative polarity drive operation (with the POL set high).

  n: 1 to 62, corresponding to gamma adjustment address of 30h + n

  This bit is used to make gamma adjustments to the source driver.

  There are 63 gamma adjustments for the positive polarity and negative polarity use respectively, each of which is variable independently, which makes it possible to provide optimum gamma characteristics according to the display mode and characteristics of the LCD.
  The gamma center value varies with the configuration of the LCD and material of the LCD while each bit value is 04h. The gamma characteristics are designed so that they will be close to 2.0, provided that standard LCD materials and configuration are used.

  See Section 6.5.4.

Note) ① Above "n" shows number of gray scale potential between VREFH – VREFL.
Number of scale : "VREFH" = 0 (V_0), "n=1" = 1 (V_1), ••• "N=62" = 62 (V_{62}), "VREFL" = 0 (V_0)

② For the resister setting value and gray scale potential, "100" as a standard, when set the value to "+", the potential is adjusted "+" side, when set the value to "-", adjusted "–" side.

Based on the above ①②, to do γ adjustment, keeping the voltage which apply to Crystal Liquid at positive and negative potential, if n scale of positive potential adjust to +1 from "100", 63-n scale(negative potential) need to adjust to –1 from "100".

Example) Adjust GRAM data "03" gray scale :
Gray scale potential of positive electrode driving : 3rd scale (V_3),
Gray scale potential of negative electrode driving : 63-n = 60th scale (V_{60})
GMP3 ⇒"101", GMN60 ⇒"011"

※Only writing is available, and unable to read.

8.5 Commands for Power Supply System

8.5.1 Operation Mode Specification for Power Supply System (70h)

Address	RW	Data							
70h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		OSCON	DDCKON	DDCKF [1:0]		VGMG	DDC [2:0]		
Initial value		0	0	0	0	0	0	0	0

- OSCON[D7]: Output control of original oscillation clock pulses

  This bit is used to turn the original oscillation clock of the controller oscillation circuit on and off.
  With the bit set to 0, the clock will stop oscillating.
  With the bit set to 1, the clock will start oscillating.

  The bit will be set to 0 by default after the IC is reset or the software reset is issued, in that case, the original oscillation clock will be interrupted.
  It will take 3 ms for the stabilization of the clock after the bit is turned on.
  Do not set registers that use the original oscillation clock until the oscillation is stabilized.
  When the original oscillation clock starts oscillating, the CKV*, POL*, STV*, and NVSYNCO will be output continuously.
  The expected waveform value will not be, however, guaranteed within 3 ms.
  While the original oscillation clock is oscillating, the CKV*, POL*, STV, and NVSYNCO will not stop.
  The cycle of the NVSYNCO follows the VCNT and VSYMODE bit settings.

- DDCKON[D6]: Step-up voltage clock output control

  This bit is used to control DC/DC clock output.
  With the bit set to 0, the DC/DC clock output will stop while the DDCK* clock output pin will be fixed at low level.
  With the bit set to 1, DC/DC clock pulses will be output from the DDCK* pin according to the DDCKF bit setting.

- DDCKF[D5:D4]: Sets frequency dividing ratio of step-up voltage clock DDCK

  These bits are used to control the output frequency of the DC/DC clock.

D5	D4	
0	0	: 1H =206.6 kHz/(HCNT+1)=18.8 kHz (HCNT=0Ah)
0	1	: Original oscillation clock × 1/4 =206.6 kHz/4=51.7 kHz
1	0	: Original oscillation clock × 1/2=206.6 kHz/2=103.3 kHz
1	1	: Original oscillation clock × 1 =206.6 kHz/1=206.6 kHz

  With these bit both set to 0, the frequency varies according to the HCNT bit settings.
  No other set values will change because the frequency of original oscillation is directly divided.

- VCMG[D3]: Sets VCOM output and VOFF output of MN863480

  This bit is used to control the VCOM output and VOFF output of the MN863480.
  With the bit set to 0, the VCOM output and VOFF output are fixed at ground level regardless of POL* or VCOMEN* setting.
  With the bit set to 1, the outputs will be normal according to each control register setting.

  By setting this bit to 0 when the IC is turned on, unstable voltage will not be input into the LCD panel from the VCOM or VOFF line.

- DDC[D2:D0]: Sets usage of step-up voltage clock of MN863480

  These bits are used to adjust the capability of the voltage step-up circuit by setting the usage of the voltage step-up clock of the MN863480.

  Following frequency dividing modes are available by bit settings.

D2	D1	D0	
0	0	0	: DDCK's input is used as it is.
0	0	1	: Frequency dividing pattern 1
'	'	'	: ' ' ' ' ' ' '
1	1	0	: Frequency dividing pattern 6
1	1	1	: Frequency dividing pattern 7

  See the Specifications of the MN863480 for frequency dividing pattern settings in detail.

8.5.2 Command Transfer to MN863480 (71h)

Address	RW	Data							
71h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	DIDX[2:0]			XDON	DSCG	SLP	DTRN
Initial value		—	0	0	0	0	0	0	0

- DIDX[D6:D4]: Specifies command transfer to MN863480
  These bits are used to specify registers for command transfer to the MN863480.

  The following transfer is available by bit settings.

D6	D5	D4	
0	0	0	: Power control
0	0	1	: Voltage setting 1
0	1	0	: Voltage setting 2
0	1	1	: Voltage setting 3
1	0	0	: Display setting
1	0	1	: Test register
1	1	1	: Reset register

  When turning the IC on after resetting (hardware or software resetting), use the following sequence to ensure each register setting.
  Voltage setting 1 → Voltage setting 2 → Voltage setting 3 → Power control

  See Section 7.1.6 or the Specifications of the MN863480.

- XDON[D3]: All-ON control of gate driver
  This bit is used to set all the output pins (including the X0 and X241 pins) of the gate driver to VGG voltage or normal output.
  With the bit set to 0, normal output will be obtained.
  With the bit set to 1, all the gate pins will be turned on (fixed at VGG voltage).

  The level is higher than the OEV* and this control takes precedence over all gate driver operations.

- DSCG[D2]: Specifies power supply IC discharge
  This bit is used to discharge electricity from the power supply IC.
  With the bit set to 0, the IC will be in normal operation.
  With the bit set to 1, electricity will be discharged from the power supply IC.

  With the bit set to 1, DIDX[000] (all zeros) will be issued to stop the operation of the DDCK. Then the DC/DC side will start discharging the electricity in the voltage step-up capacitance.

- SLP[D1]: Sleep mode control
  This bit is used to set the IC to sleep mode.
  With the bit set to 0, the IC will be in normal operation.
  With the bit set to 1, the IC will be set to sleep mode.

  With the bit set to 1, DIDX[000] (all zeros) will be issued to stop the operation of the DDCK. Simultaneously, DSCG bit setting will be possible.

  While in sleep mode, the IC will operate as explained below.
  - The DC/DC, source, and gate output blocks will stop operating.
  - Unless software or hardware resetting is performed, registers set for the controller will be kept on hold.
  - The original oscillation clock will oscillates (with the POL*, CKV*, and STV* output.)

- DTRN[D0]: Serial transfer control to the MN863480
  This bit is used for the serial transfer of control commands to the MN863480.
  With the bit set to 0, the IC will stand by.
  With the bit set to 1, the transfer of control commands will start.

  With the DTRN bit set to 1 and control commands are issued, serial transfer of the commands to the MN863480 will be performed. Approx. 110 μs after completion of serial transfer of the commands, the bit will be automatically cleared and set to 0.

8.5.3 Power Control of MN863480 (72h)

(Run/Stop Control and Multiplication and Capability Adjustments of Voltage Step-up Circuit and Operational Amplifier)

Address	RW	Data							
72h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		CPA [1:0]		CPB [1:0]		AMP [3:0]			
Initial value		0	0	0	0	0	0	0	0

- CPA[D7:D6]: Sets voltage step-up circuit 1
  These bits are used to make settings for voltage step-up circuit 1.

D7	D6	
0	0	: Voltage step-up circuit is not in operation.
0	1	: Voltage step-up circuit is not in operation.
1	0	: See Specifications of MN863480.
1	1	: See Specifications of MN863480.

- CPB[D5:D4]: Sets voltage step-up circuits 3 and 4
  These bits are used to make settings for voltage step-up circuits 3 and 4.

D5	D4	
0	0	: Voltage step-up circuit is not in operation.
0	1	: Voltage step-up circuit is not in operation.
1	0	: See Specifications of MN863480.
1	1	: See Specifications of MN863480.

- AMP[D3:D0]: Capability adjustments to operational amplifier of power supply IC.
  These bits are used to stop or make capability adjustments to the operational amplifier of the power supply IC.

D3	D2	D1	D0	
0	0	0	0	: Operational amplifier is not in operation.
0	0	0	1	: See Specifications of MN863480.
'	'	'	'	: '''''
'	'	'	'	: '''''
1	1	0	1	: Setting prohibited.
1	1	1	0	: Setting prohibited.
1	1	1	0	: Setting prohibited.

See the Specifications of the MN863480 for the details of the above register settings.

8.5.4 Power Supply Settings

Address	RW	Data							
73h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	AVD [3:0]			
Initial value		–	–	–	–	0	0	0	0
74h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	VRFH [4:0]				
Initial value		–	–	–	0	0	0	1	1
75h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	VCMH [5:0]					
Initial value		–	–	0	0	0	0	0	0
76h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	VCMPL [4:0]				
Initial value		–	–	–	0	0	0	0	1
77h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	VOFFL [4:0]				
Initial value		–	–	–	0	0	0	0	1
78h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	VOFPL [5:0]					
Initial value		–	–	0	0	0	0	0	1

- Power Supply Setting 1 (73h)
  AVD[D3:D0]: Sets AV_{DD} voltage
  These bits are used to set the AV_{DD} voltage between 3.5 V and 5.5 V.

  Pay utmost attention when making settings in order not to include prohibited bits in combination or prohibited setting areas.

- Power Supply Setting 2 (74h)
  VRFH[D4:D0]: Sets V_{REFH} voltage
  These bits are used to set the V_{REF} voltage between 3.0 V and 5.0 V (In AV_{DD} – 0.5 V).

  Pay utmost attention when making settings in order not to include prohibited bits or prohibited setting areas, in consideration of the AV_{DD} voltage. Do not make settings for 18h to 1Fh.

- Power Supply Setting 3 (75h)
  VCMH[D5:D0]: Sets VCOMH voltage
  These bits are used to set the VCOMH voltage between 1.0 V and 5.5 V (not more than the V_{REFH}) or enable an external volume.

  Pay utmost attention when making settings in order not to include prohibited bits. Do not make settings for 1h to 7h and 31h to 3Fh.
  The external volume will be set with the value set to 00h, when the settings in the built-in volume will be ignored.

- Power Supply Setting 4 (76h)
  VCMPL[D4:D0]: Sets VCOM amplitude
  These bits are used to set the VCOM amplitude between 2.0 V and 6.0 V.
  The following condition must be satisfied.
  $-(VCC \times 2 - 1)\ V \leq VCOML \leq 1\ V$

  Pay utmost attention when making settings in order not to include prohibited bits or prohibited setting areas, in consideration of the voltage set with the VCMH register. Do not make settings for 00h and 1Fh.

- Power Supply Setting 5 (77h)
  VOFFL[D4:D0]: Sets VOFFL voltage
  These bits are used to set the VOFFL voltage between VEE + 0.5 V and -4 V.

  Pay utmost attention when making settings in order not to include prohibited bits or prohibited setting areas, in consideration of the VEE voltage. Do not make settings for 00h and 1Bh to 1Fh.

- Power Supply Setting 6 (78h)
  VOFFPL[D5:D0]: Sets VOFF amplitude
  These bits are used to set the VOFF amplitude between 2.0 V and 9.0 V.
  The following condition must be satisfied.
  $VEE + 2\ V \leq VOFFH \leq -2\ V$

  Pay utmost attention when making settings in order not to include prohibited bits or prohibited setting areas, in consideration of the VEE voltage and VOFFL voltage. Do not make settings for 00h and 37h to 3Fh.

See the Specifications of the MN863480 for the details of power supply setting register.

8.5.5 Power Supply Circuit Capability Adjustment (79h)

Address	RW	Data							
79h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		CKVPW [3:0]				Unused	LPM [2:0]		
Initial value		0	1	0	0	—	0	0	0

- CKVPW[D7:D4]: Sets pulse width of CKV
  These bits are used to adjust the pulse width of the CKV* while the signal level is high.

  With the value set between 1h and Fh, the high-level width of the CKV will be within a range between 1 and 15 clock pulses. Usually set the value to 4h. Do not set the value to 0h or to HCNT+1 or over, otherwise the CKV* will be fixed at high level and the LCD will not display normally.

- LPM[D2:D0]: Adjusts capability of the VOFF and VCOM power supply circuit
  These bits are used to set the amplifier capability of the power supply circuit of the VOFF and VCOM.

  With settings of these bits, the amplifier capability of the VOFF and VCOM will vary according to the signal timing of the POL*, CKV*, and DDCK*.
  Therefore, the signal will not stop regardless of any display status.

  See the Specifications of the MN863480 for the details of capability settings for each signal.

8.6 Other Commands

8.6.1 Software Reset (7Ah)

Address	RW	Data							
7Ah	W	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Unused	Unused	Unused	Unused	SRESET
Initial value		—	—	—	—	—	—	—	0

- SRESET[D0]: Specifies software resetting
  The bit is used to initialize register values.
  The OSCON bit will not be, however, influenced.

  After software resetting, only the clock oscillation status to be automatically cleared and set to 0 will be executed.

8.6.2 Read Address Register (80h)

Address	RW	Data							
80h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		RADR [7:0]							
Initial value		0	0	0	0	0	0	0	0

- RADR[D7:D0]: Sets address of read register
  These bits are used to set the address of the read register when the REGMODE is set high.

  When the REGMODE is set high, set the address of the register to be read as data, write the command, and read the data at the next cycle. Then a set of the address and data value will be read.
  The address returned is treated as invalid, but the address of the desired data will be returned.

8.6.3 Conflict arbitration register (85h)

Address	RW	DATA							
85h	RW	D7	D6	D5	D4	D3	D2	D1	D0
		Blank				ARB_LD	ARB_AUTO	ARB_OEV	ARB_RTRY
Default		–	–	–	–	0	1	0	0

Host access to GRAM and display read to Liquid Crystal are independent action.
When movie data (ex. camera image) transfer, following actions are suggested to control preventing writing and display read conflict (access same line).

Control display read timing to Liquid Crystal by external V SYNC mode.
Control writing from Host side by V SYNC output of this LSI.

If Host writing and display read conflict, picture may be distorted.
In case of conflict, Display data shows whiteness and picture will be distorted.
If there is possibility of conflict, following setting can control the action.

・ARB_LD[D3] : a BIT which set previous line data display mode when the conflict occur.
0 : Normal mode. Not act specially.
1 : Previous line data driving mode.
When conflict occur, drive a Display data of previous line.
NOTE) Please set ARB_OEV = 0 ; refer to below chart.
In ARB_OEV = 1, the setting described on the left of the chart is given priority over ARB_LD and enable to reflect on display.

・ARB_AUTO[D2] : a BIT which display data after renewed writing when the conflict occur.
0 : Normal mode. Not act specially.
1 : Data Display mode after writing delay arbitration.
In LSI, automatically arbitrate, wait Host writing complete and indicate renewed data.
The mode is constraint on Host access cycle.
Please use over the following condition.

DV_{DD} supply voltage	Condition
2.7 V to 3.6 V	More than 210 ns (4.76 MHz and under)
from 2.5 V to less than 2.7 V	More than 250 ns (4.0 MHz and under)
from 2.35 V to less than 2.5 V	Prohibited

Note) Set ARB_OEV =0, ARB_RTRY =0 ; refer to below chart
In ARB_OEV = 1, the setting described on the left of the chart is given priority over ARB_AUTO and enable to reflect on display.
Renewed writing data drive in this mode. So re-driving does not need at ARB_RTRY = 1.

・ARB_OEV[D1] : a BIT which display previous frame data when the conflict occur.
0 : Normal mode. Not act specially
1 : Test mode. Don't use in this mode.
When conflict occur, this mode prohibit gate driver output and keep previous frame data on LCD.
NOTE) The mode is valid only set to OEVA =01h, 02h.
Please not to use except above setting.

・ARB_RTRY[D0] : a BIT set same line re-driving mode when the conflict occur.

0： Normal mode. Not act specially.

1： Re-driving at same line.

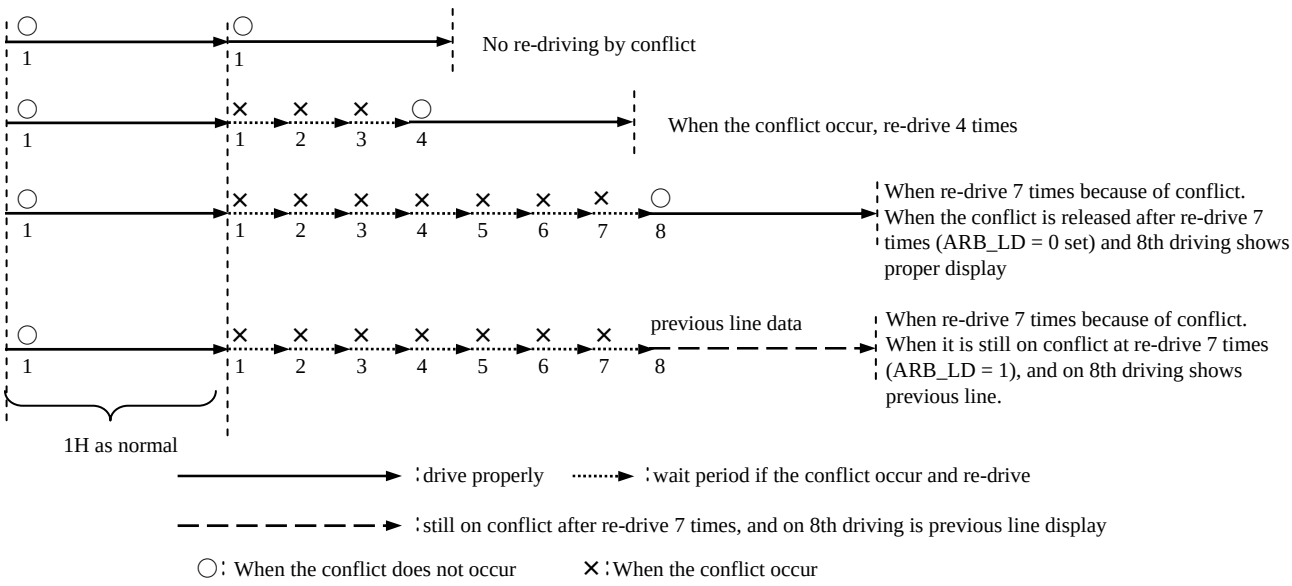
Extend H cycle at conflict. Re-drive same line after 40μs.
If conflict is released when driving re-start, driving continue properly.
If still on conflict, re-try till 7 times. If still on conflict until 7 times, drive properly at 8th times.
If conflict does not occur by 8 times, the data that have completed HOST-write is drived.
If conflict occur, conflict pixel at the 8th time become white data noise.
When the mode use together with ARB_LD = 1, previous line data surely drive at the 8th time and move to next line.

When the function is on use, please indicate LCD panel vertical pixel and GSL (20h) and VCNT (1Fh) as following table shows. In consideration of setting VCNT (1Fh) and frame frequency, set HCNT (1Eh), OEV*(22h,23h), and OEH*(24h,25h) with care.

Vertical pixel	GSL [1:0] (20h) set value	VCNT [9:2] (1Fh) set value
192	"10 x"	More than "38 h" (228 H)
220	"110"	More than "3Dh" (248 H)
240	ARB, RTRY mode prohibit	---

NOTE) It is highly recommended that this mode should use with ARB_LD = 1 when think about the conflict keeps

ARB_RTRY= "1" : operation at re-driving mode is as following figures. (combine with ARB_LD = 1)



【When use the re-drive mode (Combine with ARB_LD = 1】

① Re-driving mode is decided by host access speed when renewed data. Conflict should be solved by 7th driving. Following show the Host frequency.

Host access cycle on 1H line > { (waiting time on conflict x waiting for re-drive (6 times)) – margin (2 clock)} / horizontal writing pixel
= {(1/206.6 kHz x 110%) x (9CK x 6 times - 2CK)} ／176 = 1.30 μs
→ This only happen when Host speed is slower than 0.769 MHz

②Re-drive mode could cause for deterioration of image quality because the LCD frame frequency depend on re-drive time by conflict. Please make sure the result of evaluation on real panel.

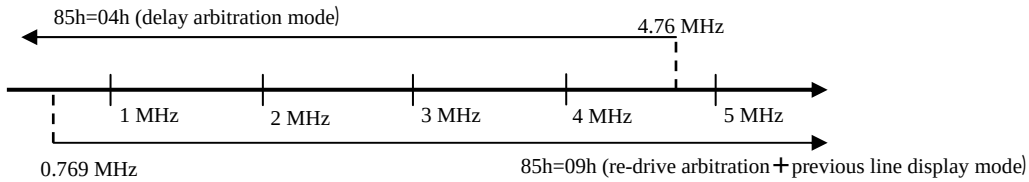
□NOTE In each case, the display should be evaluated sufficiently.

【Recommended setting values for conflict arbitration mode】

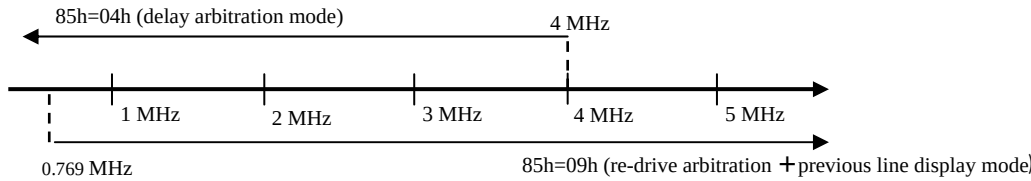
Recommended setting values for conflict arbitration mode depend on the Host access speed when conflict occur which is caused by async writing, are shown as follows. The display should be evaluated sufficiently.

□NOTE Host access speed : when GRAM access one time per a pixel.

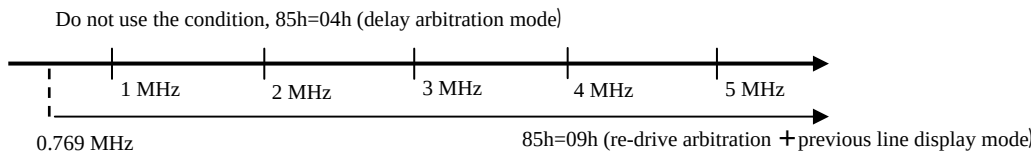
①DV_{DD} = 2.7 V to 3.6 V



②DV_{DD} = from 2.5 V to less than 2.7 V



③DV_{DD} = from 2.35 V to less than 2.5 V



□NOTE ① As a rule, this is recommended at delay arbitration mode
② Please use the re-drive arbitration mode with due caution as LCD frame frequency would be deterioration if conflict often occur
③Conflict often occur when writing mode to GRAM is set as vertical writing (ADIR = 1).
④Do not use the vertical writing mode when motion picture is transferred.

8.6.4 Device ID read resister mode(F0h / F1h)

This mode can read LSI device ID (set each variety) and device REV.
F0h is device ID. In the case of this LSI, 31h is read.
F1h is device REV. when REV=0, 00h is read.

Disable to writing in the resister.

Address	RW	Data							
F0h	R	D7	D6	D5	D4	D3	D2	D1	D0
Default		0	0	1	1	0	0	0	1
F1h	R	D7	D6	D5	D4	D3	D2	D1	D0
Default		0	0	0	0	0	0	0	1

8.7 Test Register

The following registers are for test use.
Do not use them, because the operation of these registers is not guaranteed. Take this as a serious precaution.

Address	RW	Data							
81h	RW	D7	D6	D5	D4	D3	D2	D1	D0
Initial value		0	0	0	0	0	0	0	0
82h	RW	D7	D6	D5	D4	D3	D2	D1	D0
Initial value		Unused	Unused	1	1	1	1	1	1
83h	RW	D7	D6	D5	D4	D3	D2	D1	D0
Initial value		Unused	Unused	Unused	Unused	0	0	1	1
84h	RW	D7	D6	D5	D4	D3	D2	D1	D0
Initial value		Unused	Unused	Unused	0	0	1	0	1
90h	R	D7	D6	D5	D4	D3	D2	D1	D0
		Read only							
91h	R	D7	D6	D5	D4	D3	D2	D1	D0
		Read only							
92h	R	D7	D6	D5	D4	D3	D2	D1	D0
		Unused	Unused	Unused	Read only				
93h	R	D7	D6	D5	D4	D3	D2	D1	D0
		Read only							
94h	R	D7	D6	D5	D4	D3	D2	D1	D0
		Read only							