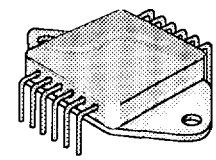
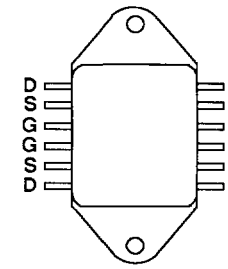
MOD500A/500B/500C

4 N-Channel Enhancement Mode Transistors

HERMETIC MODULE



TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	LEADFORM OPTION
MOD500A	500	0.43	13	Straight
MOD500B	500	0.43	13	Bent Down
MOD500C	500	0.43	13	Bent Up

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SINGLE DIE	ALL DIE	
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	13	41	A
	T_C = 100°C		8	26	
Pulsed Drain Current[1]		I_{DM}	52	164	
Avalanche Current (See Figure 9)		I_A	13	–	
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYP	MAXIMUM		UNITS
			SINGLE	ALL	
Junction-to-Case	R_{thJC}		0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}		30	30	
Case-to-Sink	R_{thCS}	0.1			

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		13		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7 A	0.33		0.43	Ω
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	0.66		0.88	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7 A	9.0	6.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700		3200	pF
Output Capacitance	C_{oss}		410		600	
Reverse Transfer Capacitance	C_{rss}		140		200	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A	75		120	nC
Gate-Source Charge[2]	Q_{gs}		12			
Gate-Drain Charge[2]	Q_{gd}		35			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 210 V, R_L = 30 Ω, $I_D \simeq$ 7 A, V_{GEN} = 10 V, R_G = 4.7 Ω	13		35	ns
Rise Time[2]	t_r		26		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		55		150	
Fall Time[2]	t_f		17		70	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				13	A
Pulsed Current[3]	I_{SM}				52	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	300			ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

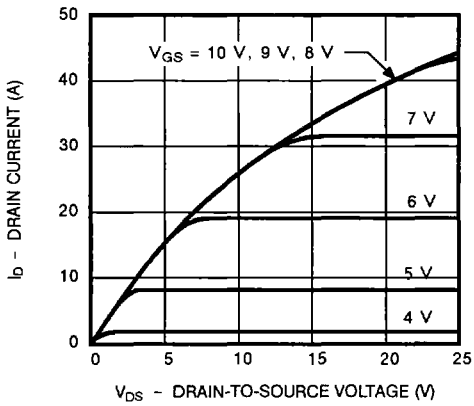


Figure 2. Transfer Characteristics

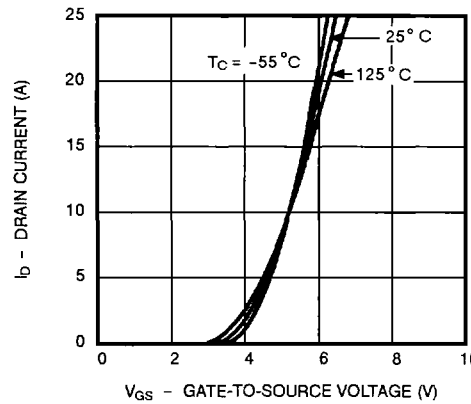


Figure 3. Transconductance

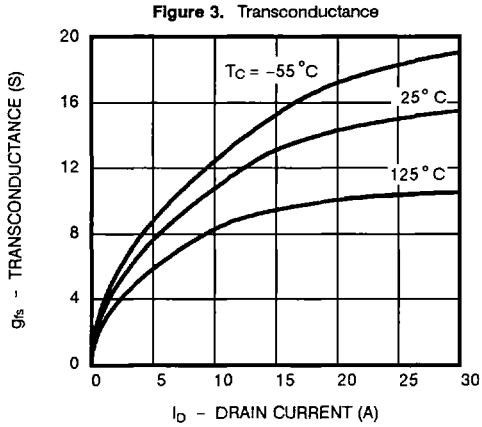


Figure 4. On-Resistance

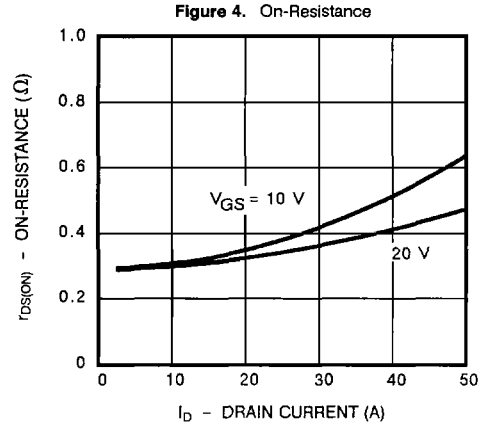


Figure 5. Capacitance

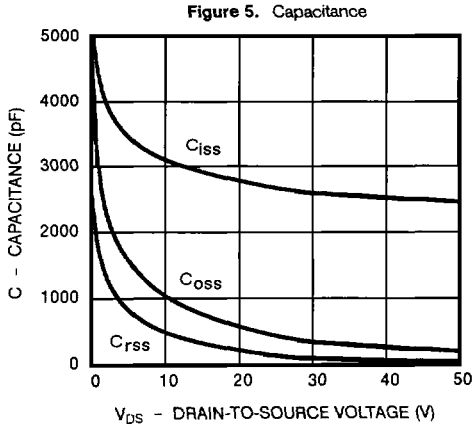
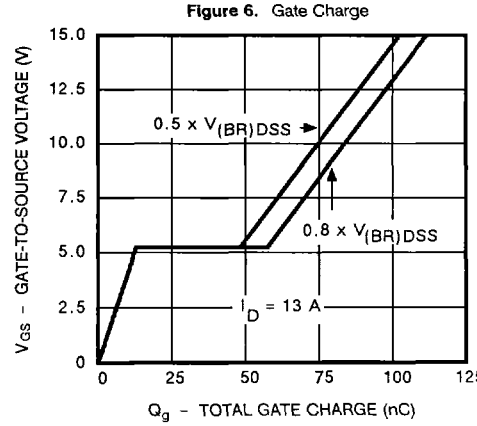


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

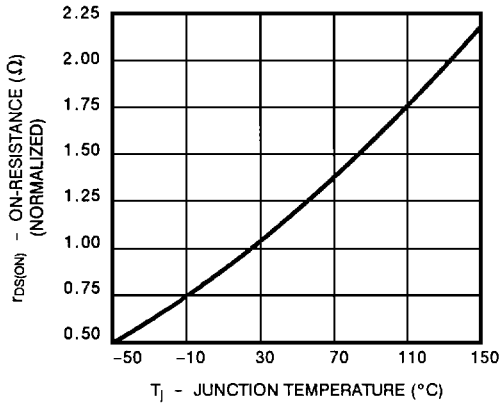
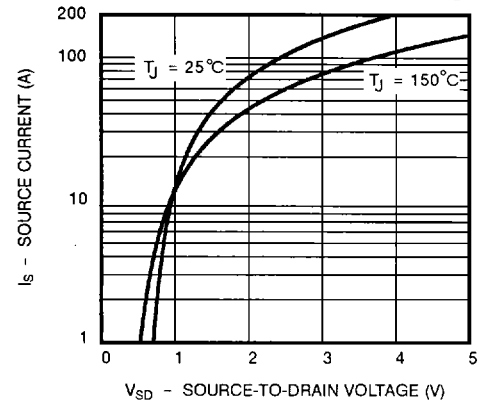


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

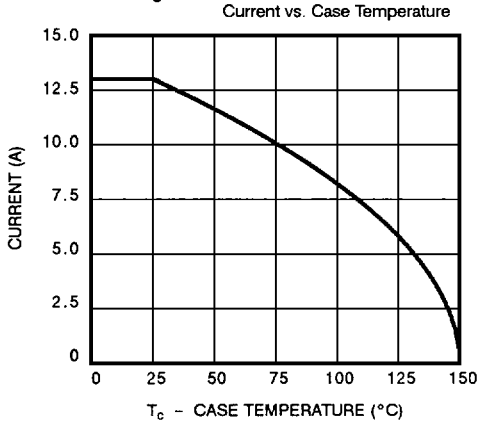
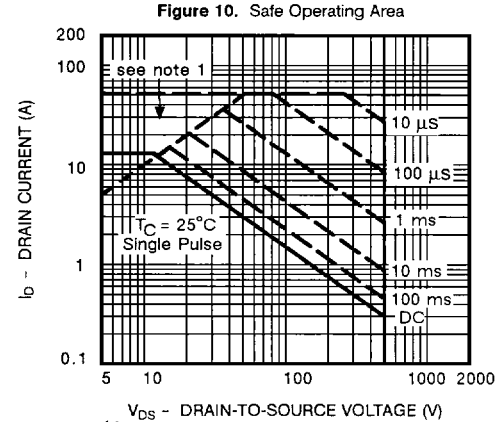


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case