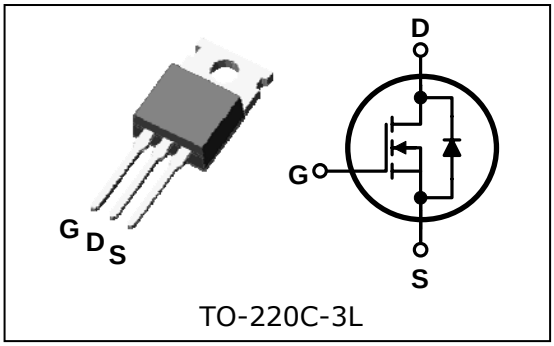
# MP12N60

**Power MOSFET**

SWITCHING REGULATOR APPLICATIONS

## PIN Connection




TO-220C-3L

## Features

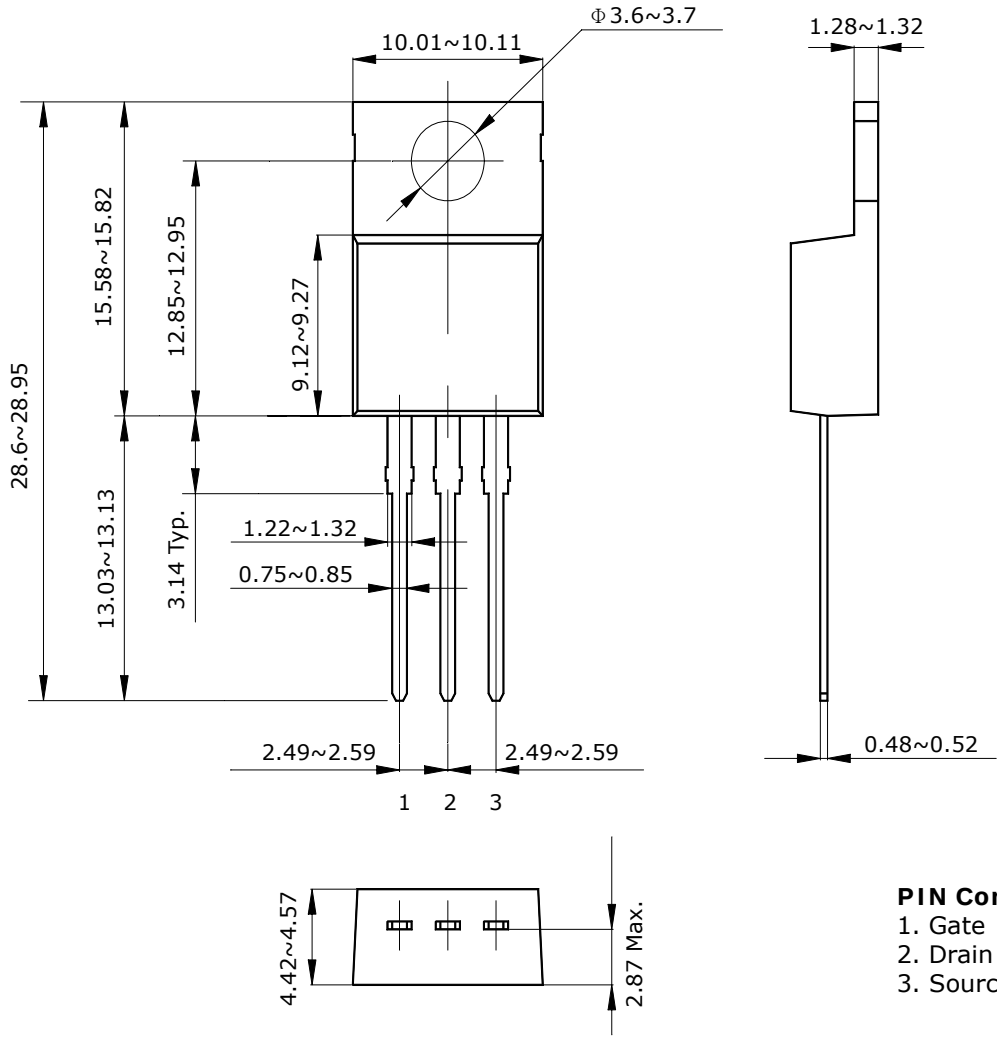
- High Voltage: $BV_{DSS}$=600V(Min.)
- Low $C_{rss}$ : $C_{rss}$=13.8pF(Typ.)
- Low gate charge : Qg=41nC(Typ.)
- Low $R_{DS(on)}$ :$R_{DS(on)}$=0.65Ω(Max.)

## Ordering Information

| Type NO. | Marking | Package Code |
|---|---|---|
| MF12N60 | MF12N60 | TO-220C-3L |

## Outline Dimensions

**unit : mm**




**PIN Connections**
1. Gate
2. Drain
3. Source

## Absolute maximum ratings

(Tc=25°C)

| Characteristic | Symbol | | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | $V_{DSS}$ | | 600 | V |
| Gate-source voltage | $V_{GSS}$ | | ±30 | V |
| Drain current (DC)* | $I_D$ | (Tc=25℃) | 12 | A |
| | | (Tc=100℃) | 7.1 | A |
| Drain current (Pulsed)* | $I_{DM}$ | | 48 | A |
| Drain power dissipation | $P_D$ | | 210 | W |
| Avalanche current (Single) ② | $I_{AS}$ | | 12 | A |
| Single pulsed avalanche energy ② | $E_{AS}$ | | 700 | mJ |
| Avalanche current (Repetitive) ① | $I_{AR}$ | | 12 | A |
| Repetitive avalanche energy ① | $E_{AR}$ | | 11.6 | mJ |
| Junction temperature | $T_J$ | | 150 | ℃ |
| Storage temperature range | $T_{stg}$ | | -55~150 | |

* Limited by maximum junction temperature

| Characteristic | | Symbol | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Thermal resistance | Junction-case | $R_{th(J-C)}$ | - | 2.7 | ℃/W |
| | Junction-ambient | $R_{th(J-a)}$ | - | 62.5 | |

## Electrical Characteristics (Tc=25°C)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $BV_{DSS}$ | $I_D$=250μA, $V_{GS}$=0 | 600 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $I_D$=250μA, $V_{DS}$= $V_{GS}$ | 2.0 | - | 4.0 | V |
| Drain-source cut-off current | $I_{DSS}$ | $V_{DS}$=600V, $V_{GS}$=0V | - | - | 1 | μA |
| Gate leakage current | $I_{GSS}$ | $V_{DS}$=0V, $V_{GS}$=±30V | - | - | ±100 | nA |
| Drain-source on-resistance ④ | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=6.0A | - | 0.55 | 0.65 | Ω |
| Forward transfer conductance ④ | $g_{fs}$ | $V_{DS}$=10V, $I_D$=6.0A | - | 10 | - | S |
| Input capacitance | Ciss | $V_{GS}$=0V, $V_{DS}$=25V f=1MHz | - | 2213 | 2951 | pF |
| Output capacitance | Coss | | - | 170 | 226 | |
| Reverse transfer capacitance | Crss | | - | 13.8 | 18.4 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=300V, $I_D$=12A $R_G$=25Ω ③④ | - | 30 | - | ns |
| Rise time | $t_r$ | | - | 85 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 140 | - | |
| Fall time | $t_f$ | | - | 90 | - | |
| Total gate charge | $Q_g$ | $V_{DS}$=480V, $V_{GS}$=10V $I_D$=12A ③④ | - | 41 | 63 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 13 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 10.5 | - | |

## Source-Drain Diode Ratings and Characteristics (Tc=25°C)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Source current (DC) | $I_S$ | Integral reverse diode in the MOSFET | - | - | 12 | A |
| Source current (Pulsed) ① | $I_{SM}$ | | - | - | 48 | |
| Forward voltage ④ | $V_{SD}$ | $V_{GS}$=0V, $I_S$=12A | - | - | 1.4 | V |
| Reverse recovery time | $t_{rr}$ | $I_s$=12A, $V_{GS}$=0, $di_S/dt$=100A/ us | - | 500 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 4.3 | - | uC |

Note ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=20mH, $I_{AS}$=8A, $V_{DD}$=50V, $R_G$=25Ω , Starting $T_J$ = 25℃

③ Pulse Test : Pulse Width < 300us, Duty cycle≤ 2%

④ Essentially independent of operating temperature

## Electrical Characteristic Curves

**Fig. 1 $I_D$ - $V_{DS}$**

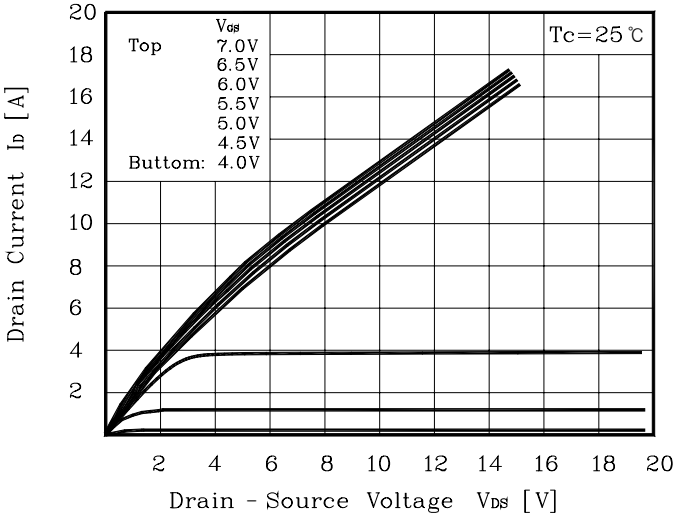



**Fig. 2 $I_D$ - $V_{GS}$**

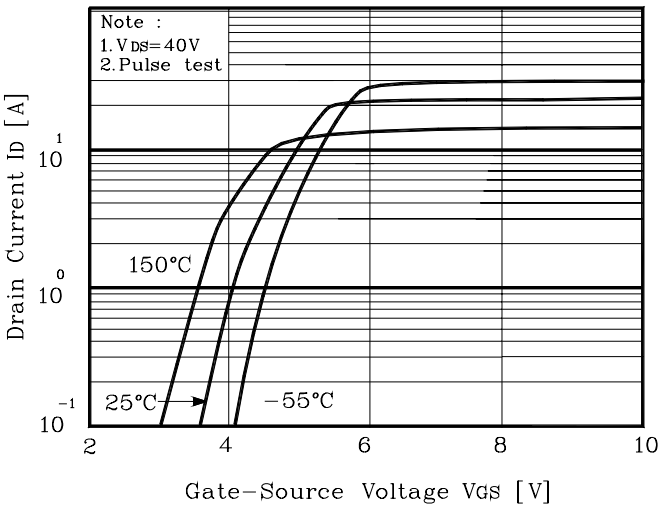



**Fig. 3 $R_{DS(on)}$ - $I_D$**

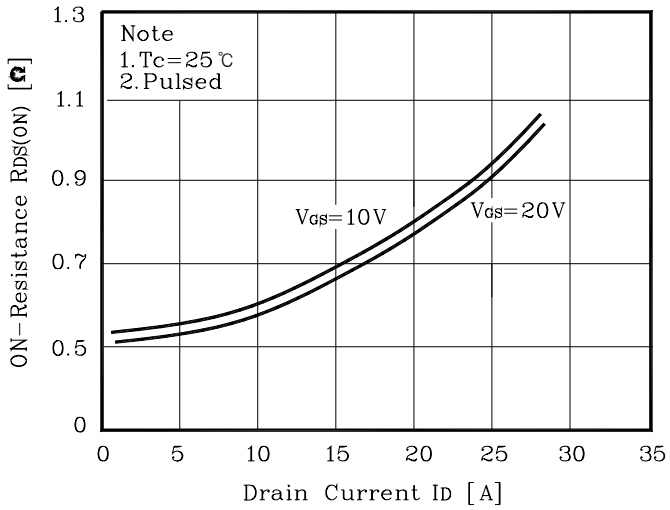



**Fig. 4 $I_S$ - $V_{SD}$**

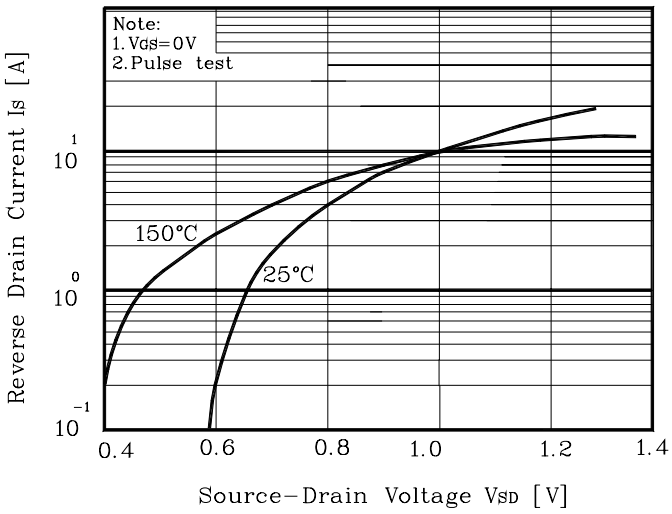



**Fig. 5 Capacitance - $V_{DS}$**

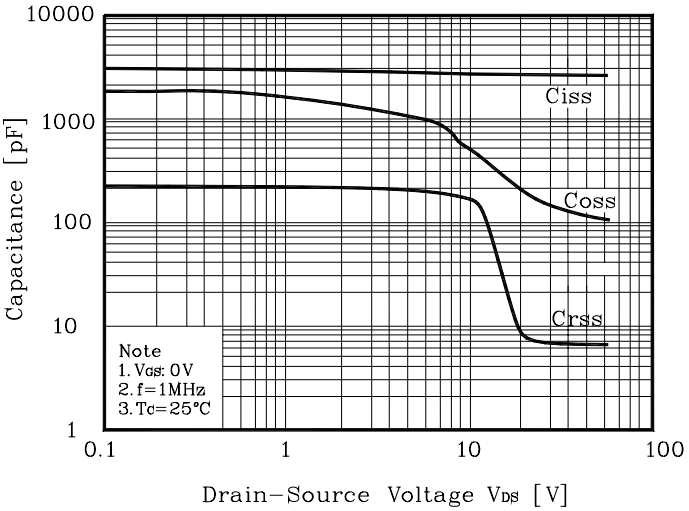
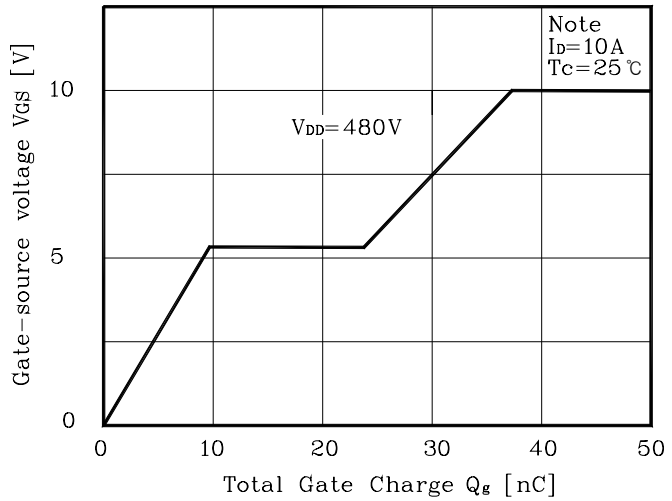



**Fig.6 $V_{GS}$ - $Q_G$**



## Electrical Characteristic Curves

**Fig. 7 $V_{DSS}$ - $T_J$**

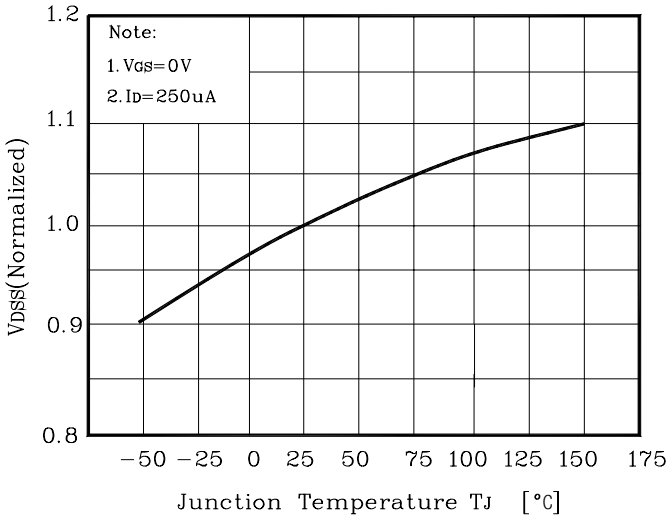



**Fig.8 $R_{DS(on)}$ - $T_J$**

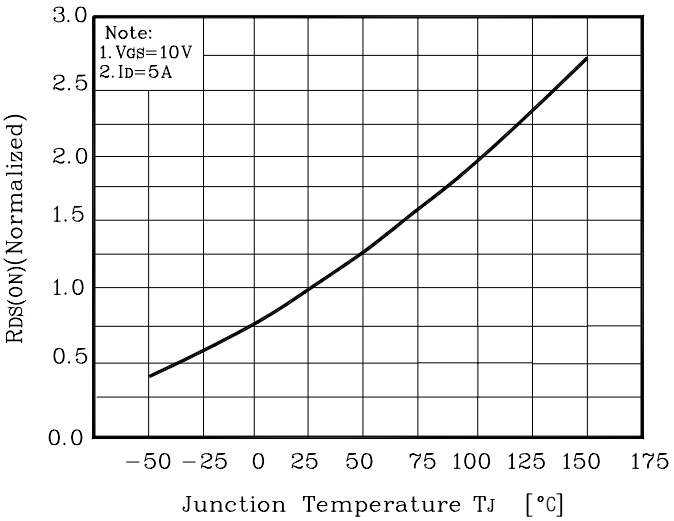



**Fig. 9 $I_D$ - $T_C$**

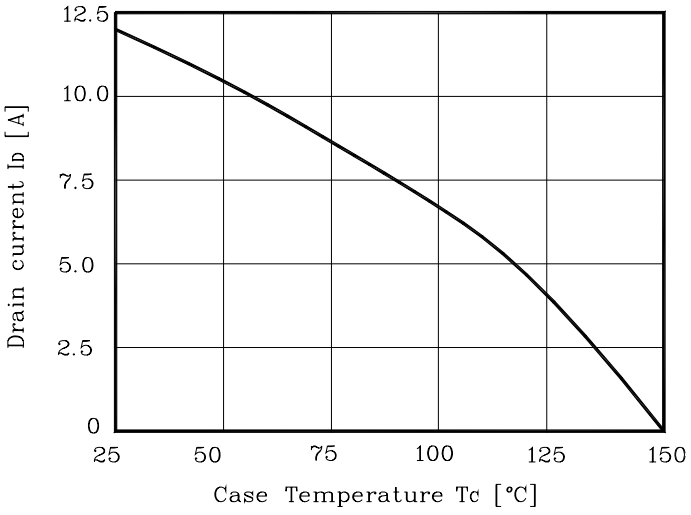



**Fig. 10 Safe Operating Area**

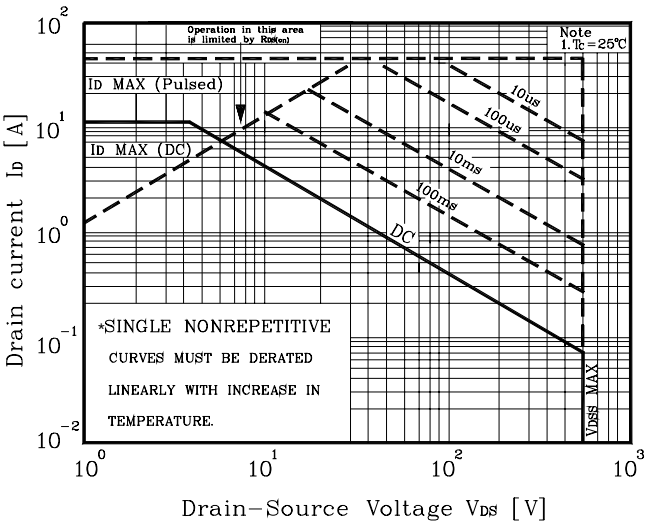


**Fig. 10 Gate Charge Test Circuit & Waveform**

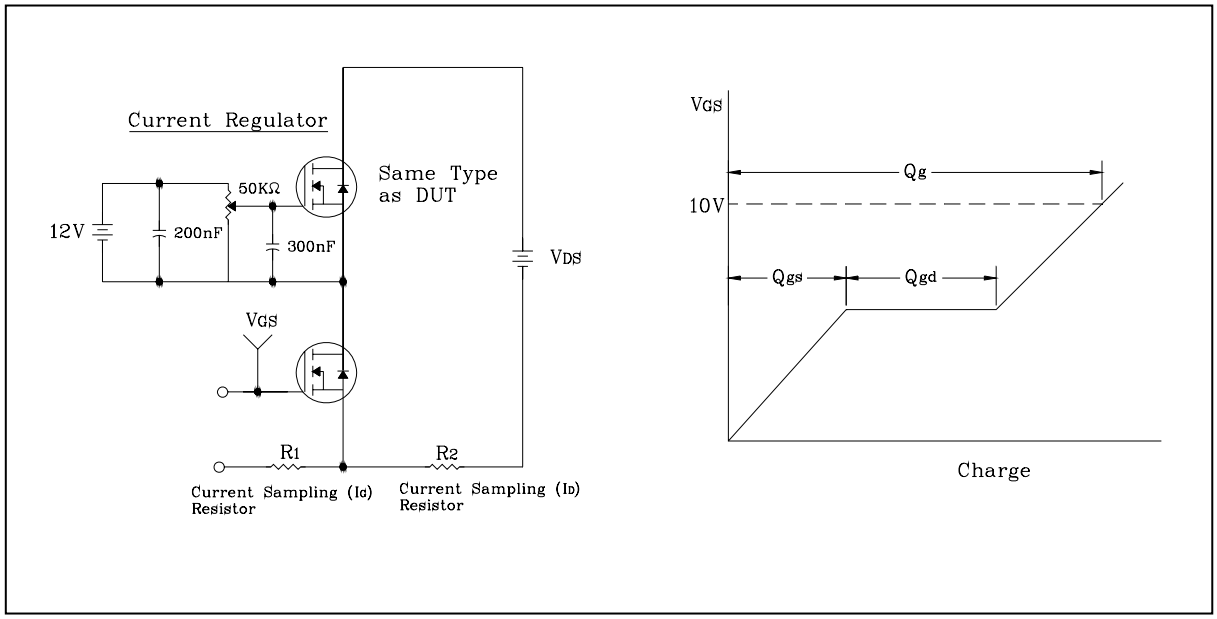



**Fig. 11 Resistive Switching Test Circuit & Waveform**

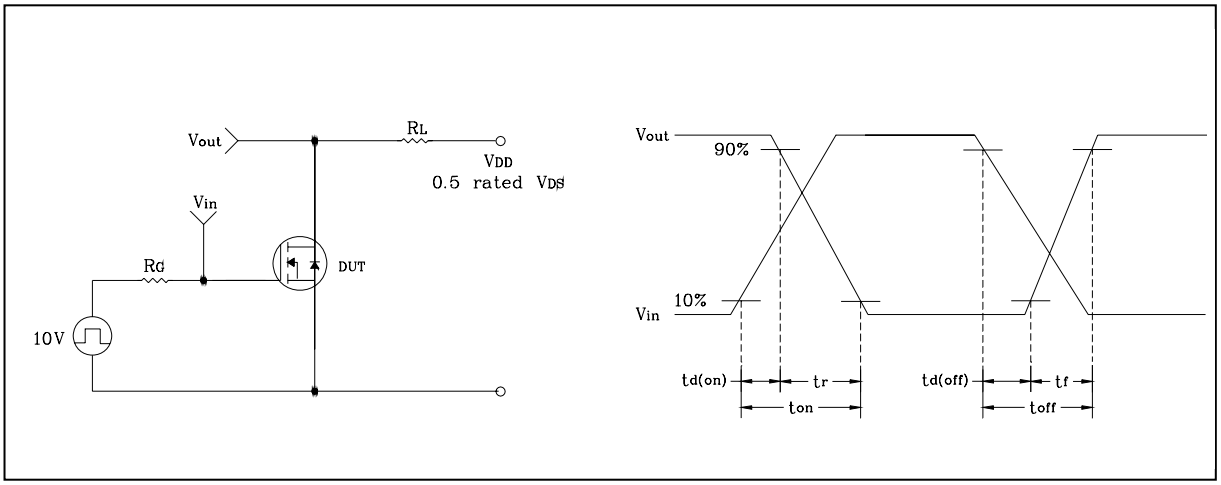



**Fig. 12 $E_{AS}$ Test Circuit & Waveform**

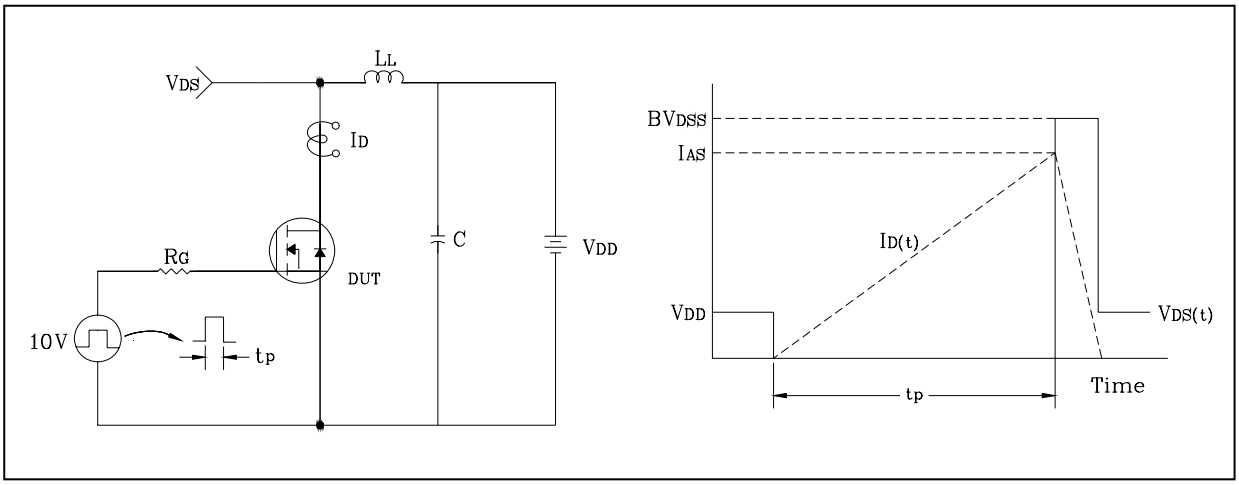


**Fig. 13 Diode Reverse Recovery Time Test Circuit & Waveform**