MP1608C

5.5V, 6A, Synchronous Step-Down Converter with FCCM in SOT583 Package

DESCRIPTION

The MP1608C is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. It achieves 6A of continuous output current (I_{OUT}) from a 2.4V to 5.5V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.4V.

The constant-on-time (COT) control scheme provides fast transient response and facilitates loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP1608C is well-suited for a wide range of applications including high-performance digital signal processors (DSPs), wireless power, portable and mobile devices, and other low-power systems.

The MP1608C requires a minimal number of readily available, standard external components. It is available in an ultra-small SOT583 package.

FEATURES

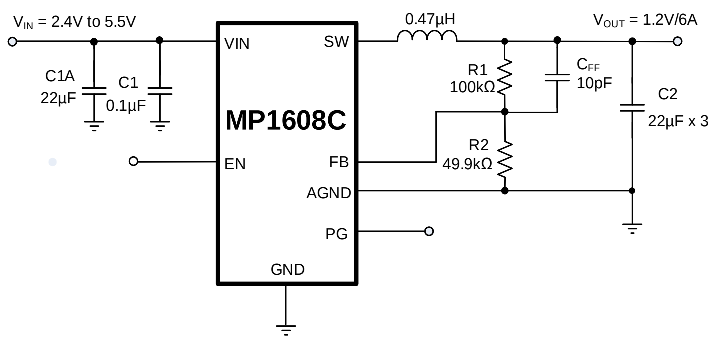
- Wide 2.4V to 5.5V Operating Input Voltage (V_{IN}) Range
- Up to 6A Output Current (I_{OUT})
- 15mΩ and 9mΩ Internal Power MOSFET Switches
- Forced Continuous Conduction Mode (FCCM)
- 1.25MHz Switching Frequency (f_{SW})
- Enable (EN) Function
- High Feedback Accuracy:
  - ±0.75% at Junction Temperature (T_J) = 25°C
  - ±1% at T_J = -40°C to +125°C
- Output Discharge Function
- Short-Circuit Protection (SCP) with Hiccup Mode
- Power Good (PG) Indication
- Available in an SOT583 Package

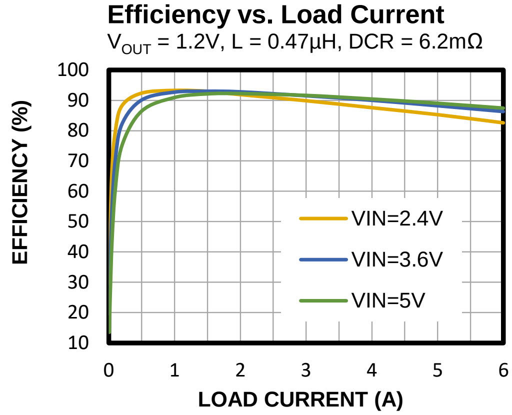
MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

APPLICATIONS

- IP Cameras
- Notebooks and PCs
- SSD/Optical Modules
- Multi-Function Printers
- Battery-Powered Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1608CGTL	SOT583	*See Below*	1

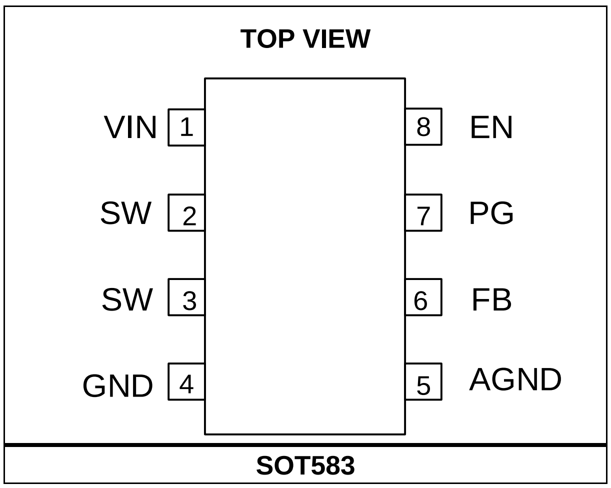
* For Tape & Reel, add suffix -Z (e.g. MP1608CGTL-Z).

TOP MARKING

BZUY
LLL

BZU: Product code of MP1608CGTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The MP1608C operates from a 2.4V to 5.5V input. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
2, 3	SW	**Output switching node.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
4	GND	**Power ground.**
5	AGND	**Signal ground.**
6	FB	**Feedback pin.** An external resistor divider connected from the output to AGND, tapped to the FB pin, sets the output voltage (V_{OUT}).
7	PG	**Power good indicator.** The output of this pin is an open drain.
8	EN	**On/off control.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW}..
..-0.3V (-5V for <10ns) to +6.5V (+8V for <10ns)
All other pins ....-0.3V to +6.5V
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
…………….. .... 2.3W
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... ±2000V
Charged-device model (CDM) .... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.4V to 5.5V
Output voltage (V_{OUT})............. 0.4V to V_{IN} x D_{MAX}
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
SOT583			
EVL1608C-TL-00A (4)	58	13	°C/W
JESD51-7 (5)	120	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a EVL1608C-TL-00A, 2-layer, 63.5mmx63.5mm PCB.
5) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) range			2.4		5.5	V
Under-voltage lockout (UVLO) rising threshold	$V_{INUVLO-R}$			2.25	2.35	V
UVLO threshold hysteresis	$V_{INUVLO-HYS}$			200		mV
Supply current (shutdown)	I_{SD}	V_{EN} = 0V, T_J = 25°C		0.2	0.5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.405V, T_J = 25°C		450		μA
Feedback voltage	V_{FB}	T_J = 25°C	397	400	403	mV
		T_J = -40°C to +125°C (7)	396	400	404	
Feedback current	I_{FB}	V_{FB} = 0.405V		10	50	nA
P-channel MOSFET (P-FET) switch on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V		15		mΩ
N-channel MOSFET (N-FET) switch on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V		9		mΩ
P-FET switch leakage	SW_{LKG_P}	V_{EN} = 0V, V_{SW} = 0V, T_J = 25°C		0	1	μA
N-FET switch leakage	SW_{LKG_N}	V_{EN} = 0V, V_{SW} = 5V, T_J = 25°C		2	3	μA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V	1100	1250	1400	kHz
Minimum on time (7)	t_{MIN-ON}			40		ns
P-FET peak current limit	I_{LIMIT_PEAK}	T_J = 25°C	7	9	11	A
N-FET valley current limit	I_{LIMIT_VALLEY}	T_J = 25°C	6	8	10	A
Soft-start time	t_{SS}	Time from 5% to 95% of the nominal output voltage (V_{OUT})		1		ms
Power good (PG) under-voltage (UV) rising threshold	$V_{PG\_R\_UV}$	FB rising edge		95		%
PG UV falling threshold	$V_{PG\_F\_UV}$	FB falling edge		90		%
Power good (PG) over-voltage (OV) rising threshold	$V_{PG\_R\_OV}$	Refer to V_{FB}		110		%
PG OV falling threshold	$V_{PG\_F\_OV}$	Refer to V_{FB}		105		%
PG rising delay	$t_{PG\_R\_DLY}$	PG rising edge		50		μs
PG falling delay	$t_{PG\_F\_DLY}$	PG falling edge		35		μs
PG sink current capability	V_{PG-L}	Sink 1mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Enable (EN) turn-on delay	$t_{EN\_ON\_DLY}$	EN on to SW active		500		µs
EN turn-off delay	$t_{EN\_OFF\_DLY}$	EN off to stop switching		10		µs
EN input logic low voltage	V_{EN_LOW}				0.4	V
EN input logic high voltage	V_{EN_HIGH}		1.2			V
EN pull-down resistor	R_{EN}			1.65		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		54		Ω
EN input current	I_{EN}	V_{EN} = 2V		0.1		µA
		V_{EN} = 0V		0		µA
Low-side current limit	$I_{LIMIT\_LOW\_SIDE}$			-3		A
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

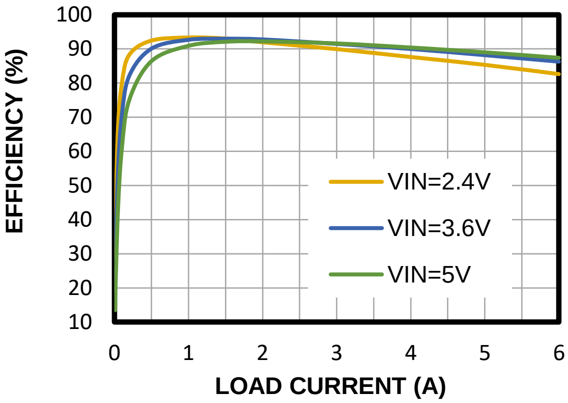
Notes:

6) Not tested in production. Derived by over-temperature correlation.
7) Derived by sample characterization. Not tested in production.

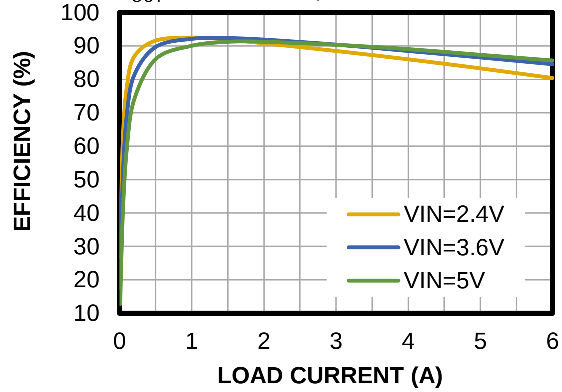
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

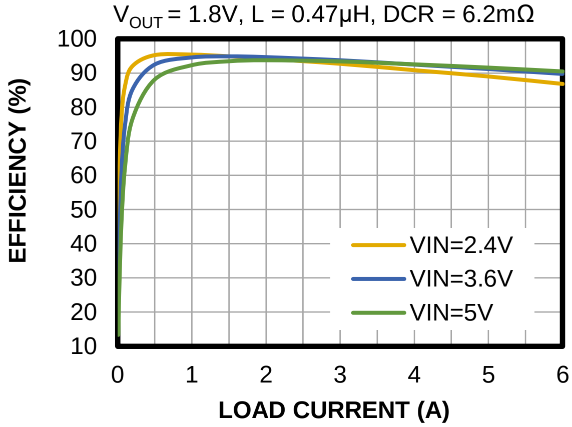
Efficiency vs. Load Current
V_{OUT} = 1.2V, L = 0.47µH, DCR = 6.2mΩ



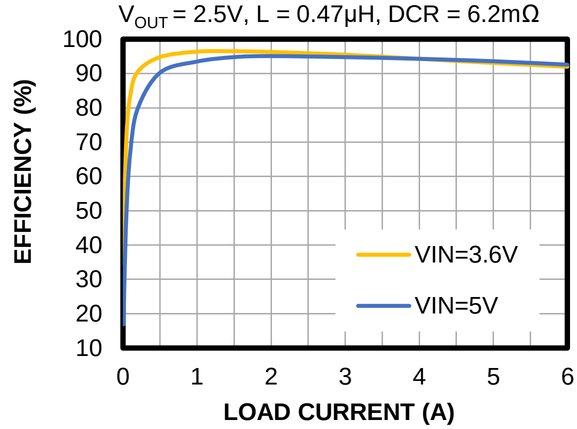
Efficiency vs. Load Current
V_{OUT} = 1V, L = 0.47µH, DCR = 6.2mΩ



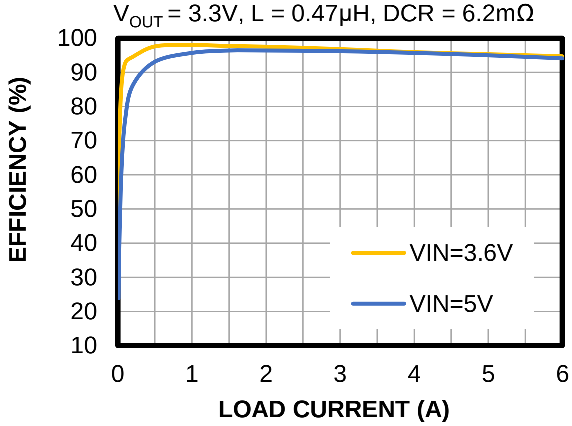
Efficiency vs. Load Current
V_{OUT} = 1.8V, L = 0.47µH, DCR = 6.2mΩ



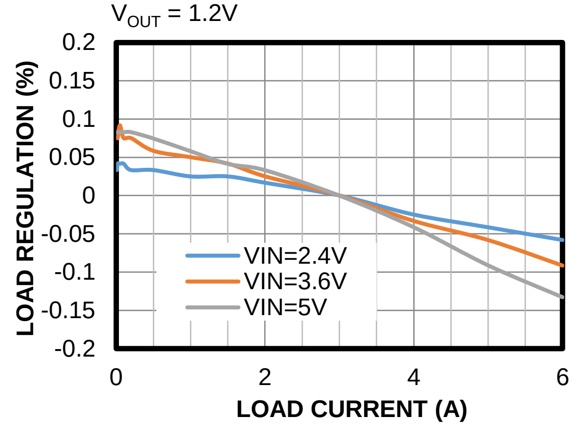
Efficiency vs. Load Current
V_{OUT} = 2.5V, L = 0.47µH, DCR = 6.2mΩ



Efficiency vs. Load Current
V_{OUT} = 3.3V, L = 0.47µH, DCR = 6.2mΩ



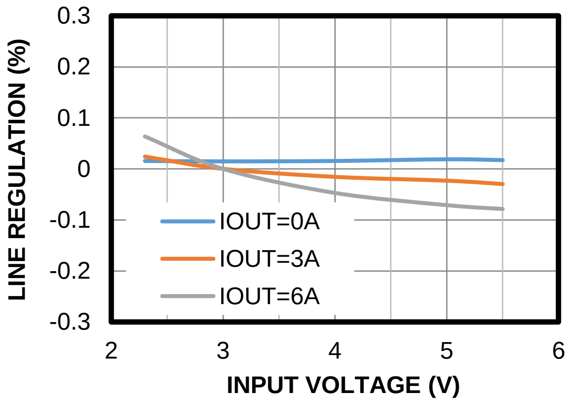
Load Regulation
V_{OUT} = 1.2V



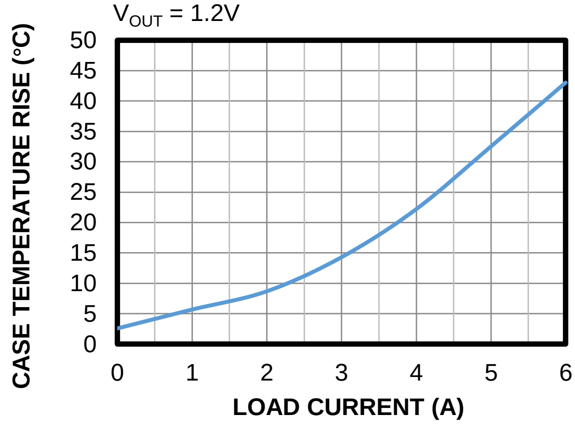
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

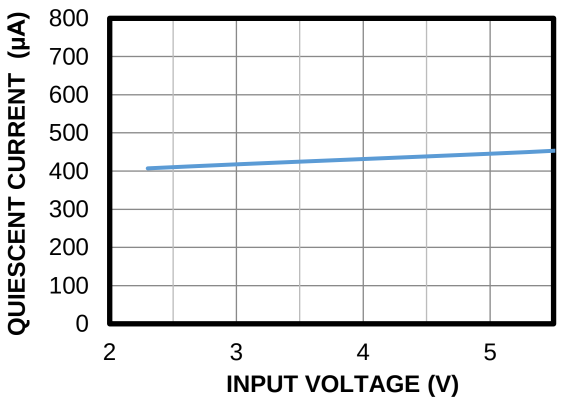
Line Regulation
V_{OUT} = 1.2V



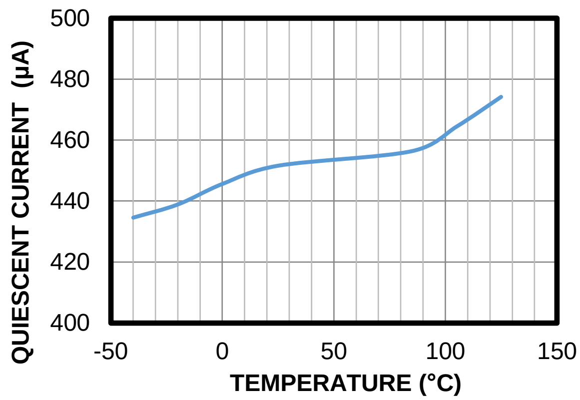
Case Temperature Rise vs. Load Current
V_{OUT} = 1.2V



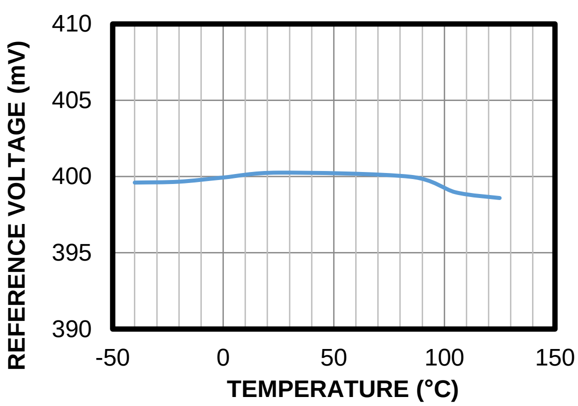
Quiescent Current vs. Input Voltage



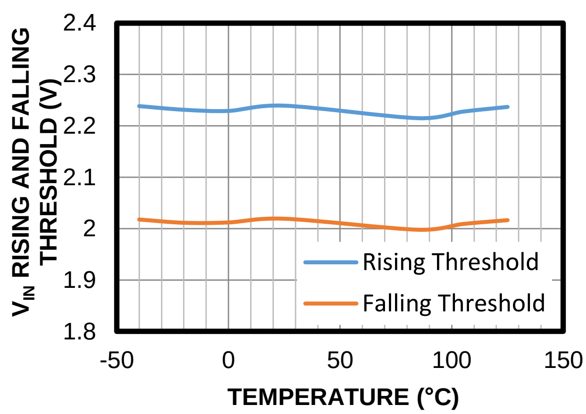
Quiescent Current vs. Temperature



Reference Voltage vs. Temperature

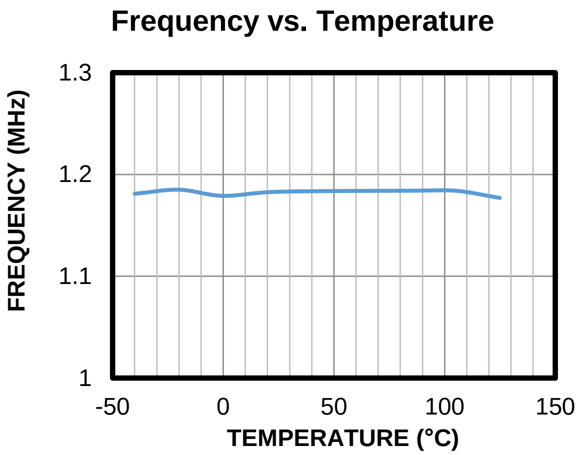


V_{IN} Rising and Falling Threshold vs.Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

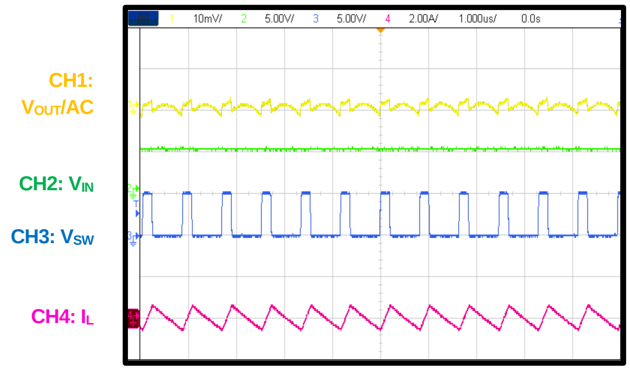


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

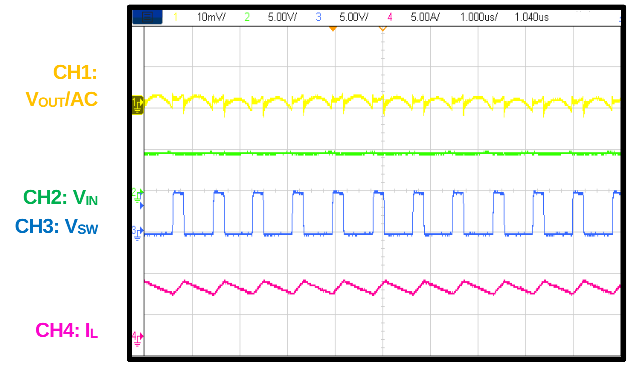
Output Voltage Ripple

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



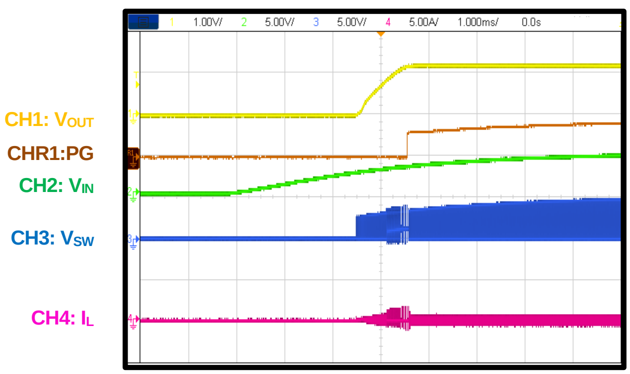
Output Voltage Ripple

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



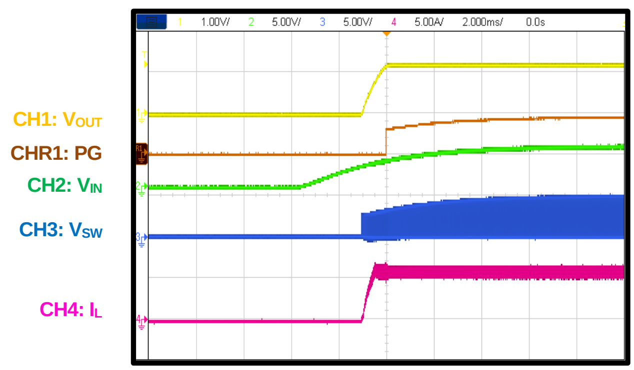
Start-Up through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



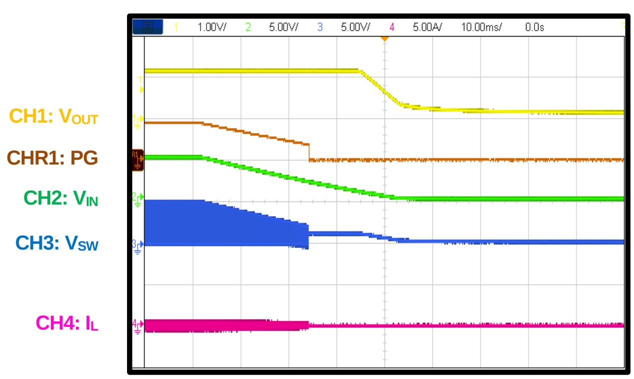
Start-Up through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



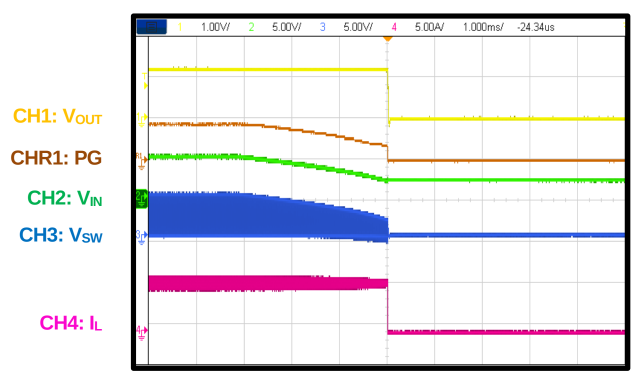
Shutdown through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



Shutdown through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A

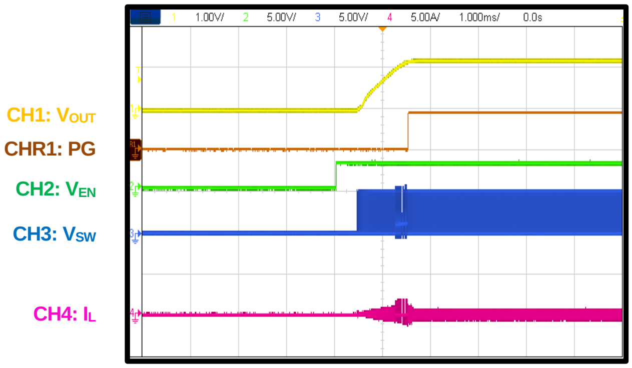


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47μH, T_A = 25°C, unless otherwise noted.

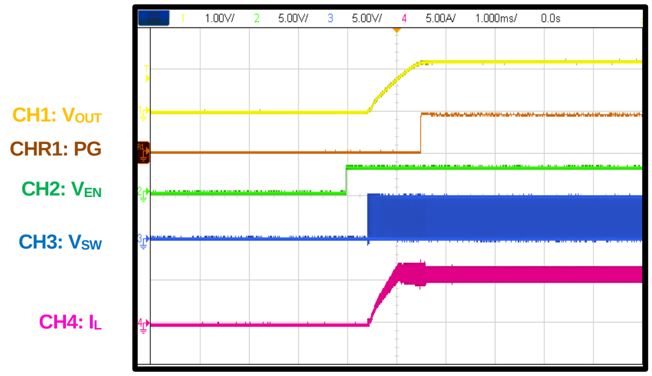
Start-Up through EN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



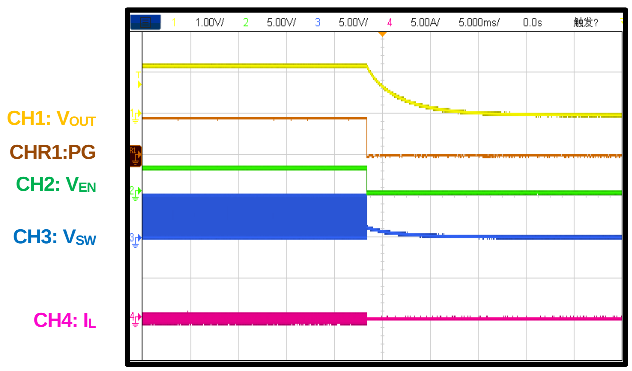
Start-Up through EN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



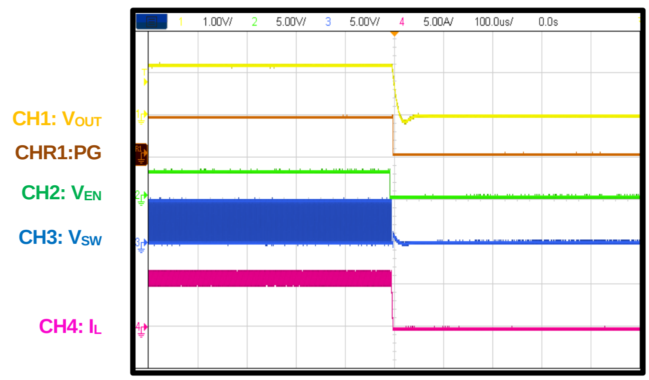
Shutdown through EN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



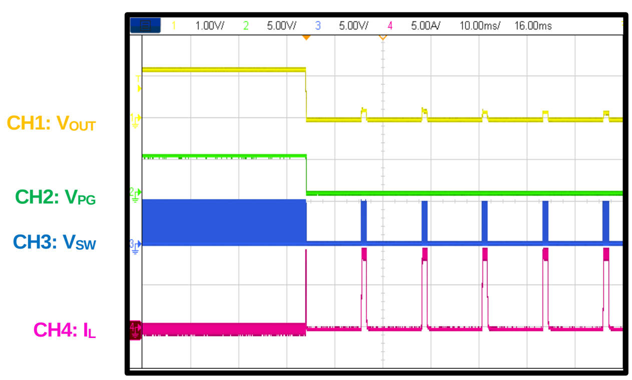
Shutdown through EN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



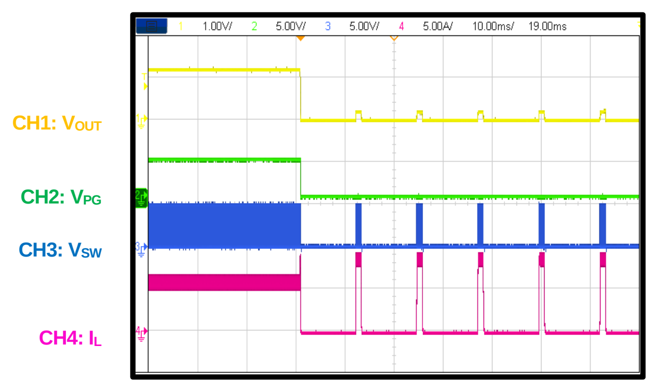
SCP Entry

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



SCP Entry

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A

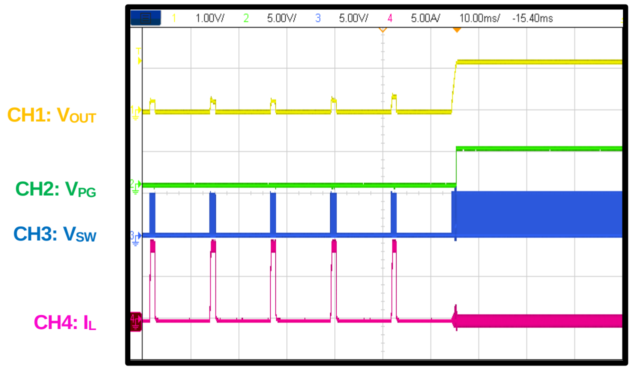


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47μH, T_A = 25°C, unless otherwise noted.

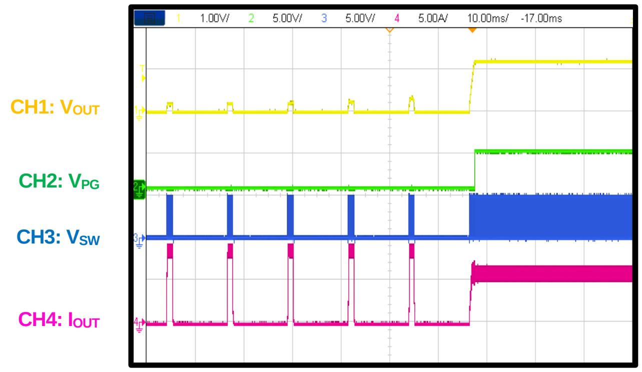
SCP Recovery

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



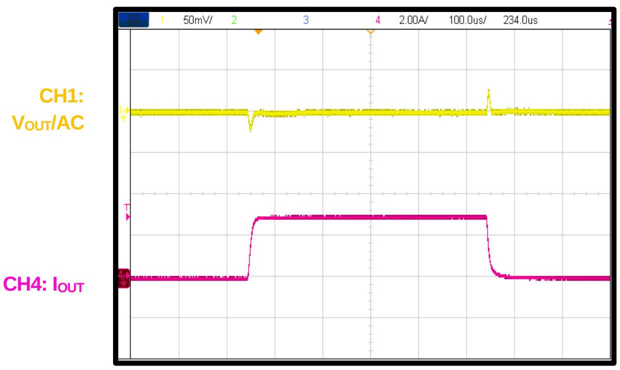
SCP Recovery

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A



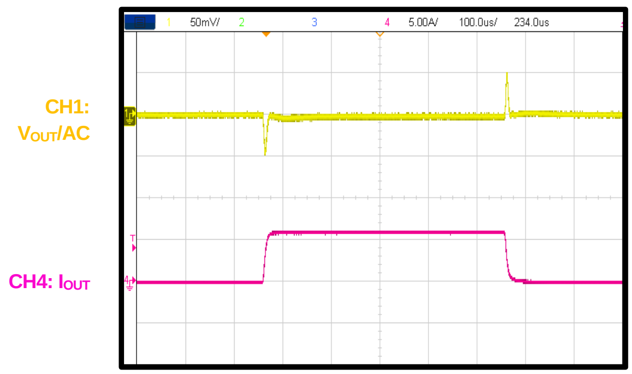
Load Transient Response

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A to 3A, 2.5A/μs with e-load



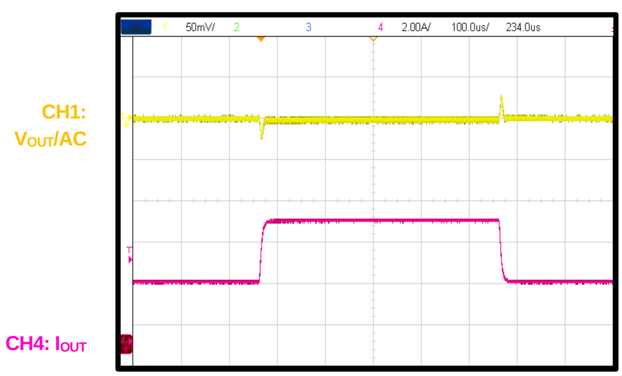
Load Transient Response

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A to 6A, 2.5A/μs with e-load



Load Transient Response

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A to 6A, 2.5A/μs with e-load



FUNCTIONAL BLOCK DIAGRAM

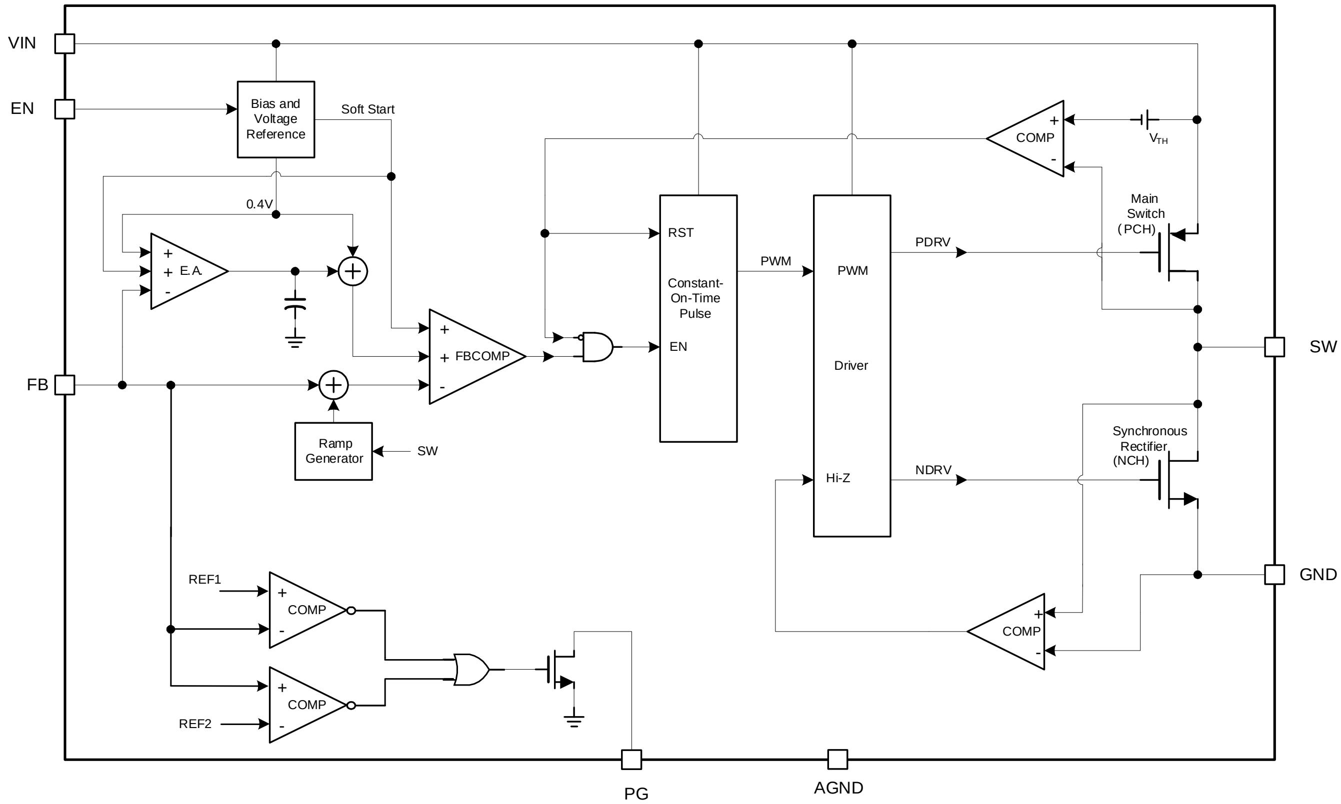


Figure 1: Functional Block Diagram

OPERATION

The MP1608C uses constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the full V_{IN} range. It achieves 6A of continuous output current (I_{OUT}) from a 2.4V to 5.5V V_{IN} with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.4V.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and a faster transient response. By using V_{IN} feed-forward, the MP1608C maintains a nearly constant f_{SW} across the V_{IN} and V_{OUT} ranges. The switching pulse on time (t_{ON}) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.83\mu s \tag{1}$$

To prevent inductor current (I_L) runaway during load transients, the MP1608C has a fixed minimum off time and valley current protection.

Enable (EN)

When V_{IN} exceeds the under-voltage lockout (UVLO) threshold, the MP1608C can be enabled by pulling the EN pin above 1.2V. Leave the EN pin floating or pull it down to ground to disable the MP1608C. There is an internal 1.65MΩ resistor connected from EN pin to ground.

When the device is disabled, the part goes into output discharge mode automatically, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Internal Soft Start (SS)

The MP1608C has an internal soft start (SS) that ramps up V_{OUT} at a controlled slew rate to prevent overshoot during start-up. The soft-start time (t_{SS}) is 1ms typically.

Current Limit

The MP1608C has a high-side switch current limit. When the high-side switch reaches its current limit, the MP1608C remains in hiccup mode until the current drops. This prevents I_L from continuing to rise and damaging the components.

Short-Circuit Protection (SCP) and Recovery

The MP1608C enters short-circuit protection (SCP) mode when it reaches the current limit, and it tries to recover with hiccup mode. The MP1608C disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the short-circuit condition remains after soft start ends, the MP1608C repeats this cycle until the short-circuit condition disappears and the output voltage rises back to its regulation level.

Power Good (PG) Indicator

The MP1608C has an open-drain output and requires an external pull-up resistor (100kΩ to 500kΩ) for the power good indicator. When the feedback voltage (V_{FB}) exceeds 90% of the regulation voltage, the PG pin's voltage (V_{PG}) is pulled up to V_{OUT} or V_{IN} by the external resistor. If V_{FB} exceeds this window, the internal MOSFET pulls PG to ground.

When VIN and EN are not available, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 2 shows the relationship between the PG voltage and the pull-up current.

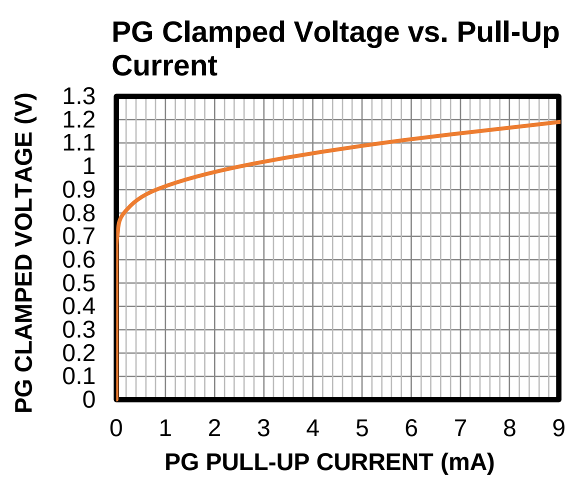


Figure 2: PG Clamped Voltage

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Figure 3). Select the feedback resistor (R1, typically between 100kΩ and 200kΩ) that reduces the VOUT leakage current. There is no strict requirement on the feedback resistor. Select R1 to exceed 10kΩ. R2 can then be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.4} - 1} \quad (2)$$

Figure 2 shows the feedback circuit.

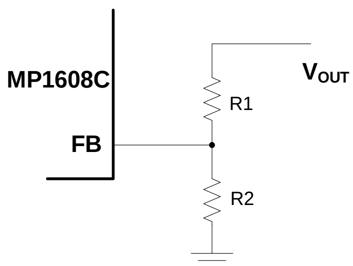


Figure 3: Feedback Network

Table 1 shows the recommended parameters for common V_{OUT} values.

Table 1: Parameter Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)
1	100	64.9	0.47
1.2	100	49.9	0.47
1.8	105	30	0.47
2.5	105	20	0.47
3.3	110	15	0.47

Selecting the Inductor

Optimized Performance with MPS Inductor MPL-AL4020 Series

Most applications work best with a 0.47µH to 1.5µH inductor. Select an inductor with a DC resistance below 25mΩ to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device has strong electromagnetic inference within the system. Do not use un-shielded power inductors, as they provide poor magnetic shielding. Shielded inductors, such as metal alloy or multi-player chip powers, are the best candidates for applications because they effectively decrease interference.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Suggested Inductor List

Manufacturer PN	Inductance (µH)	Manufacturer
MPL-AL4020-R47	0.47	MPS
MPL-AL4020-R68	0.68	MPS
MPL-AL4020-1R0	1.0	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

For most designs, calculate the inductance with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating, because it absorbs the input switching current.

Calculate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, estimated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be calculated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2, also known as C_{OUT}) stabilizes the DC output voltage. Ceramic capacitors are recommended. Low-ESR capacitors are recommended to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductance and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Proper layout of the switching power supply is critical for efficient device functioning. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the VIN and GND pins.
3. Place the external feedback resistors next to the FB pin.
4. Keep the switching node (SW) short and route it away from the feedback network.
5. Route the V_{OUT} sense line away from the power inductor.
6. Place the V_{OUT} sensing point close to C_{OUT}.
7. Add some GND vias around the GND pin.

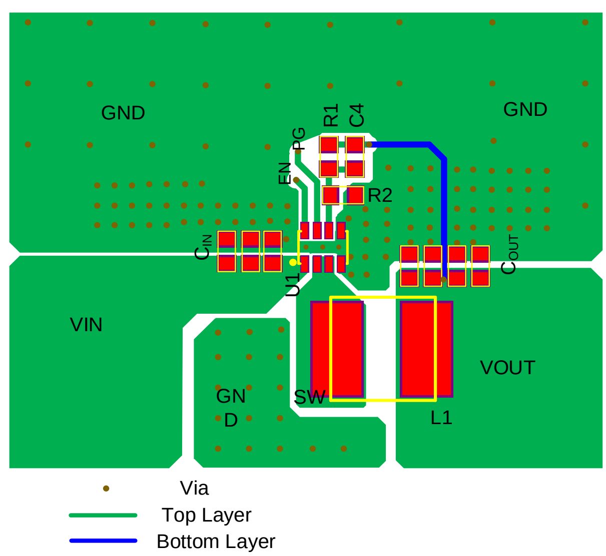


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS (8)

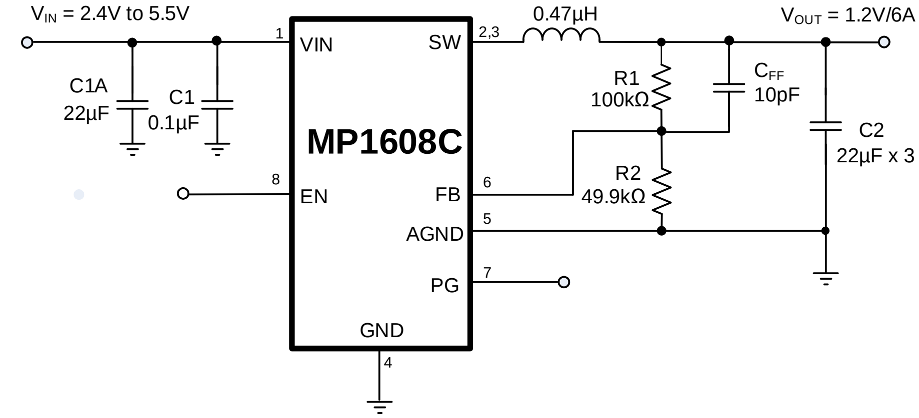


Figure 5: Typical Application Circuit (V_{IN} = 2.4V to 5.5V, V_{OUT} = 1.2V/6A)

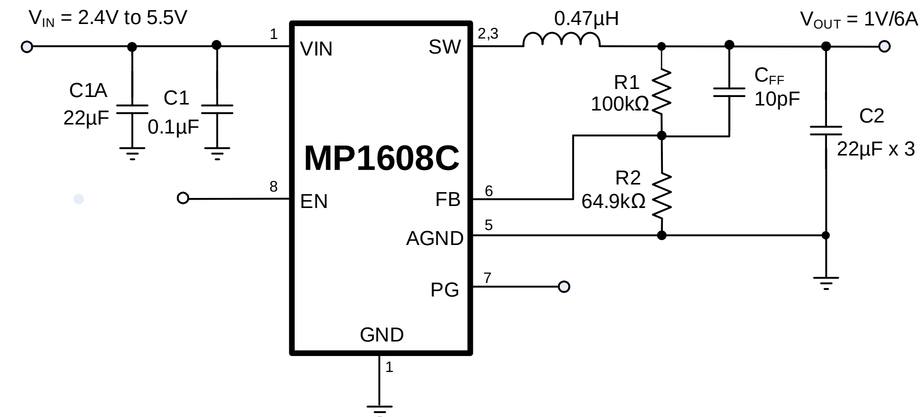


Figure 6: Typical Application Circuit (V_{IN} = 2.4V to 5.5V, V_{OUT} = 1V/6A)

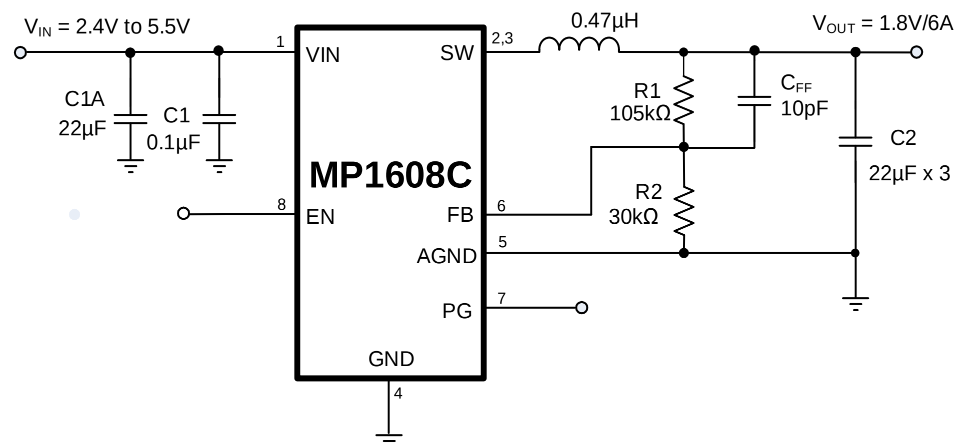


Figure 7: Typical Application Circuit (V_{IN} = 2.4V to 5.5V, V_{OUT} = 1.8V/6A)

TYPICAL APPLICATION CIRCUITS *(continued)* (8)

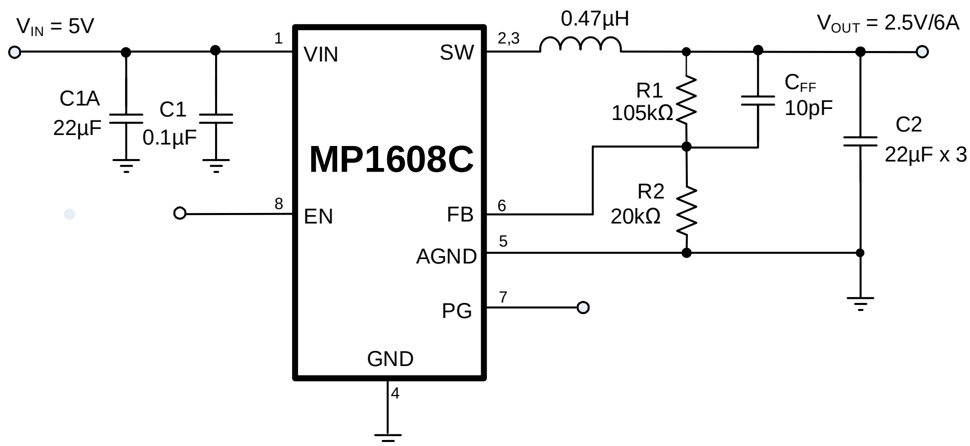


Figure 8: Typical Application Circuit (V_{IN} = 5V, V_{OUT} = 2.5V/6A)

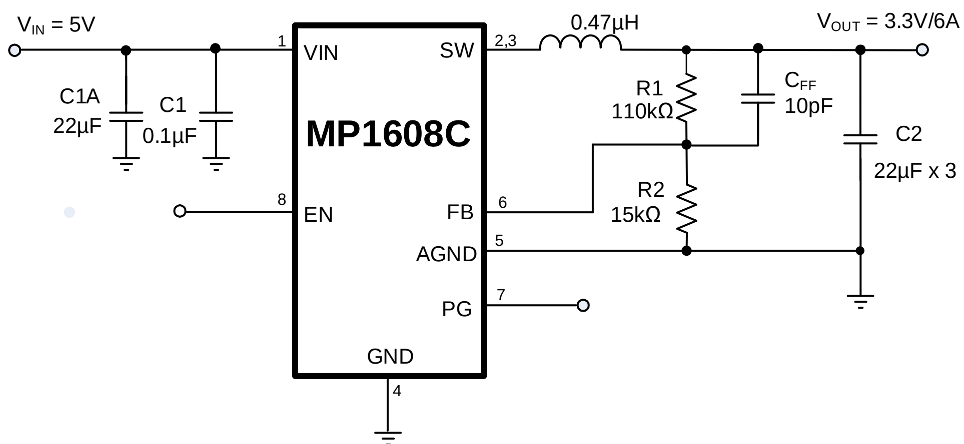


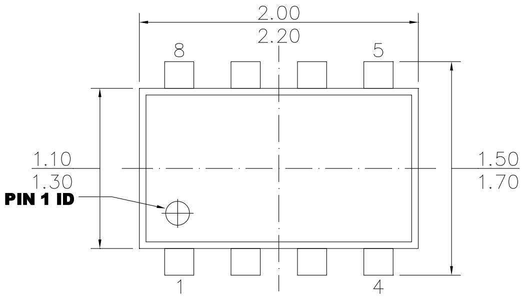
Figure 9: Typical Application Circuit (V_{IN} = 5V, V_{OUT} = 3.3V/6A)

Note:

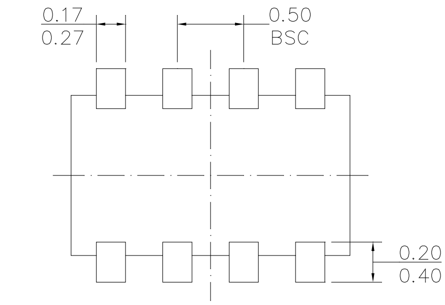
8) If V_{IN} < 3.3V, additional input capacitance may be required.

PACKAGE INFORMATION

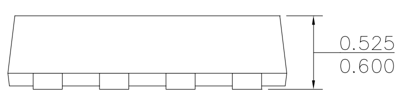
SOT583



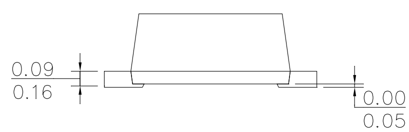
TOP VIEW



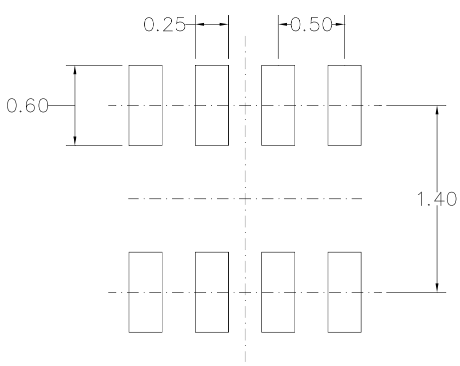
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

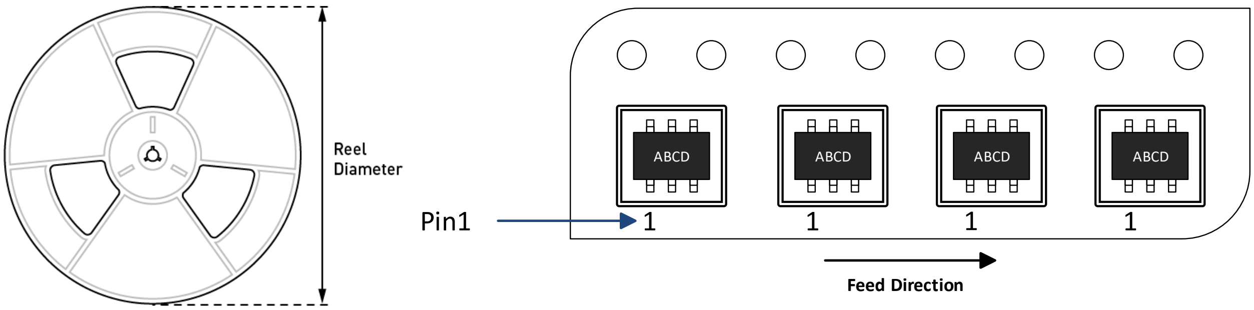


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1608CGTL-Z	SOT583	5000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/5/2024	Initial Release	-