MP1652

High-Efficiency, 2A, 18V, 680kHz Synchronous, Step-Down Converter In SOT 563

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP1652 is a fully-integrated high-frequency, synchronous rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input range, with excellent load and line regulation. The MP1652 has synchronous-mode operation for higher efficiency over the output current-load range.

Constant On-Time control operation provides very fast transient response and easy loop design as well as very tight output regulation.

Full protection features include SCP, OCP, UVP and thermal shutdown.

The MP1652 requires a minimal number of readily-available, standard, external components and is available in a space-saving SOT563 package.

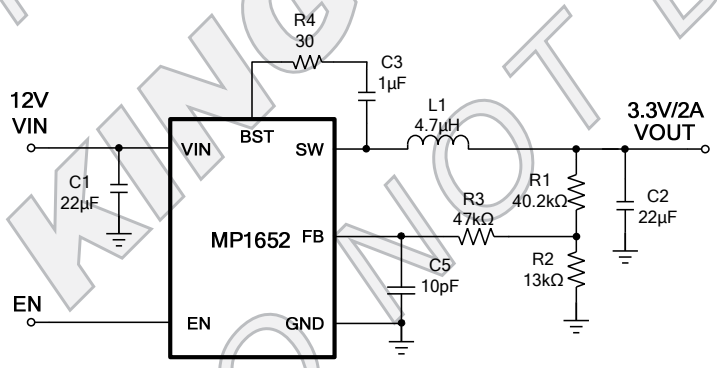
FEATURES

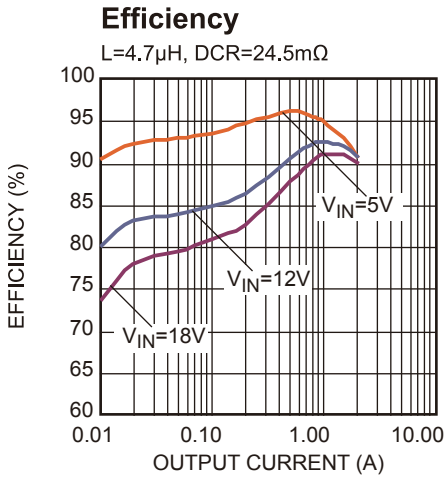
- Wide 4.2V-to-18V Operating Input Range
- 130mΩ/65mΩ Low-$R_{DS(ON)}$ Internal Power MOSFETs
- 180μA Low Iq
- High-Efficiency Synchronous-Mode Operation
- Power Save Mode at Light Load
- Fast Load Transient Response
- 680kHz Switching Frequency
- Internal Soft-Start
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a SOT563 package

APPLICATIONS

- Security Camera
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1652GTF	SOT563	*See below*

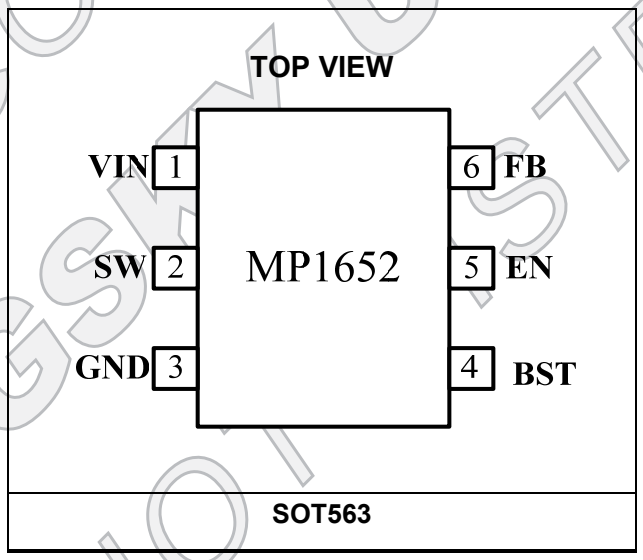
* For Tape & Reel, add suffix –Z (e.g. MP1652GTF–Z)

TOP MARKING

ATUY
LLL

ATU: Product code of MP1652GTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 20V
V_{SW}.....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BST} ..... V_{SW}+3.3V
V_{EN} ..... –0.3V to 6.5V (2)
All Other Pins.....–0.3V to 5V
Continuous Power Dissipation (T_A = +25°C) (3)
..... 1W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} .....4.2V to 18V
Output Voltage V_{OUT}.....
0.8V to V_{IN} x Dmax or 10V max
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}	
SOT563	130	60	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to Page 10, Enable Control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J=-40°C to +125°C(6), typical value is tested at T_J=+25°C, unless otherwise noted

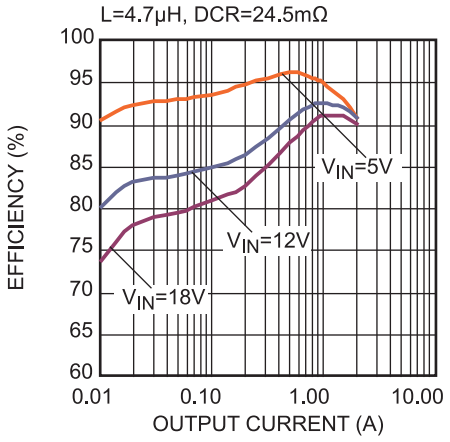
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 0.85V		0.18		mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}= 3.3V		130		mΩ
LS Switch-On Resistance	LS_{RDS-ON}			65		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			10	μA
Valley Current Limit	I_{LIMIT}			2.4		A
ZCD(7)	I_{ZCD}	VOUT=3.3V, Lo=4.7μH		50		mA
Oscillator Frequency	f_{SW}	V_{FB}=0.75V		680		kHz
Minimum On Time(7)	T_{ON_MIN}			30		ns
Minimum Off Time(7)	T_{OFF_MIN}			140		ns
Feedback Voltage	V_{REF}	T_J=-40°C to +125°C		807		mV
Feedback Current	I_{FB}			10	50	nA
FB UV threshold(H to L)	V_{UV_th}	Hiccup Entry		75%		Vref
Hiccup duty cycle(7)	D_{Hiccup}			25		%
EN Rising Threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN Hysteresis	V_{EN_HYS}			100		mV
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0		
V_{IN} Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$		3.7	4.1	4.2	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			330		mV
Soft-Start Period	T_{SS}		1	1.4	2	ms
Thermal Shutdown(7)	TSD			150		°C
Thermal Hysteresis(7)	TSD_{HYS}			20		°C

Notes:
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by design and engineering sample characterization.

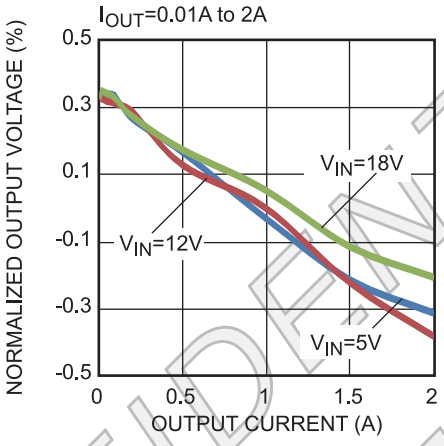
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

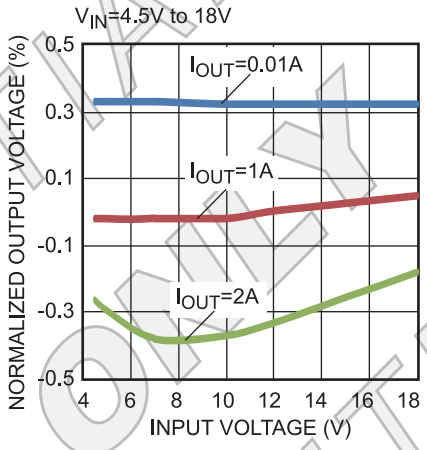
Efficiency



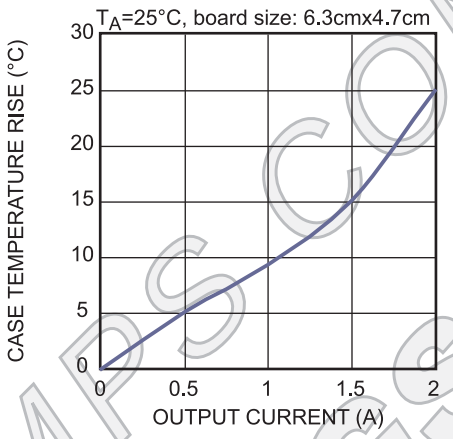
Load Regulation



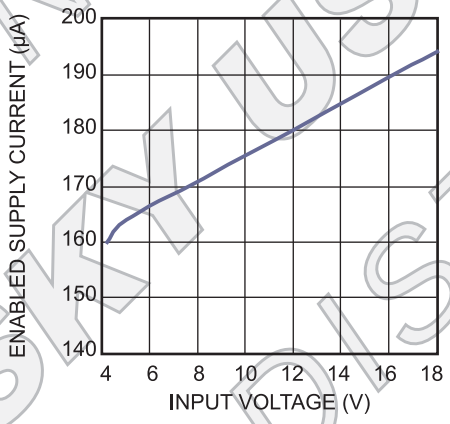
Line Regulation



Case Temperature Rise vs. Output Current



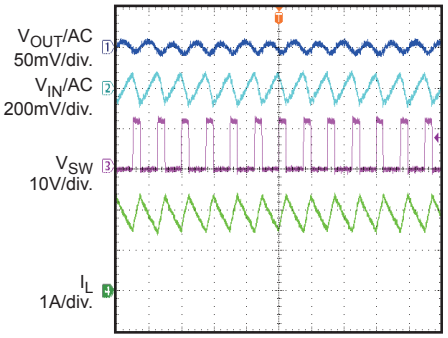
Enabled Supply Current vs. Input Voltage



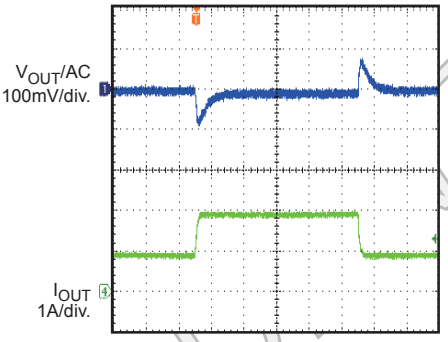
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

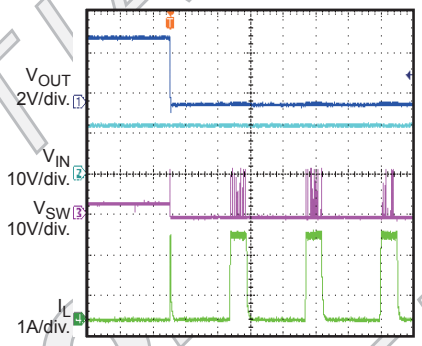
Input/Output Ripple
I_{OUT}=2A



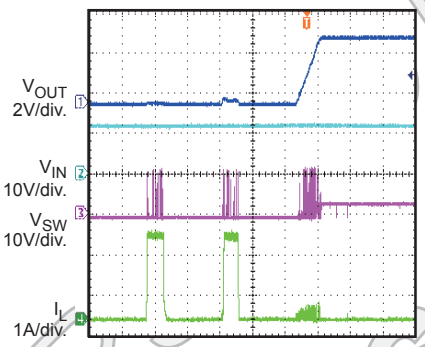
Transient Response
I_{OUT}=1A to 2A, 2.5A/µs



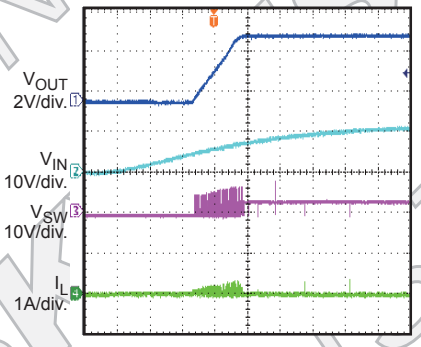
Short Circuit Entry
I_{OUT}=0A



Short Circuit Recovery
I_{OUT}=0A



Startup through Input Voltage
I_{OUT}=0A



Shutdown through Input Voltage
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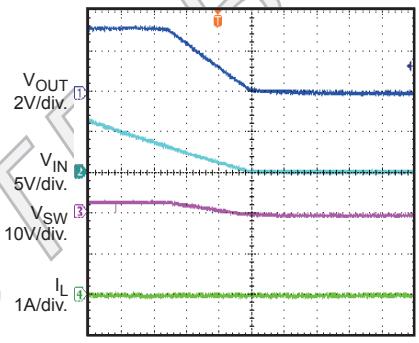
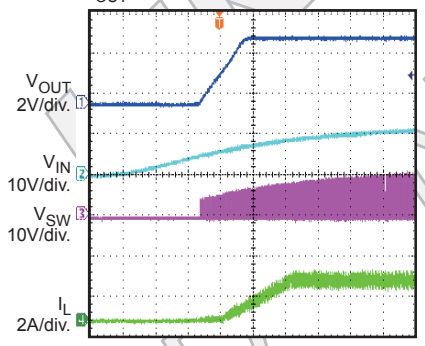
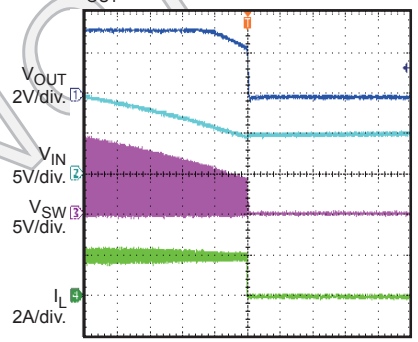


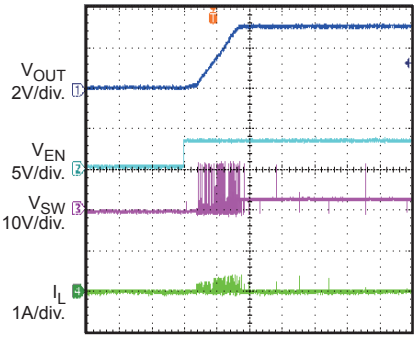
Startup through Input Voltage
I_{OUT}=2A



Shutdown through Input Voltage
I_{OUT}=2A



Startup through Enable
I_{OUT}=0A

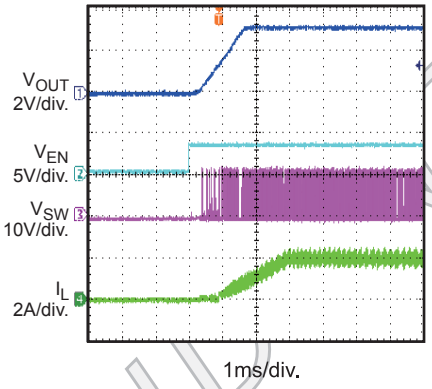


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

Startup through Enable

I_{OUT}=2A



PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN	Supply Voltage. The MP1652 operates from a 4.2V-to-18V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
2	SW	Switch Output. Connect using a wide PCB trace.
3	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
4	BST	Bootstrap. Connect a capacitor and a resistor between SW and BST pins to form a floating supply across the high-side switch driver. Use a 1μF BST capacitor.
5	EN	EN=HIGH to enable the MP1652. For automatic start-up, connect EN to VIN through 100k pull-up resistor.
6	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current-limit runaway during a short circuit fault.

BLOCK DIAGRAM

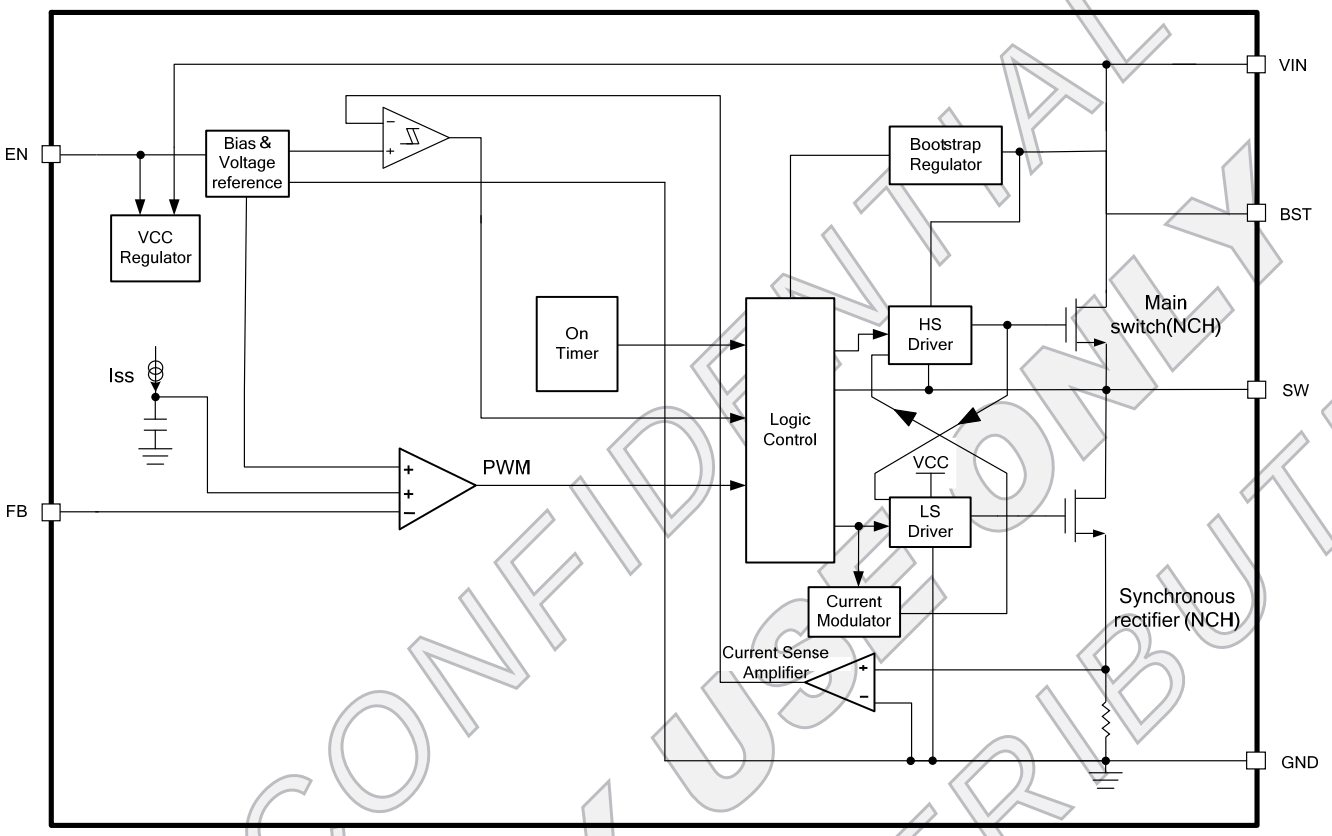


Figure 1: Functional Block Diagram

OPERATION

The MP1652 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS) is turned ON when the FB voltage drops below reference voltage. The HS is turned on for a fixed interval which is determined by one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS is turned off until next period. By repeating operation this way, the converter regulates the output voltage.

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The LS is turned on when HS is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS and LS are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time is internally generated between HS off and LS on, or LS off and HS on.

When the MP1652 works in PFM and during light-load operation—the MP1652 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS driver goes into tri-state (high Z). Hence, the output capacitors discharge slowly to GND through R1, and R2. When FB voltage drops below reference voltage, the HS is turned on. This operation greatly improves device efficiency when the output current is low.

Light-load operation is also called skip mode because the HS does not turn on as frequently as during heavy-load conditions. The frequency at which the HS turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Enable Control

EN is a digital control pin that turns the regulator on and off: Drive EN HIGH to turn on the regulator, drive it LOW to turn it off. An internal 1MΩ resistor from EN to GND allows EN to float to shutdown the IC.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VIN limits the EN input current less than 100μA to prevent damage the Zener diode. For example, connect 100k pull-up resistor to 12V VIN, I_{Zener}=(12V-2.8V)/(100k+35k)=68μA.

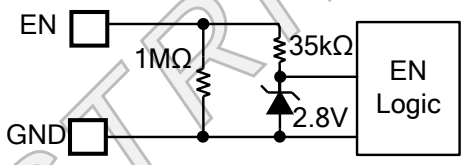


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1652 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.1V while its falling threshold is consistently 3.77V.

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.4ms.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP1652 has valley current limit control. During LS-FET ON state, the inductor current is monitored. When the sensed inductor current hits the valley current limit, the LS limit comparator (shown in Figure 1) turns over, the device enters over-current protection mode, HS-FET will wait until valley current limit disappear to turn on again. Meanwhile, the output voltage drops until VFB is below the under-voltage (UV) threshold—typically 75% below the reference. Once UV is triggered, the MP1652 enters hiccup mode to periodically restart the part.

During over-current protection, the device tries to recover from over-current fault with hiccup mode, that means the chip will disable output power stage, discharge soft-start and then automatically try to soft-start again. If the over-current condition still holds after soft-start ends, the device repeats this operation cycle till over-current conditions disappear and then output rises back to regulation level. So the OCP is non-latch protection.

Pre-bias startup

The MP1652 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the BST voltage will be refreshed and charged, the voltage on the soft-start will be charged too. If BST voltage exceeds its rising threshold voltage and Soft-start voltage exceeds the sensed output voltage at the FB pin, the part starts to work normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1 and C2 (Figure 3). If (V_{IN}-V_{SW}) exceeds 3.3V, U2 will regulate M1 to maintain a 3.3V BST voltage across C3.

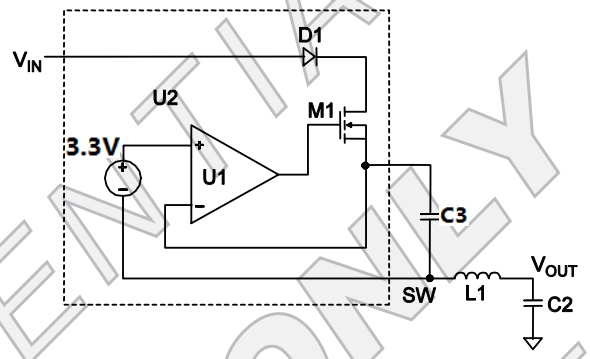


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONINFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-100kΩ for R2. Typically, set the current through R2 between 5-30uA will make a good balance between system stability and also the no load loss. Then R1 is determined as follow:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

The feedback circuit is shown as Figure 4.

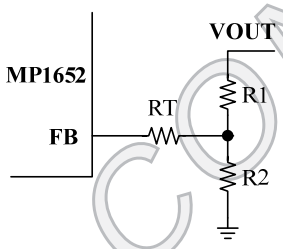


Figure 4: Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (8)

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)
3.3	40.2	13	4.7

8) For detail design circuit, please refer to the TYPICAL APPLICATION CIRCUIT in figure 6 page 15.

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is

an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (12)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

PC Board Layout

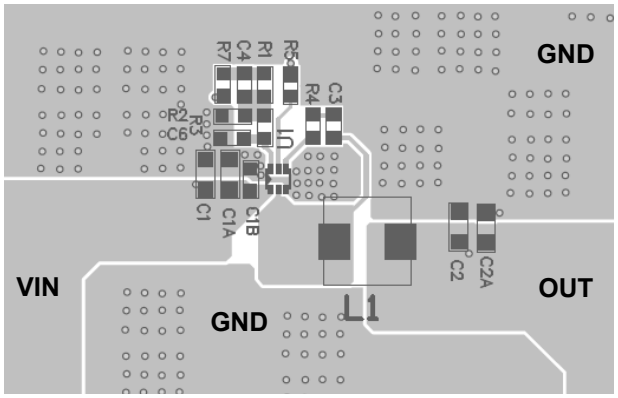
Proper layout of the switching power supplies is very important, and sometimes critical for proper function. Poor layout design can result in poor line or load regulation and stability issues. Please follow these guidelines and take Figure 5 as reference:

1）The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.

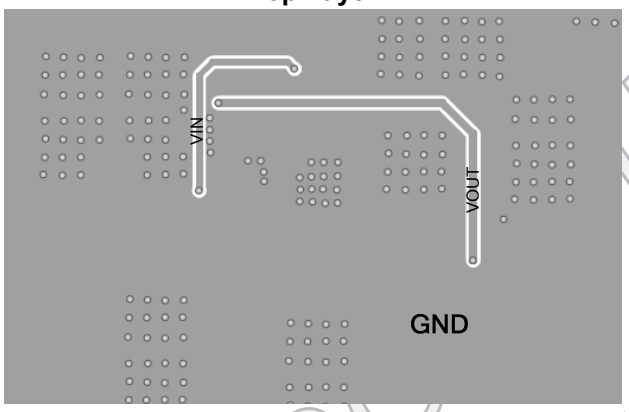
2）The input capacitor needs to be as close as possible to the VIN and GND pins. Recommend within 1mm.

3）The external feedback resistors should be placed next to the FB pin.

4）Keep the switching node SW short and away from the feedback network.



Top Layer



Bottom Layer

Figure 5: Sample Board Layout

Design Example

A design example is provided below when the ceramic capacitors are applied:

V_{IN}	12V
V_{OUT}	3.3 V
I_{OUT}	2A

The detailed application schematic is showed in Figure 6. The typical performance and waveforms have been showed in the Typical Performance Characteristics Section. For more devices applications, please refer to the related Evaluation Board Datasheet.

TYPICAL APPLICATION CIRCUITS

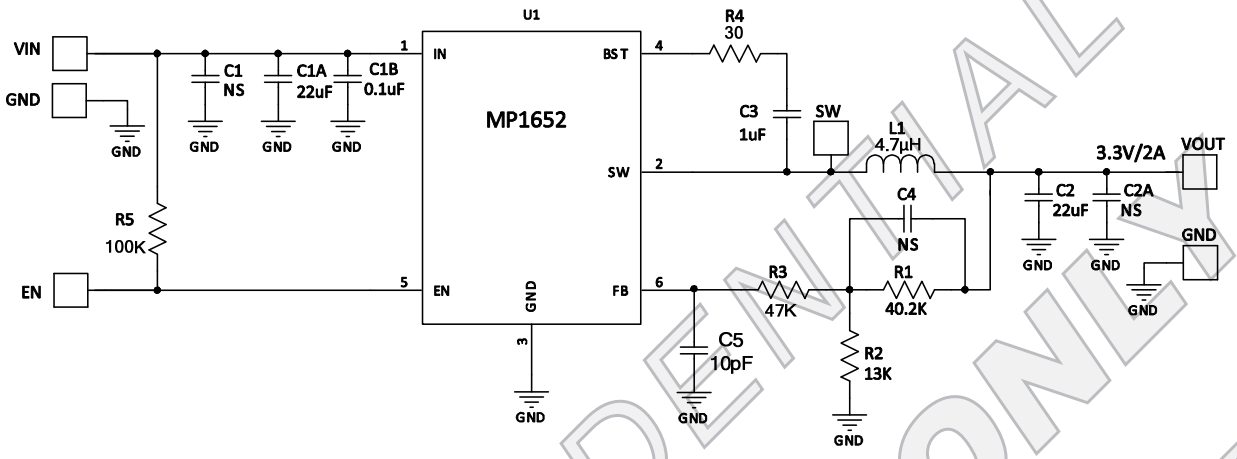
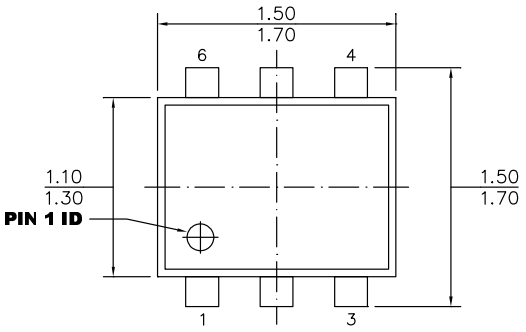


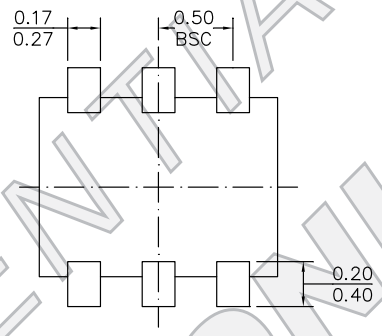
Figure 6: 12Vin, 3.3V/2A output

PACKAGE INFORMATION

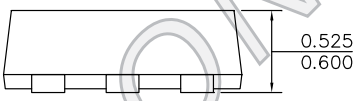
SOT563



TOP VIEW

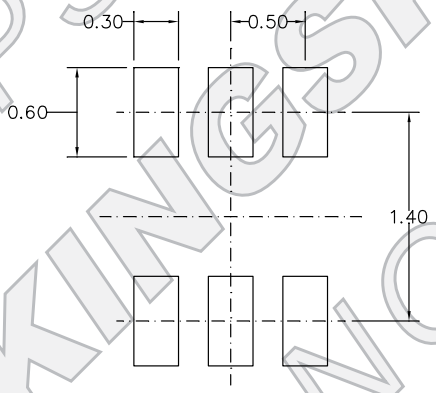


BOTTOM VIEW



FRONT VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.