MP2702

1-Cell to 2-Cell, 26V Input, 1A Linear Charger with EN Control and Configurable JEITA

DESCRIPTION

The MP2702 is a linear charger for 1-cell to 2-cell Li-ion, Li-polymer, and LiFePO4, and 2-cell to 6-cell NiMH batteries. The device can sustain a voltage up to 26V.

The MP2702 measures the battery voltage (V_{BATT}) and automatically charges the battery in four phases: trickle charge, pre-charge, constant-current (CC) fast charge, and constant-voltage charge.

The MP2702 provides a dedicated ISET pin to set the charge current by connecting a resistor between ISET and ground. The device also provides a USBM pin to set the input current limit (I_{IN_LIM}) prior to setting the charge current. If the input power is overloaded, the MP2702 has a minimum input voltage limit (V_{IN_LIM}) to reduce battery current.

The MP2702 has robust protection features including input and battery over-voltage protection (OVP), a charge safety timer, and battery temperature protection compliant with the JEITA standard.

The MP2702 provides a dedicated $\overline{EN}$ pin to enable or disable charging. Once charging is disabled, the quiescent current (I_Q) flowing into either the IN or BATT pin is minimized.

In addition, the MP2702 provides two open-drain pins to indicate the input power status and charge status. The $\overline{ACOK}$ pin indicates whether the input power is present. The $\overline{CHG}$ pin indicates several states of charging, including charging, termination, and fault events.

The MP2702 also offers flexible one-time programmable (OTP) memory to configure a variety of charge parameters.

The MP2702 is available in a QFN-10 (2mmx2.5mm) package.

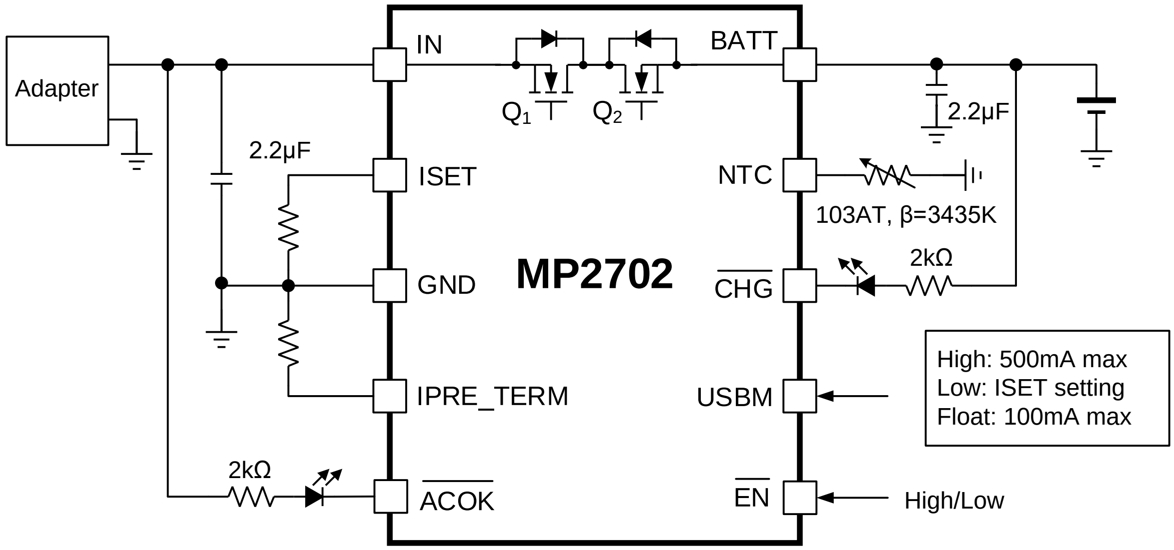
FEATURES

- Up to 26V of Sustainable Voltage
- Up to 1A of Charge Current Configurable via the ISET Pin
- ISET Pin Short-Circuit Protection (SCP)
- Additional Input Current Limit (I_{IN_LIM}) Setting via the USBM Pin
- Configurable Pre-Charge Current (I_{PRE})
- Configurable Termination Current (I_{TERM}) Threshold
- One-Time Programmable (OTP) Memory Selection for Three Levels of the Minimum Input Voltage Limit (V_{IN_LIM})
- OTP Selection for Battery-Full Voltage from 2.4V to 4.5V Per Cell
- 0.5% Battery Regulation Voltage Accuracy
- OTP Selection for 1-Cell or 2-Cell Battery
- Integrated Chip Junction Temperature (T_J) Regulation
- Battery Temperature Protection Compliant with JEITA Standard
- $\overline{EN}$ Pin to Enable the Whole Chip
- 100nA Battery Leakage Current in Shutdown Mode
- Down to 3mA I_{TERM}
- Charge Status and Fault Indication
- Input Power Indication
- Integrated Charge Safety Timer
- OTP for Miscellaneous Parameters
- Provides Option for Charging 2-Cell to 6-Cell NiMH Battery
- Compatible with LiFePO4 Battery
- Available in a Compact QFN-10 (2mmx2.5mm) Package

APPLICATIONS

- Headphones
- Wearable Devices
- Emergency Calls

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2702GRP-xxxx**	QFN-10 (2mmx2.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2702GRP-xxxx-Z).

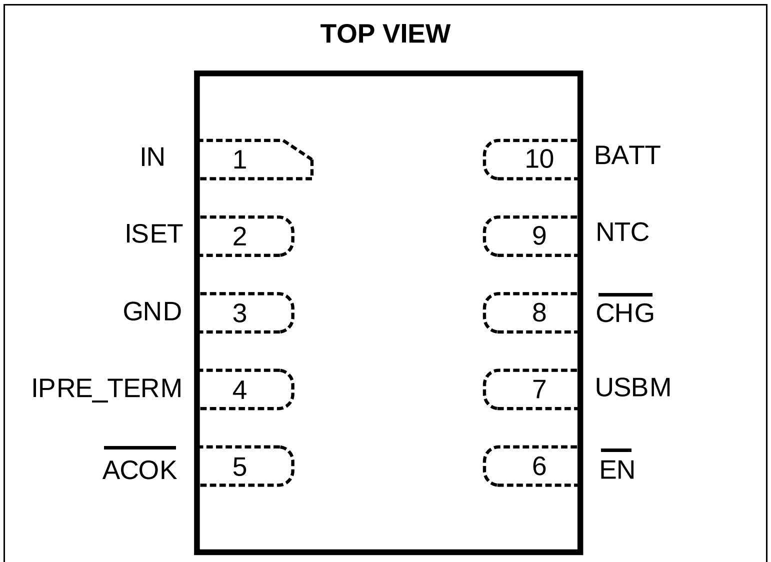
**"xxxx" is the register setting option. The factory default is "0000". This content can be viewed in the OTP register map. Please contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

LCY
LLL

LC: Product code of MP2702GRP-xxxx
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-10 (2mmx2.5mm)

PIN FUNCTIONS

Pin #	Name	Type (1)	Description
1	IN	P	**Power input of the IC.** Place a 1µF to 10µF bypass capacitor between the IN and GND pins.
2	ISET	AI	**Charge current setting.** Connect a resistor between the ISET and GND pins to set the fast charge current, which should range between 20mA and 1A.
3	GND	P	**Ground terminal.**
4	IPRE_TERM	AI	**Pre-charge and termination current setting.** Connect a resistor between the IPRE_TERM and GND pins to set the pre-charge current (I_{PRE}) and termination current (I_{TERM}).
5	$\overline{\text{ACOK}}$	DO	**Input power status indication.** The $\overline{\text{ACOK}}$ pin is an open-drain output. If the input voltage (V_{IN}) exceeds its under-voltage lockout (UVLO) threshold (V_{IN_UVLO}) and the battery voltage (V_{BATT}), then $\overline{\text{ACOK}}$ is pulled low.
6	$\overline{\text{EN}}$	DI	**Chip enable control.** The $\overline{\text{EN}}$ pin is active low. When $\overline{\text{EN}}$ is floated, the chip is enabled by default. When the chip is disabled, all blocks including the ACOK indicator do not work.
7	USBM	DI	**Input current limit setting.** The USBM pin configures the input current limit (I_{IN_LIM}) for USB or adapter sources, where high = 500mA max, low = ISET setting, and floating = 100mA max. Do not pull USBM above 3.6V.
8	$\overline{\text{CHG}}$	DO	**Charge status indication.** If the $\overline{\text{CHG}}$ pin is pulled low, this indicates charging. If $\overline{\text{CHG}}$ is open drain, this indicates either no charging or charge complete.
9	NTC	AI	**Temperature-sense input.** Connect a negative temperature coefficient (NTC) thermistor between the NTC and GND pins. Pull the NTC pin to ground to disable charging.
10	BATT	P	**Battery terminal.** Place a 1µF to 10µF bypass capacitor between the BATT and GND pins.

Note:

1) AI refers to analog input, DI refers to digital input, DO refers to digital output, and P refers to power.

ABSOLUTE MAXIMUM RATINGS (2)

IN, $\overline{ACOK}$, $\overline{CHG}$ to GND ....-0.3V to +26V
BATT to GND...............................- 0.3V to +26V
All other pins to GND ....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (3)...... .... 1.78W
Junction temperature (T_J) ....150°C
Lead temperature (solder) ....260°C
Storage temperature…. .... -65°C to +150°C

ESD Ratings

Human body model (HBM) (4).................... 1.5kV
Charged-device model (CDM) (5) 750V

Recommended Operating Conditions (6)

Supply voltage (V_{IN}) ....Up to 13.5V
Input current (I_{IN}) ....Up to 1A
Constant-current fast charge current (I_{CC}) .... ……………………………………………Up to 1A
Battery voltage (V_{BATT}) ....Up to 9V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (7)

Thermal Resistance (7)	θ_{JA}	θ_{JC}	
QFN-10 (2mmx2.5mm)...........	88	13...	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per ANSI/ESDA/JEDEC JS-001, all pins.
5) Per ANSI/ESDA/JEDEC JS-002, all pins.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.4	3.6	3.8	V
Input UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$	V_{IN} rising		340		mV
Input voltage (V_{IN}) vs. battery voltage (V_{BATT}) headroom threshold	V_{HDRM}	V_{IN} rising, 1 cell		200		mV
		V_{IN} rising, 2 cells		240		mV
		V_{IN} falling, 1 cell	10	100	190	mV
		V_{IN} falling, 2 cells	20	130	240	mV
Input power good (PG) rising deglitch time	t_{VIN_GD}	V_{IN} rising		30		ms
Input over-voltage protection (OVP) threshold	V_{IN_OVP}	V_{IN} rising, 1 cell	5.8	6	6.2	V
		V_{IN} rising, 2 cells	13.8	14.4	15	V
Input OVP hysteresis	$V_{IN\_OVP\_HYS}$	V_{IN} falling, 1 cell		220		mV
		V_{IN} falling, 2 cells		550		mV
Input OVP deglitch time	t_{VIN_OVP}	V_{IN} rising		100		µs
Input OVP recovery deglitch time		V_{IN} falling		30		ms
Input shutdown current	I_{IN_Q}	V_{IN} = 5V, part is disabled via $\overline{EN}$		1	3.8	µA
		V_{IN} = 5V, charge is disabled by pulling NTC to GND		260	350	µA
		V_{IN} = 5V, charge termination		460	550	µA
BATT leakage current in shutdown mode	I_{BATT_SHDN}	V_{BATT} = 4.2V (1 cell) or 8.4V (2 cells), V_{IN} = GND		0.1	1	µA
Battery quiescent current after termination	I_{BATT_Q}	V_{IN} = 5V, 1 cell, charge terminated		3.8	5	µA
		V_{IN} = 9V, 2 cells, charge terminated		5.6	7.2	µA
Battery Charger (T_A = 0°C to 70°C)						
IN to BATT on resistance	R_{ON_Q1+Q2}			370		mΩ
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	0.9	1	1.1	V/cell
Trickle charge to pre-charge threshold hysteresis	$V_{BATT\_TC\_HYS}$	V_{BATT} falling		100		mV/cell
Trickle charge current	I_{TC}	R_{ISET} = 550Ω	28	50	72	mA
		Minimum clamp	1	3	5.5	mA
Pre-charge to fast charge threshold	V_{BATT_PRE}	VBATT_PRE = 2.5V/cell	2.4	2.5	2.6	V/cell
		VBATT_PRE = 2.8V/cell	2.7	2.8	2.9	
		VBATT_PRE = 3V/cell	2.9	3	3.1	
		VBATT_PRE = 3.2V/cell	3.1	3.2	3.3	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pre-charge to fast charge deglitch time	t_{PRE_CC}			30		ms
Fast charge to pre-charge deglitch time	t_{CC_PRE}			30		ms
Pre-charge current	I_{PRE}	Float IPRE_TERM, R_{ISET} = 1.1kΩ	88	100	112	mA
		Float IPRE_TERM, R_{ISET} = 550Ω	160	200	240	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 1.1kΩ	75	100	125	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 550Ω	145	202	258	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 1.1kΩ	32	50	66	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 550Ω	70	100	130	mA
		Minimum clamp	1	3	5.5	mA
Constant-current fast charge current	I_{CC}	R_{ISET} = 786Ω	665	700	735	mA
		R_{ISET} = 11kΩ	45	50	55	mA
		R_{ISET} = 27.5kΩ	15	20	25	mA
Over-charge (OC) current protection	I_{OC}	R_{ISET} = 0Ω		1.25		A
Battery charge regulation voltage	V_{BATT_REG}	VBATT_REG = 3.6V/cell	3.582	3.6	3.618	V/cell
		VBATT_REG = 4.1V/cell	4.080	4.1	4.121	
		VBATT_REG = 4.2V/cell	4.179	4.2	4.221	
		VBATT_REG = 4.35V/cell	4.328	4.35	4.372	
		VBATT_REG = 4.5V/cell	4.478	4.5	4.523	
Battery charge termination threshold	I_{TERM}	R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 1.1kΩ	38	50	62	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 550Ω	74	100	126	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 1.1kΩ	12	22	31	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 550Ω	32	48	64	mA
		Minimum clamp	1	3	5.5	mA
Charge termination deglitch time	t_{TERM_DGL}			30		ms
Automatic recharge voltage threshold	V_{RECH}	Below V_{BATT_REG}	135	200	265	mV/cell
Automatic recharge voltage deglitch time	t_{RECH_DGL}			30		ms
Battery OVP threshold	V_{BATT_OVP}	Compared to V_{BATT_REG} and V_{BATT} rising	85	150	215	mV/cell
Battery OVP threshold hysteresis	$V_{BATT\_OVP\_HYS}$	Compared to V_{BATT_OVP} and V_{BATT} falling		30		mV/cell
Input Voltage and Input Current Regulation (T_A = 0ºC to 70ºC)						
Input current limit	I_{IN_LIM}	Float USBM	80	90	100	mA
		USBM = high	405	450	500	
Minimum V_{IN} limit	V_{IN_LIM}	VIN_LIM = 4.375V/cell	4.25	4.37	4.49	V/cell
		VIN_LIM = 4.5V/cell	4.37	4.5	4.6	
		VIN_LIM = 4.75V/cell	4.63	4.75	4.87	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown rising threshold (8)	T_{J_SHDN}	T_J rising		160		°C
Thermal shutdown hysteresis (8)	$T_{J\_SHDN\_HYS}$			20		°C
Thermal regulation (8)	T_{J_REG}			120		°C
Battery Temperature Monitoring and Protection						
Negative temperature coefficient (NTC) bias current	I_{NTC}		47.5	50	52	µA
Cold temperature threshold	V_{COLD}	V_{NTC} = 1V to 1.5V, VCOLD = 0°C	1363	1377	1391	mV
Cold temperature threshold hysteresis	V_{COLD_HYS}	V_{NTC} = 1.5V to 1V, VCOLD = 0°C		90		mV
Cool temperature threshold	V_{COOL}	V_{NTC} = 0.5V to 1V, VCOOL = 10°C	893	902	915	mV
Cool temperature threshold hysteresis	V_{COOL_HYS}	V_{NTC} = 1V to 0.5V, VCOOL = 10°C		34		mV
Warm temperature threshold	V_{WARM}	V_{NTC} = 0.5V to 0.2V, VWARM = 45°C	239	245	251	mV
Warm temperature threshold hysteresis	V_{WARM_HYS}	V_{NTC} = 0.2V to 0.5V, VWARM = 45°C		11		mV
Hot temperature threshold	V_{HOT}	V_{NTC} = 0.2 to 0.1V, VHOT = 60°C	138	151	157	mV
Hot temperature threshold hysteresis	V_{HOT_HYS}	V_{NTC} = 0.1 to 0.2V, VHOT = 60°C		11		mV
NTC enable charge threshold		V_{NTC} = 0V to 0.15V	75	90	105	mV
NTC enable charge threshold hysteresis		V_{NTC} = 0.15V to 0V		15		mV
NTC bias current when the charge is disabled via the NTC pin		V_{NTC} = 0V	20	30	40	µA
NTC charge termination disable threshold		V_{NTC} rising	2.4	2.5	2.6	V
NTC charge termination disable threshold hysteresis		V_{NTC} falling		100		mV
NTC minimum bias current when NTC is floated	I_{NTC_FLT}	V_{NTC} = 3V	3	4.5	6	µA
Floated NTC voltage	V_{NTC_FLT}			3.6		V

Note:

8) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40°C to +125°C, unless otherwise noted.

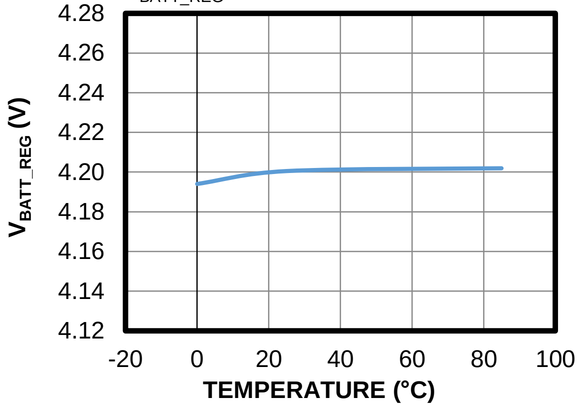
Parameter	Symbol	Condition	Min	Typ	Max	Units
Open-Drain Pin Characteristics						
$\overline{CHG}$ pin output voltage		I_{SINK} = 5mA			0.4	V
$\overline{ACOK}$ pin output voltage		I_{SINK} = 5mA			0.4	V
Logic Levels on the USBM and $\overline{EN}$ Pins						
Logic low input voltage	V_{IL}				0.4	V
Logic high input voltage	V_{IH}		1.4			
Floated USBM voltage	V_{FLT}		700	900	1100	mV
Timing Characteristics (T_A = 0ºC to 70ºC)						
Charge timer	t_{TMR}	t_{MR_SET} = 10hr	8	10	12	hr
Trickle charge and pre-charge timer			0.8	1	1.2	hr

TYPICAL CHARACTERISTICS

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

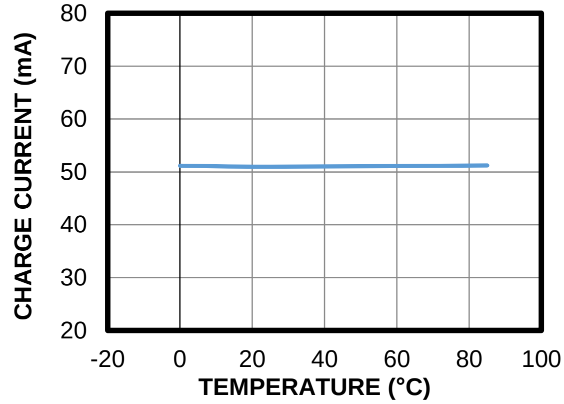
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.2V, 1 cell



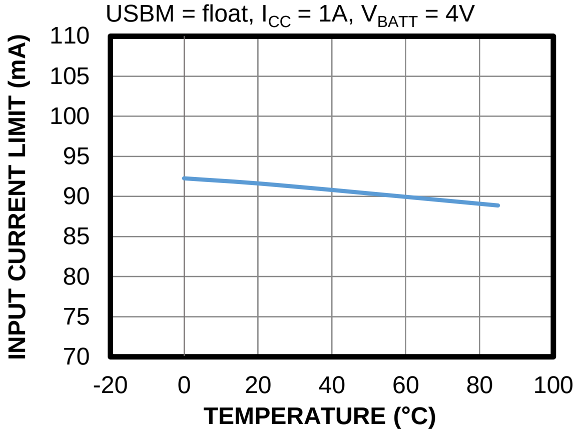
Charge Current vs. Temperature

I_{CC} = 50mA, V_{IN} = 5V, V_{BATT} = 3.8V



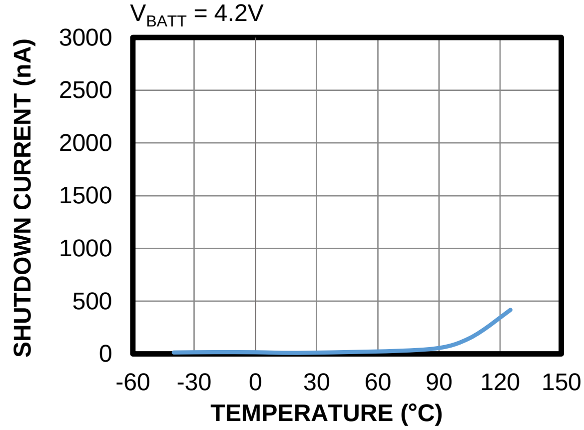
Input Current Limit vs. Temperature

USBM = float, I_{CC} = 1A, V_{BATT} = 4V



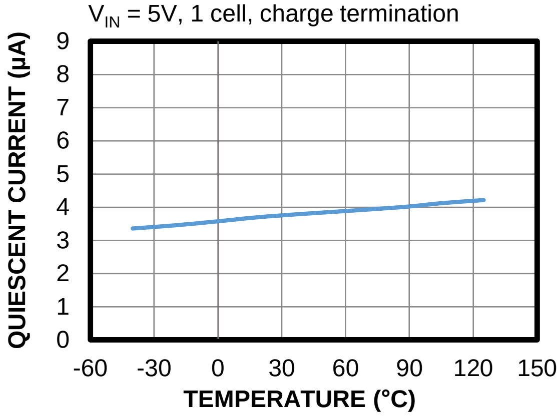
Battery Shutdown Current vs. Temperature

V_{BATT} = 4.2V



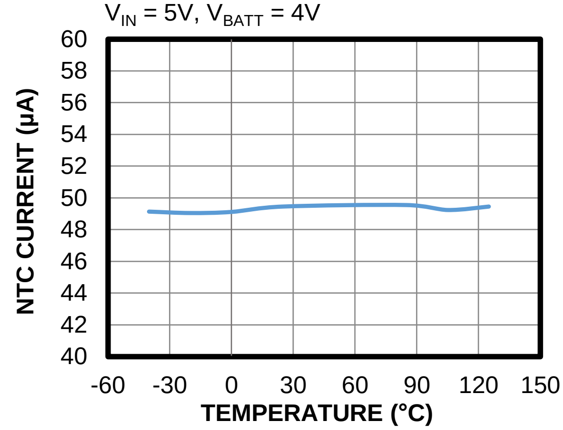
Battery Quiescent Current vs. Temperature

V_{IN} = 5V, 1 cell, charge termination



NTC Current vs. Temperature

V_{IN} = 5V, V_{BATT} = 4V

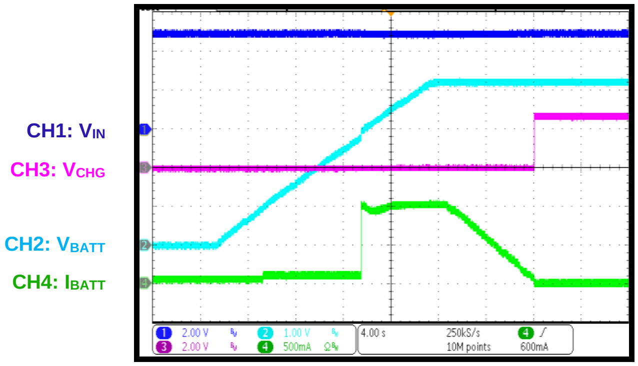


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

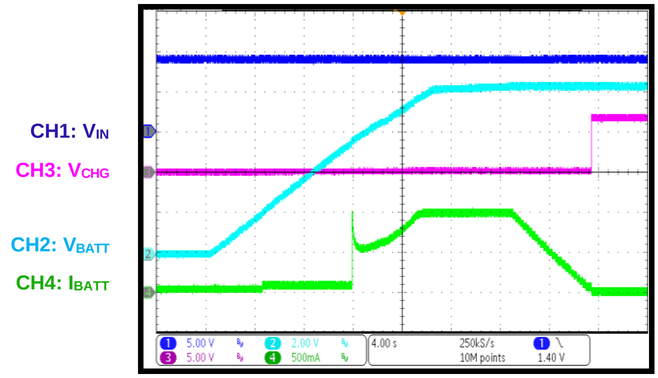
Battery Charge Profile

V_{IN} = 5V, I_{PRE} = 10%, I_{CC} = 1A, 1 cell



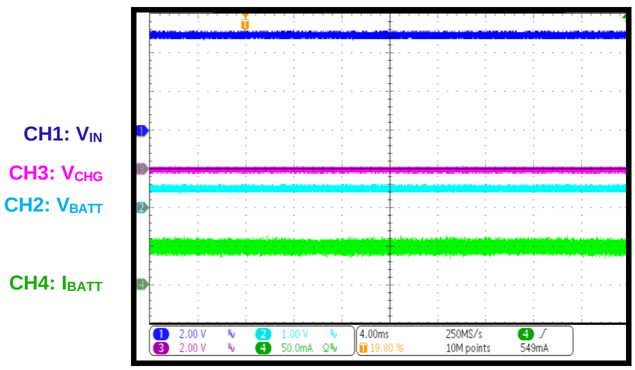
Battery Charge Profile

V_{IN} = 9V, I_{PRE} = 10%, I_{CC} = 1A, 2 cells



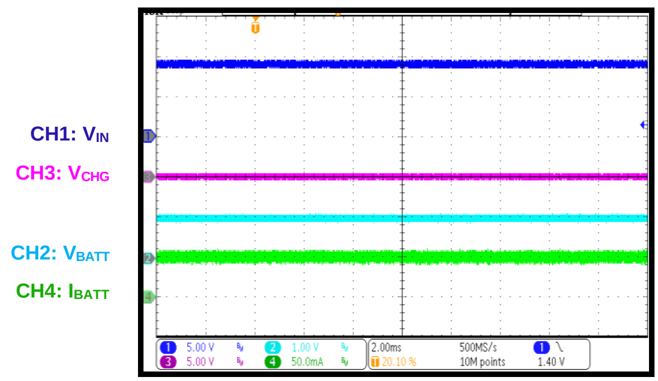
Trickle Charge

V_{IN} = 5V, V_{BATT} = 0.5V, I_{TC} = 50mA, 1 cell



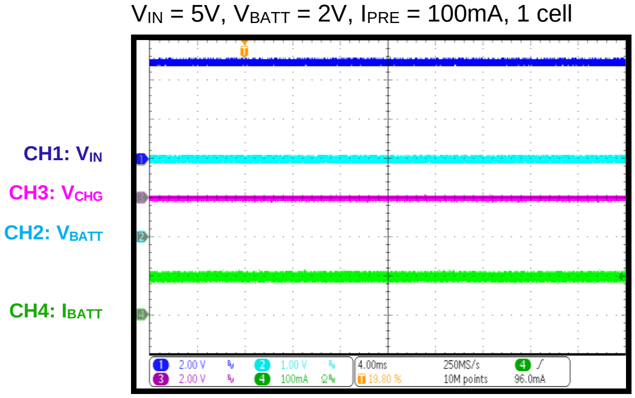
Trickle Charge

V_{IN} = 9V, V_{BATT} = 1V, I_{TC} = 50mA, 2 cells



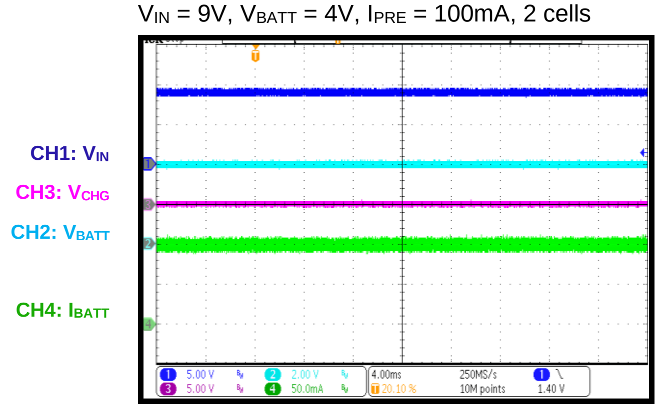
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2V, I_{PRE} = 100mA, 1 cell



Pre-Charge

V_{IN} = 9V, V_{BATT} = 4V, I_{PRE} = 100mA, 2 cells

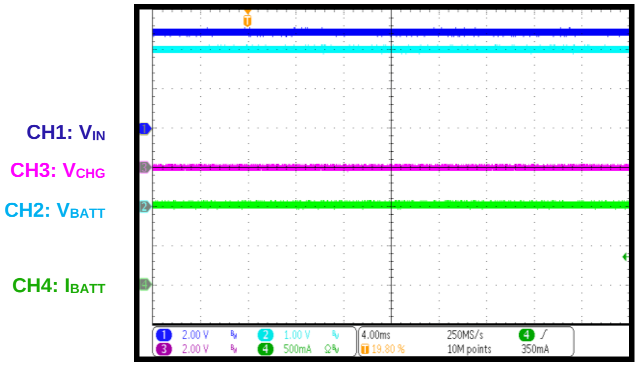


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

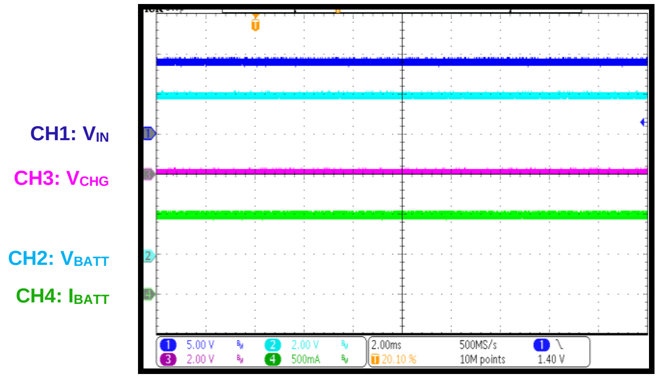
Constant Current Charge

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



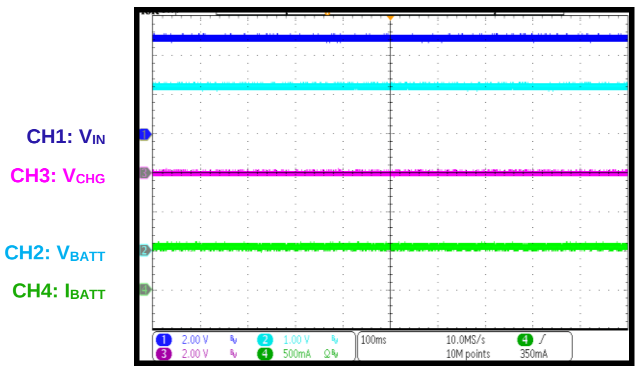
Constant Current Charge

V_{IN} = 9V, V_{BATT} = 8V, I_{CC} = 1A, 2 cells



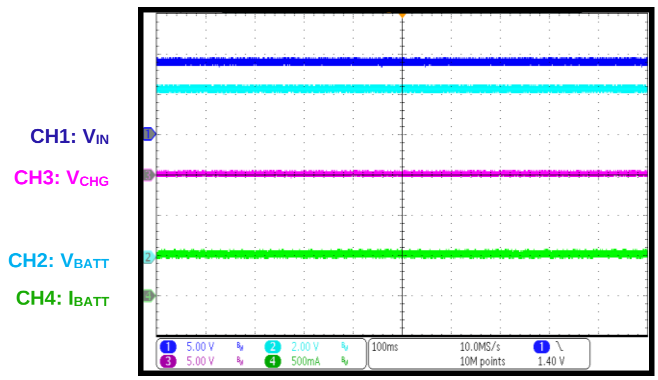
Constant-Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.185V, I_{CC} = 1A, 1 cell



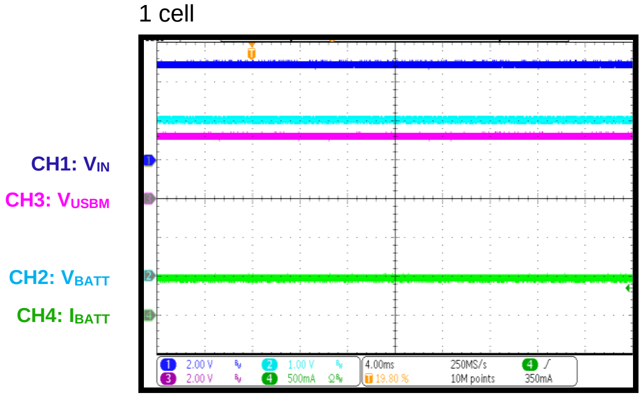
Constant-Voltage Charge

V_{IN} = 9V, V_{BATT} = 8.389V, I_{CC} = 1A, 2 cells



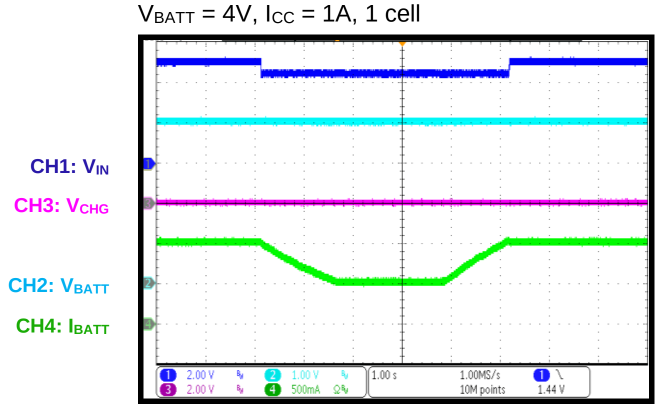
Input Current Limit

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, USBM = high, 1 cell



Input Voltage Limit

V_{IN} = 5V (1A >> 0.5A >> 1A), V_{IN_LIM} = 4.5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



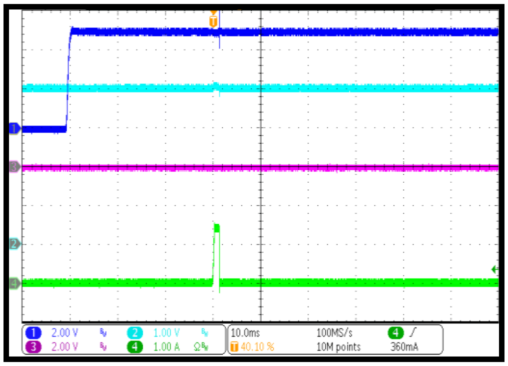
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

Start-Up with ISET Short

V_{IN} = 5V, V_{BATT} = 4V, ISET short, 1 cell

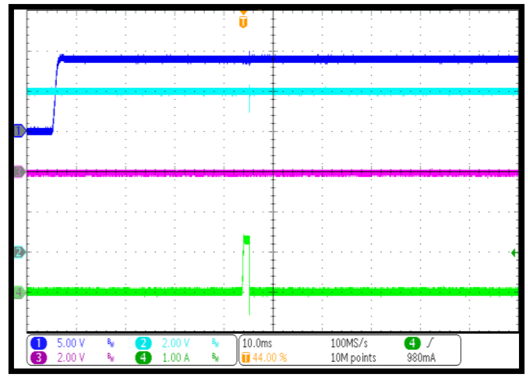
CH1: V_{IN}
CH3: V_{ISET}
CH2: V_{BATT}
CH4: I_{BATT}



Start-Up with ISET Short

V_{IN} = 9V, V_{BATT} = 8V, ISET short, 2 cells

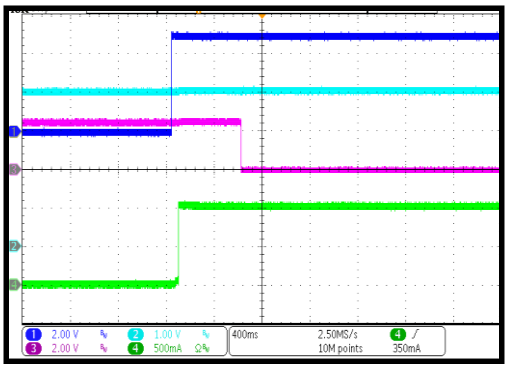
CH1: V_{IN}
CH3: V_{ISET}
CH2: V_{BATT}
CH4: I_{BATT}



Start-Up

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell

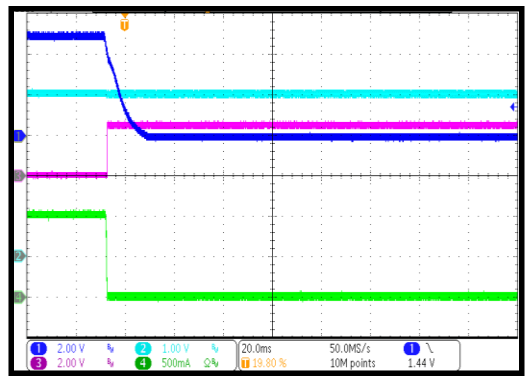
CH1: V_{IN}
CH3: V_{CHG}
CH2: V_{BATT}
CH4: I_{BATT}



Shutdown

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell

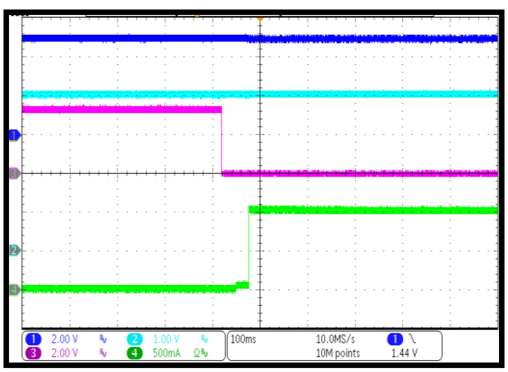
CH1: V_{IN}
CH3: V_{CHG}
CH2: V_{BATT}
CH4: I_{BATT}



Charge Enable via EN

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell

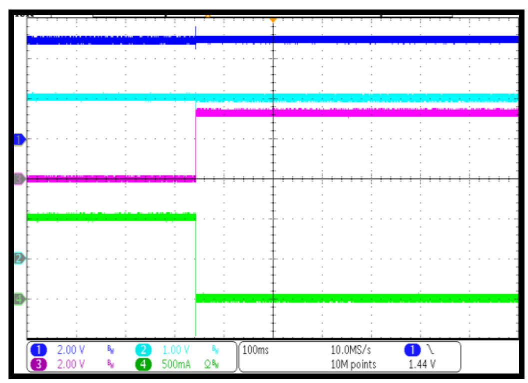
CH1: V_{IN}
CH3: V_{EN}
CH2: V_{BATT}
CH4: I_{BATT}



Charge Disable via EN

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell

CH1: V_{IN}
CH3: V_{EN}
CH2: V_{BATT}
CH4: I_{BATT}



FUNCTIONAL BLOCK DIAGRAM

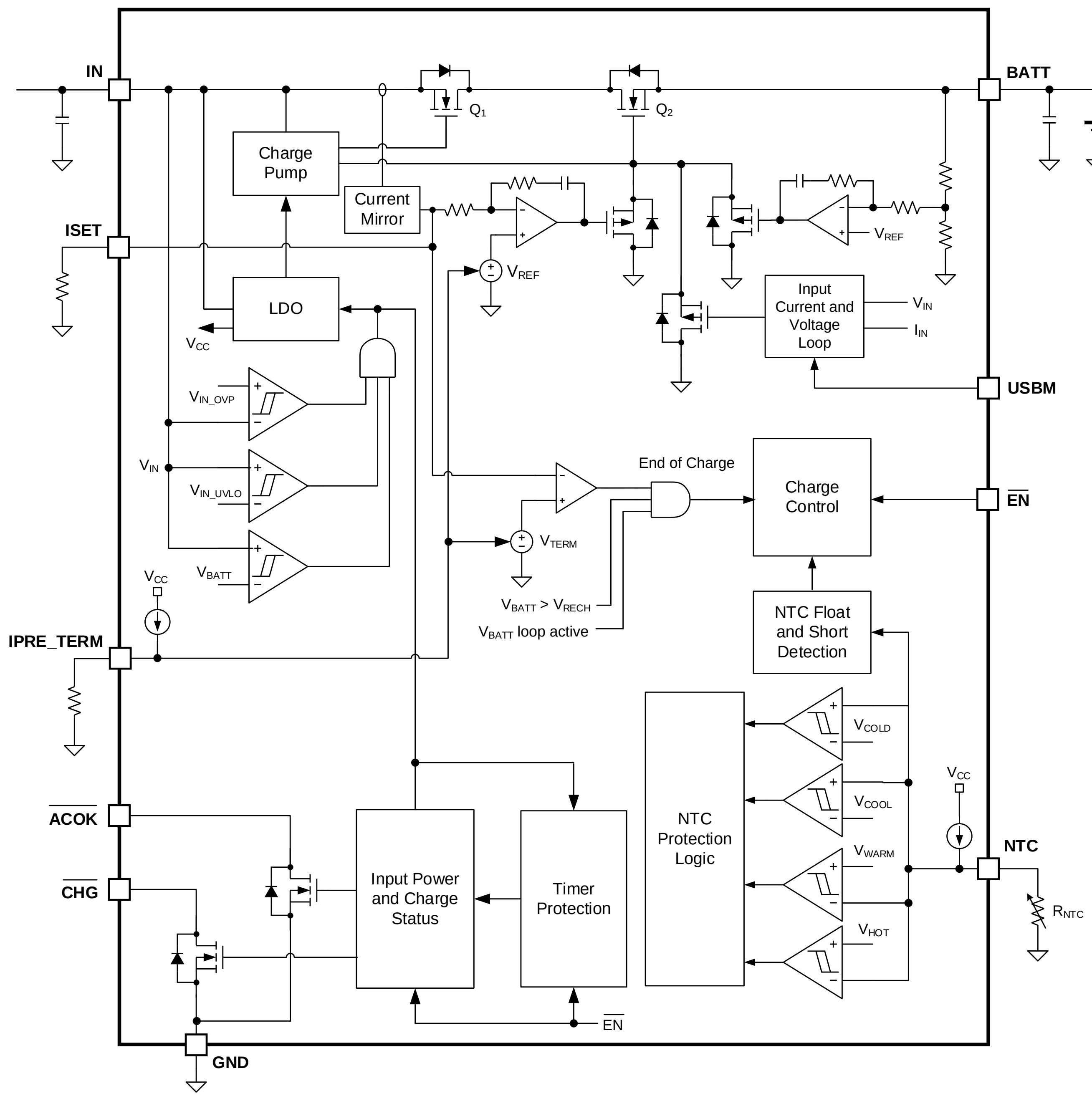


Figure 1: Functional Block Diagram

OPERATION

Introduction

The MP2702 is a linear charger for 1-cell to 2-cell Li-ion, Li-polymer, and LiFePO4 battery applications, and 2-cell to 6-cell NiMH battery applications. The device can sustain an input voltage (V_{IN}) up to 26V and achieve up to 1A of charge current.

Power Supply

The IC is powered by the input. Once V_{IN} exceeds its under-voltage lockout threshold (V_{IN_UVLO}), the internal control and logic circuit starts to operate. If V_{IN} exceeds both V_{IN_UVLO} and the sum of the battery voltage (V_{BATT}) and the V_{IN} vs. V_{BATT} headroom threshold (V_{HDRM}) (V_{BATT} + V_{HDRM}), the IC indicates power good (PG), and the $\overline{ACOK}$ pin is pulled down to GND.

Charge Cycle

When the input power is qualified as a good power supply, the IC checks V_{BATT} and provides four charging phases: trickle charge, pre-charge, constant-current fast charge, and constant-voltage charge (see Figure 2).

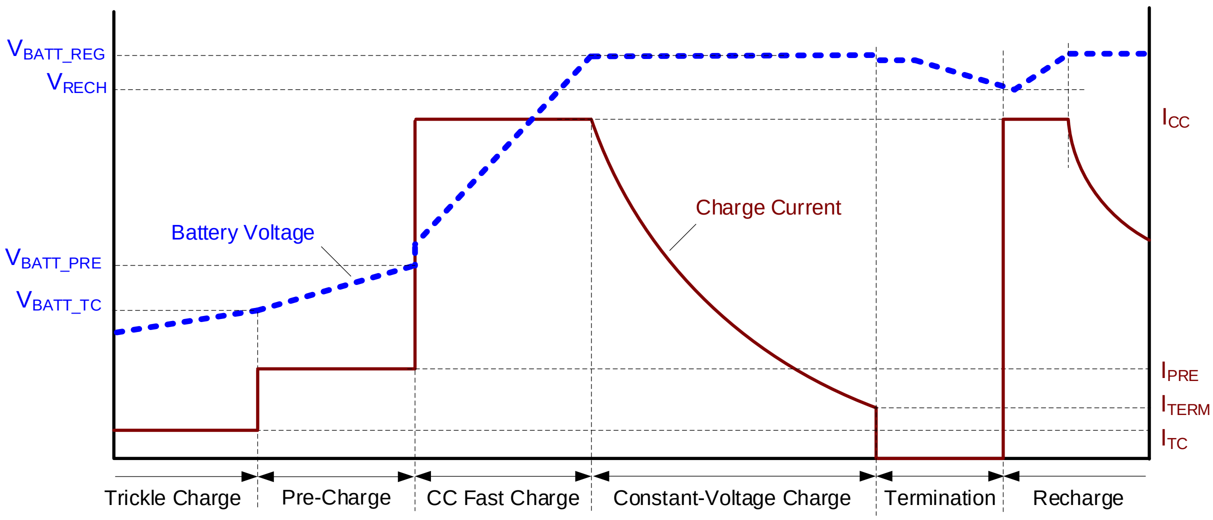


Figure 2: Charge Cycle Profile

Phase 1 (Trickle Charge)

If V_{BATT} is below the trickle charge to pre-charge threshold (V_{BATT_TC}), a trickle charging current is applied on the battery to reset the protection circuit in the battery pack. The trickle charge current (I_{TC}) is 5% of the set fast charge current. Once the constant-current fast charge current (I_{CC}) x 5% is below 3mA, I_{TC} is clamped at 3mA.

Phase 2 (Pre-Charge)

If V_{BATT} exceeds V_{BATT_TC} but remains below the pre-charge to fast charge threshold (V_{BATT_PRE}), the IC charges the battery with the pre-charge current (I_{PRE}). There are four one-time programmable (OTP) memory options available for V_{BATT_PRE}.

I_{PRE} is proportional to the fast charge current and can be configured via the IPRE_TERM pin.

Phase 3 (Constant-Current Fast Charge)

If V_{BATT} exceeds V_{BATT_PRE}, the IC enters constant-current fast charge phase. I_{CC} can be set via the ISET pin.

Phase 4 (Constant-Voltage Charge)

If V_{BATT} rises to the battery charge regulation voltage (V_{BATT_REG}), the charge current starts to decrease. Once the charge current reaches the battery charge termination threshold (I_{TERM}), the charge cycle is considered complete after the charge termination deglitch time (t_{TERM_DGL}). If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle stops and the corresponding timeout fault signal asserts.

Charge Termination

If V_{BATT} reaches the full voltage regulation threshold and the charge current is below I_{TERM}, charging is terminated after a deglitch time of 30ms. The charge termination can be disabled by floating the NTC pin.

Automatic Recharge

Once the battery charge cycle completes, the IC remains off. During this time, the external load consumes battery power or the battery self-discharges. A new charge cycle automatically begins once V_{BATT} drops below the automatic recharge threshold for the 30ms deglitch time. The safety charge timer resets when the automatic recharge cycle begins.

Input Current Limit

The MP2702 provides an USBM pin to set the input current limit (I_{IN_LIM}), which has higher priority than configuring the ISET pin. Table 1 shows the I_{IN_LIM} setting. If the charge current exceeds I_{IN_LIM} when USBM is floated or set high, the charge current is limited by I_{IN_LIM}. The logic high voltage at USBM must be below 3.6V.

Table 1: I_{IN_LIM} Setting

USBM Level	I_{IN}
High	500mA max
Low	Depending on ISET setting
Float	100mA max

Minimum Input Voltage Limit

The MP2702 includes a minimum input voltage limit (V_{IN_LIM}) regulation loop. If the charge current or I_{IN_LIM} exceeds the input power supply current rating, the MP2702 automatically reduces the charge current once V_{IN} reaches V_{IN_LIM}. There are three options for setting V_{IN_LIM}. See the One-Time Programmable (OTP) Memory Map section on page 21.

Cell Selection

The MP2702 can support 1-cell and 2-cell batteries. The battery cell counts can be set via the OTP. See the One-Time Programmable (OTP) Memory Map section on page 21.

For 2-cell applications, battery hot insertion or short is not allowed when V_{IN} is present and charge is enabled.

Battery Regulation Voltage

The MP2702 can support a variety of battery-full voltages ranging between 2.4V/cell to 4.5V/cell with a 50mV step, which are set via the OTP.

Setting the Fast Charge Current

An external resistor connected between the ISET and GND pins configures the fast charge current.

The relationship between I_{CC} and the ISET resistor (R_{ISET}) can be calculated with Equation (1):

$$V_{REF} = k \times I_{CC} \times R_{ISET} \quad (1)$$

Where k is the sense gain of the current mirror.

I_{CC} can be calculated with Equation (2):

$$I_{CC} = \frac{V_{REF} / k}{R_{ISET}} \quad (2)$$

Where the reference voltage (V_{REF}) is 1.2V, and the k factor is 2.18 x 10^{-3}.

Figure 3 shows the functional diagram for setting I_{CC} via ISET.

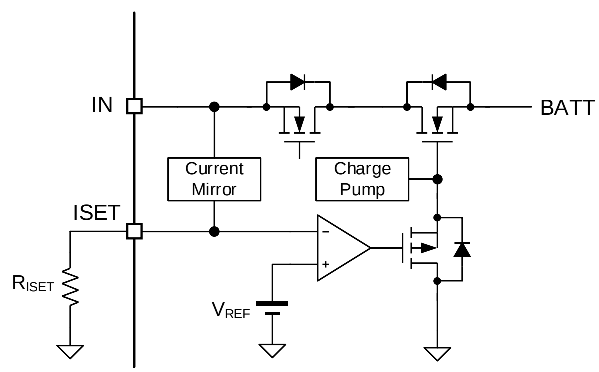


Figure 3: Functional Diagram of Setting I_{CC} via the ISET Pin

The actual fast charge current is the lower value between I_{IN_LIM} and I_{CC}. Table 2 on page 17 shows an example of the actual fast charge current at different ISET and USBM settings.

Table 2: Example of Real Fast Charge Current at Different ISET and USBM Settings

I_{CC}	USBM = High	USBM = Float	USBM = Low
80mA	80mA typical	80mA typical/ 100mA max	80mA typical
300mA	300mA typical	100mA max	300mA typical
600mA	500mA max	100mA max	600mA typical

Over-Current Protection (OCP)

If the charge current is set too high erroneously, the MP2702 provides over-current protection (OCP). For example, if ISET is shorted to GND, the charge current is clamped at 1.25A, and the part latches off after a deglitch time of 1ms. This fault can be reset by re-plugging V_{IN}, pulling NTC to GND, or toggling the $\overline{EN}$ pin.

Setting the Pre-Charge Current

Connect a resistor between the IPRE_TERM and GND pins to configure the proportion of I_{PRE} to I_{CC}.

Figure 4 shows the functional diagram for setting I_{PRE}.

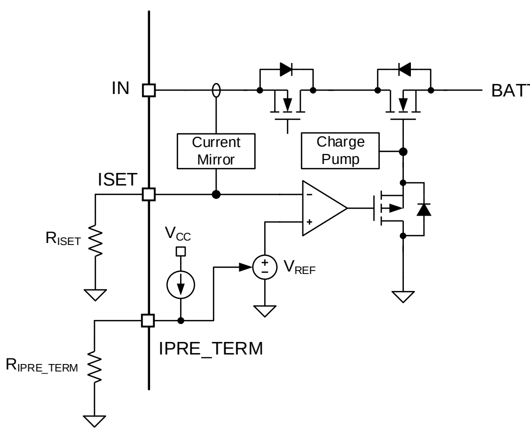


Figure 4: Functional Diagram for Setting I_{PRE}

The ratio of I_{PRE} to I_{CC} can be calculated with Equation (3):

$$I_{PRE} / I_{CC} = R_{IPRE\_TERM} / K_{PRE-CC} \quad (3)$$

Where K_{PRE-CC} is 112.36Ω/%.

For example, to set the proportion of I_{PRE} / I_{CC} to 10%, connect a 1.13kΩ resistor between the IPRE_TERM pin and ground.

When IPRE_TERM pin is floated, I_{PRE} is fixed at 20% of the I_{CC} setting.

Setting the Charge Termination Threshold

If V_{BATT} reaches the full voltage, the battery voltage loop is initiated and the charge current declines. Once the three conditions below are satisfied, charging terminates:

1. The V_{BATT} loop is active.
2. V_{BATT} exceeds the automatic recharge voltage threshold (V_{RECH}).
3. The battery current (I_{BATT}) is below I_{TERM}.

I_{TERM} is also proportional to I_{CC}. This threshold (I_{TERM} / I_{CC}) can be configured via the resistor placed between IPRE_TERM and ground, and can be calculated with Equation (4):

$$I_{TERM} / I_{CC} = R_{IPRE\_TERM} / K_{TERM-CC} \quad (4)$$

Figure 5 shows the functional diagram of I_{TERM}.

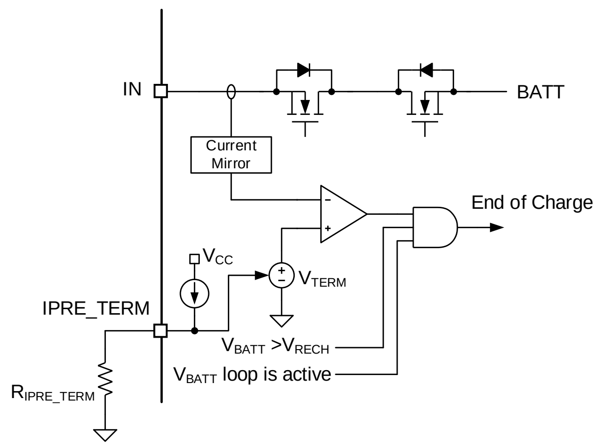


Figure 5: Functional Diagram of I_{TERM}

Where $K_{TERM-CC}$ is 224.72Ω/%.

For example, if R_{IPRE_TERM} is 1.13kΩ, then the proportion of I_{TERM} to I_{CC} is 5%.

When IPRE_TERM pin is floated, I_{TERM} is fixed at 10% of the set I_{CC}.

Battery Temperature Monitor via the Negative Thermal Coefficient (NTC) Thermistor

Thermistor is the generic name for thermally sensitive resistors. Negative temperature coefficient (NTC) thermistors are typically called thermistors. Depending on the manufacturing method and structure, there are many shapes and characteristics for various purposes.

The thermistor resistances, unless otherwise specified, are classified at a standard temperature of 25°C. The temperature resistance is solely a function of its absolute temperature.

Refer to the thermistor datasheet for the mathematic expression that relates the resistance and absolute temperature of a thermistor. The resistance at absolute temperature T1 (R1) can be calculated with Equation (5):

$$R1 = R2 \times e^{\beta \times \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (5)$$

Where R2 is the resistance at absolute temperature T2, and β is a constant that depends on the material of the thermistor.

The MP2702 continuously monitors the battery's temperature by measuring the NTC pin voltage (V_{NTC}), which is generated by a precise current flowing from the NTC pin through the NTC resistor (R_{NTC}) to ground.

The MP2702 compares V_{NTC} to an internal threshold to determine the fault type that occurs and takes different actions accordingly. The current from the NTC pin is only active when V_{IN} is present.

Figure 6 shows the functional diagram of the NTC protection circuit.

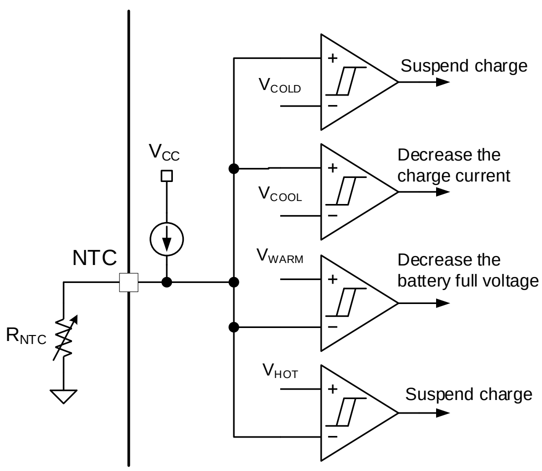


Figure 6: Functional Diagram of NTC Protection Circuit

To satisfy the JEITA requirements, the MP2702 provides four temperature thresholds: cold (0ºC by default), cool (10ºC by default), warm (45ºC by default), and hot (60ºC by default). For a given NTC thermistor, these temperatures correspond to V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}, respectively. If V_{NTC} is below V_{HOT}, or V_{NTC} exceeds V_{COLD}, then charging and the timers are suspended. If $V_{HOT} < V_{NTC} < V_{WARM}$, or if $V_{COOL} < V_{NTC} < V_{COLD}$, then the charging behavior is configured via the OTP. The preset thresholds are defined based on a thermistor where β = 3435K. Figure 7 shows the NTC JEITA profile.

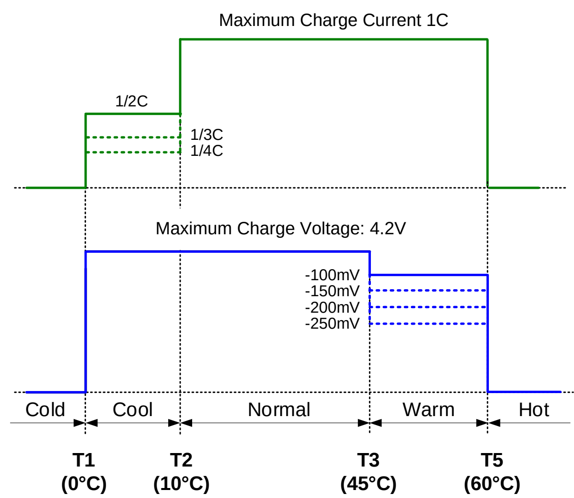


Figure 7: NTC JEITA Profile

EN Pin Control

The MP2702 provides a dedicated EN pin to disable the entire chip completely. In this situation, the quiescent current (I_Q) at the IN and BATT pins is minimized. When the chip is disabled by the EN pin, both the ACOK and CHG pins enter a high-impedance (Hi-Z) state.

Charge Enable Control

In addition to EN pin control, charging can be disabled by pulling the NTC pin to GND. This allows the ACOK pin to remain low, provided a normal input is available. To enable charging, the five conditions below must be met:

1. Pull the EN pin to ground or leave the pin floating to enable the chip.
2. The NTC pin is not pulled to GND.
3. There are no NTC faults that can suspend charging.

4. There is no timer fault present.
5. There is no thermal fault present.

Floated NTC Mode

When the NTC pin is floated, V_{NTC} is 3.6V. Since this exceeds the 2.5V charge termination disable threshold, the charge termination and safety timer are disabled.

To avoid overlap between the termination disable threshold and the cold temperature threshold, an internal loop can decrease the NTC bias current when V_{NTC} exceeds 2V. This prevents a cold thermistor from setting V_{NTC} above 2.5V.

Input Over-Voltage Protection (OVP)

The MP2702 provides input over-voltage protection (OVP). When V_{IN} rises to the input OVP threshold (V_{IN_OVP}), the MP2702 stops charging. Once V_{IN} drops back to its normal range, the device starts charging automatically.

V_{IN_OVP} is set to 6V for 1-cell applications and 14.4V for 2-cell applications.

Battery Over-Voltage Protection (OVP)

If V_{BATT} exceeds the battery OVP threshold (V_{BATT_OVP}), charging stops. If V_{BATT} is below the V_{BATT_OVP} falling threshold, the battery state transitions from battery OVP to charge termination.

Safety Charge Timer

The MP2702 provides a backup charge timer to ensure charge safety. When any new charge cycle starts, if the charging stays in trickle charge and pre-charge for 1 hour, or the entire charge process lasts for 10 hours (configurable via the OTP), charging automatically stops and the fault is reported. Once charging transitions from fast charge to pre-charge, the pre-charge timer resets.

After the safety timer expires, it can be reset by one of the actions below:

- Pull the $\overline{\text{EN}}$ pin high
- Re-plug V_{IN}
- Pull the NTC pin to GND

Operation Indication

The MP2702 has two open-drain indicators to report the V_{IN} and charging status. Table 3 shows the $\overline{\text{ACOK}}$ pin indication.

Table 3: $\overline{\text{ACOK}}$ Indication

V_{IN} Status	$\overline{\text{ACOK}}$
V_{IN} UVLO	Hi-Z
V_{IN} OVP	Hi-Z
$V_{IN} < V_{BATT} + V_{HDRM}$	Hi-Z
Normal input ($V_{IN} > V_{BATT} + V_{HDRM}$, and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVP}$), $\overline{\text{EN}}$ = low	Low
$\overline{\text{EN}}$ = high	Hi-Z

For $\overline{\text{CHG}}$ indication, the $\overline{\text{CHG}}$ pin is set low when charging is in process. After charge termination, the $\overline{\text{CHG}}$ pin enters a Hi-Z state. When charging is disabled by the NTC pin, the $\overline{\text{CHG}}$ pin also enters a Hi-Z state. In addition, the $\overline{\text{CHG}}$ pin can indicate fault events including NTC faults, timer faults, and charge OCP.

After the input power on or the charge being enabled, there is a 600ms deglitch time for the $\overline{\text{CHG}}$ indicator, which remains in a Hi-Z state during this blanking time.

Table 4 on page 20 shows the $\overline{\text{CHG}}$ pin indication.

Table 4: CHG Indication

Charging Status	CHG
Invalid input	Hi-Z
EN= high	Hi-Z
Charge disabled by pulling NTC to ground	Hi-Z
Charge termination	Hi-Z
Charge in process	Low
NTC fault, timer fault, charge OCP	Blinking (1Hz)

Thermal Regulation and Thermal Shutdown

During the battery charging process, the MP2702 continuously monitors the internal junction temperature (T_J) to avoid overheating the chip. If the internal temperature reaches the thermal regulation threshold (T_{J_REG}), the MP2702 starts to reduce the charge current to prevent higher power dissipation.

If T_J reaches the thermal shutdown threshold (T_{J_SHDN}), the MP2702 stops charging immediately. Once T_J drops below the T_{J_SHDN} falling threshold, the device resumes normal operation.

One-Time Programmable (OTP) Memory

The MP2702 provides OTP memory to configure the default value of several parameters. See the One-Time Programmable (OTP) Memory Map section on page 21 for the configurable parameters. Contact MPS to obtain a custom OTP setting.

ONE-TIME PROGRAMMABLE (OTP) MEMORY MAP

REG00h: Battery Voltage Threshold Setting

This register sets the battery cells' information and battery regulation voltage for each cell.

Bits	Bit Name	Default	Description
7	CELLS	1'b0	Selects the battery cell. 0: 1 cell (default) 1: 2 cells
6	RESERVED	1'b0	Reserved.
5:0	VBATT_REG	6'b100100	Sets the battery regulation voltage. Range: 2.4V/cell (000000) to 4.5V/cell (101010) Offset: 2.4V/cell Step: 50mV/cell Default: 4.2V/cell (100100)

REG01h: Timer and Thermal Setting

This register sets the safety charge timer and internal junction temperature (T_J) regulation threshold.

Bits	Bit Name	Default	Description
7	TMR_PRE	1'b1	Sets the safety timer for trickle charge and pre-charge. 0: Disabled 1: 1 hour (default)
6	TMR_EN	1'b1	Sets the safety timer enable control. 0: Disabled 1: Enabled (default)
5:3	TMR_SET	3'b010	Sets the safety timer for entire charge process. Range: 2 hours (000) to 30 hours (111) Offset: 2 hours Step: 4 hours Default: 10 hours (010)
2	RESERVED	1'b0	Reserved.
1	TJ_REG	1'b1	Sets the T_J regulation loop. 0: 100°C 1: 120°C
0	RESERVED	1'b0	Reserved.

REG02h: Input Voltage Limit Setting

This register sets the input voltage (V_{IN}) limit loop threshold. If V_{IN} drops below this threshold, charge current decreases to prevent V_{IN} from dropping further.

Bits	Bit Name	Default	Description
7:6	RESERVED	2'b00	Reserved.
5:4	VIN_LIM	2'b10	Sets the V_{IN} limit. 00: Reserved 01: 4.375V/cell 10: 4.5V/cell (default) 11: 4.75V/cell
3:0	RESERVED	4'b0000	Reserved.

REG03h: JEITA Temperature Threshold Setting

This register sets the JEITA hot, warm, cool, and cold temperature thresholds.

Bits	Bit Name	Default	Description
7:6	VHOT	2’b10	Sets the hot falling threshold. 00: 0.208V (50°C) 01: 0.176V (55°C) 10: 0.151V (60°C, default) 11: 0.129V (65°C)
5:4	VWARM	2’b01	Sets the warm falling threshold. 00: 0.291V (40°C) 01: 0.245V (45°C, default) 10: 0.205V (50°C) 11: 0.176V (55°C)
3:2	VCOOL	2’b10	Sets the cool rising threshold. 00: 1.377V (0°C) 01: 1.111V (5°C) 10: 0.902V (10°C, default) 11: 0.737V (15°C)
1:0	VCOLD	2’b01	Sets the cold rising threshold. 00: 1.732V (-5°C) 01: 1.377V (0°C, default) 10: 1.111V (5°C) 11: 0.902V (10°C)

REG04h: JEITA Protection Setting

This register sets the charge behavior during the JEITA warm and cool temperature windows.

Bits	Bit Name	Default	Description
7:6	WARM_ACT	2’b01	Sets the charge action when the NTC is warm. 00: No action. Charging stops when the NTC is hot 01: Reduce V_{BATT_REG} when the NTC is warm (default) 10: Reduce I_{CC} when the NTC is warm 11: Reduce both V_{BATT_REG} and I_{CC} when the NTC is warm
5:4	COOL_ACT	2’b10	Sets the charge action when the NTC is cool. 00: No action. Charging stops when NTC is cold 01: Reduce V_{BATT_REG} when the NTC is cool 10: Reduce I_{CC} when the NTC is cool (default) 11: Reduce both V_{BATT_REG} and I_{CC} when the NTC is cool
3:2	JEITA_VSET	2’b00	00: V_{BATT_REG} - 100mV/cell (default) 01: V_{BATT_REG} - 150mV/cell 10: V_{BATT_REG} - 200mV/cell 11: V_{BATT_REG} - 250mV/cell
1:0	JEITA_ISET	2’b00	00: 50% of I_{CC} (default) 01: 33% of I_{CC} 10: 25% of I_{CC} 11: 0% of I_{CC} (disable charge)

REG05h: Pre-Charge Threshold Setting

This register sets the pre-charge threshold.

Bits	Bit Name	Default	Description
7:2	RESERVED	6'b000000	Reserved.
1:0	VBATT_PRE	2'b01	Sets the pre-charge threshold. 00: 2.5V/cell 01: 2.8V/cell (default) 10: 3.0V/cell 11: 3.2V/cell

APPLICATION INFORMATION

Setting the Fast Charge Current

A resistor connected between the ISET and GND pins sets I_{CC}. The relationship between I_{CC} and R_{ISET} can be calculated with Equation (6):

$$I_{CC} = \frac{V_{REF} / k}{R_{ISET}} \quad (6)$$

Where V_{REF} is 1.2V, and k is 2.18 x 10^{-3}.

For example, R_{ISET} must be set to 550Ω to set I_{CC} to 1A.

Setting the Pre-Charge Current and Termination Current

The pre-charge current is set as percentage of I_{CC} by connecting a resistor between the IPRE_TERM and GND pins.

The ratio of I_{PRE} to I_{CC} can be calculated with Equation (7):

$$I_{PRE} / I_{CC} = R_{IPRE\_TERM} / K_{PRE\text{-}CC} \quad (7)$$

Where $K_{PRE\text{-}CC}$ is 112.36Ω/%.

For example, to set I_{PRE} / I_{CC} to 10%, connect a 1.13kΩ resistor between the IPRE_TERM and GND pins.

When IPRE_TERM pin is floated, I_{PRE} is fixed at 20% of the set I_{CC}.

I_{TERM} is fixed as 50% of I_{PRE}.

Setting the Battery Cell

The MP2702 supports 1-cell and 2-cell batteries, where the battery cell is configured via the OTP.

For 2-cell applications, the battery hot insertion or short is not allowed when V_{IN} is present, and charge is enabled.

Selecting the Input Capacitor

An input capacitor (C_{IN}) is typically required for stable operation. In the MP2702, a minimum 1μF capacitor must be connected between the IN and GND pins to achieve stable operation across a full load current range. The capacitor's voltage rating must exceed the normal V_{IN} level. A low-ESR ceramic capacitor (X5R or X7R) is recommended.

Selecting the BATT to GND Capacitor

The capacitor connected between BATT and GND is also required for the MP2702. A minimum 1μF ceramic capacitor (X5R or X7R) is suitable for most applications.

Selecting the NTC Resistor

The MP2702 supports configurable JEITA that is based on a precise 50μA current source flowing through the external NTC thermistor. To use this function, connect a 10kΩ NTC thermistor with β = 3435K between the NTC and GND pins.

The JEITA threshold can be configured via the OTP.

If NTC is not used, connect a fixed 10kΩ resistor between the NTC and GND pins.

PCB Layout Guidelines

Place the external capacitors as close to the IC as possible to ensure the smallest input and output inductances and ground impedance.

TYPICAL APPLICATION CIRCUIT

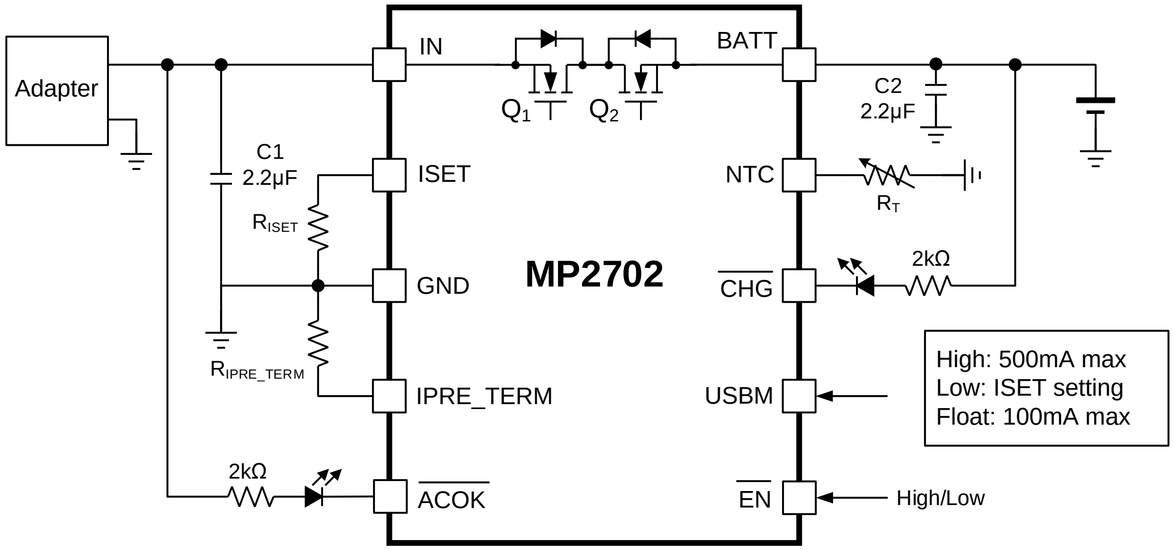


Figure 8: Typical Application Circuit

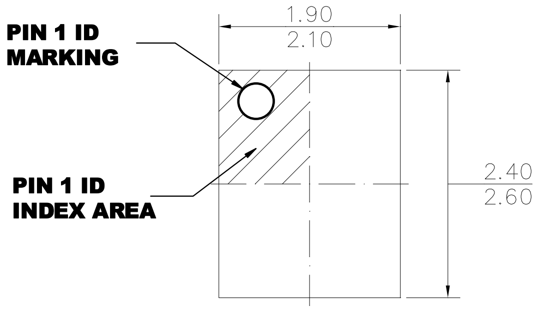
Table 5 shows the key bill of materials for Figure 8.

Table 5: Key Bill of Material for Figure 8

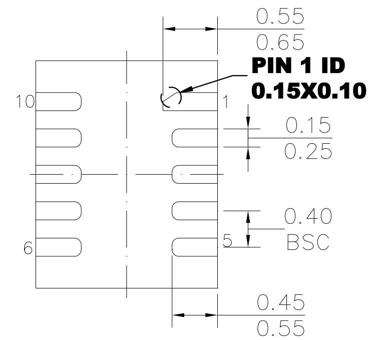
Qty	Ref	Value	Description	Package	Manufacturer
1	C1	2.2μF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C2	2.2μF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	R_T	10kΩ	β = 3435K	Any	Any

PACKAGE INFORMATION

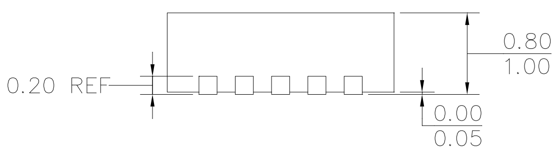
QFN-10 (2mmx2.5mm)



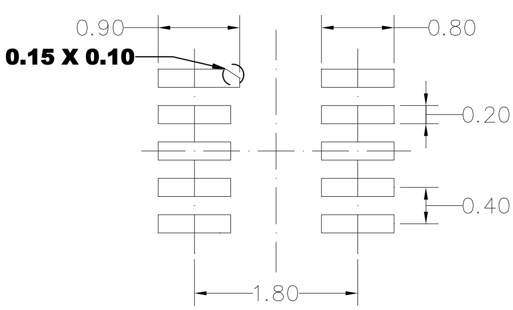
TOP VIEW



BOTTOM VIEW



SIDE VIEW

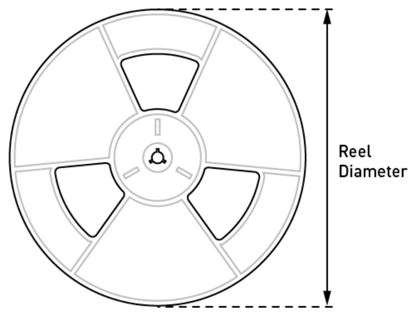


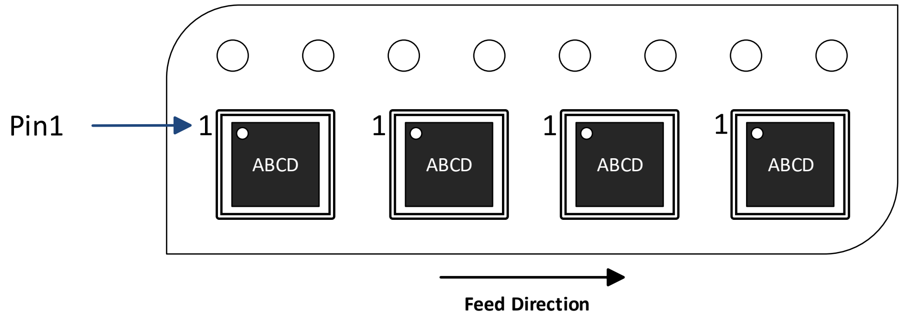
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2702GRP-xxxx-Z	QFN-10 (2mmx2.5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/15/2023	Initial Release	-