MP28162

High-Efficiency, Synchronous Buck-Boost Converter with 1.5A MOSFETs in a Small WLCSP Package

DESCRIPTION

The MP28162 is a high-efficiency, low quiescent current (I_Q), buck-boost converter that operates from an input voltage (V_{IN}) exceeding, below, or equal to the output voltage (V_{OUT}). The device provides a compact solution for products powered by single-cell Li-ion or multi-cell alkaline batteries, where V_{OUT} is within the battery voltage (V_{BATT}) range.

Current-mode control and the fixed pulse-width modulation (PWM) frequency provide optimal stability and transient response. The fixed 2MHz switching frequency (f_{REQ}) and integrated, low on resistance ($R_{DS(ON)}$) MOSFETs reduce the solution size and maintain high efficiency.

To optimize battery life, the MP28162 employs selectable pulse-skip mode to reduce f_{REQ} under light-load conditions. For low-noise applications where pulse-skip mode may cause interference, a high-logic input on the MODE/SYNC pin ensures that the part operates in fixed-frequency PWM mode under all load conditions.

The MP28162 is available in a small WLCSP-15 (1.3mmx2.1mm) package.

FEATURES

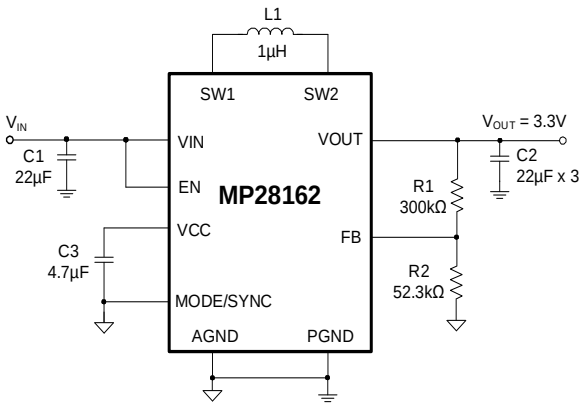
- 1.8V Minimum Start-Up Input Voltage (V_{IN})
- 1.2V to 5.5V Operating V_{IN} Range
- 1.5V to 5.5V Output Voltage (V_{OUT}) Range
- 1.5A Switching Current Limit
- 2MHz Fixed Switching Frequency (f_{REQ}) or External Synchronous f_{REQ}
- Selectable Pulse-Skip Mode or Pulse-Width Modulation (PWM) Mode
- 25µA Typical Quiescent Current (I_Q)
- Load Disconnect during Shutdown
- Internal Soft Start (SS) and Compensation
- Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Protection (OTP)
- Available in a Small WLCSP-15 (1.3mmx2.1mm) Package

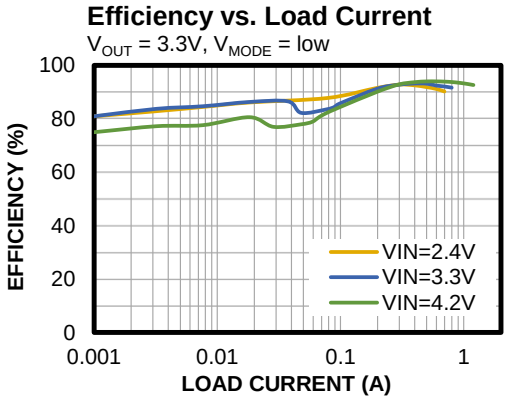
MPL Optimized Performance with MPS Inductor MPL-AT2010 Series

APPLICATIONS

- Optical Modules
- Portable Instruments
- Battery-Powered Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28162GC	WLCSP-15 (1.3mmx2.1mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP28162GC-Z).

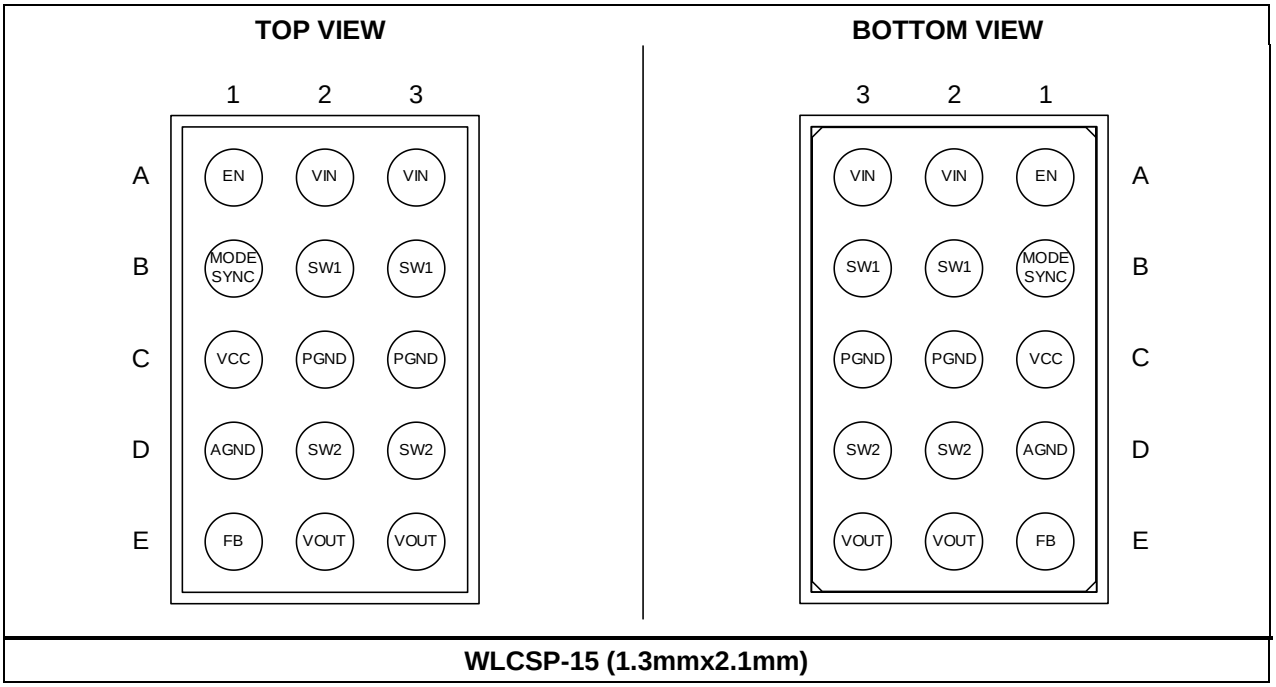
TOP MARKING

JMY

LLL

JM: Product code of MP28162GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-15 (1.3mmx2.1mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	EN	**On/off control.** Pull the EN pin high to enable the MP28162; pull EN low or float the pin to disable all internal circuits. EN is pulled down to AGND with an internal, 1.5MΩ resistor.
A2, A3	VIN	**Supply voltage for power stage.**
B1	MODE/ SYNC	**Operation mode selection.** If the MODE/SYNC pin is low, the MP28162 switches between pulse-skip mode and fixed-frequency pulse-width modulation (PWM) mode automatically, based on the load level. If MODE/SYNC is high, the MP28162 works in fixed-frqeuncy PWM mode continuously. An external clock can be applied to MODE/SYNC for switching frequency (f_{REQ}) synchronization. MODE/SYNC is pulled down to AGND with an internal, 1MΩ resistor. Pull MODE/SYNC high or low via a resistor below 10kΩ.
B2, B3	SW1	**Switch 1.** Internal switches are connected to the SW1 pin. Connect an inductor between the SW1 and SW2 pins.
C1	VCC	**Supply voltage for control stage.** The VCC pin is powered by the higher value between the input voltage (V_{IN}) and output voltage (V_{OUT}). Decouple VCC using a 4.7μF capacitor.
C2, C3	PGND	**Power ground.**
D1	AGND	**Signal ground.**
D2, D3	SW2	**Switch 2.** Internal switches are connected to the SW2 pin. Connect an inductor between the SW1 and SW2 pins.
E1	FB	**Output voltage feedback.** Keep the FB pin and its associated traces far from noise sources such as SW1 and SW2.
E2, E3	VOUT	**Buck-boost converter output.** Place an output capacitor (C_{OUT}) close to the VOUT and PGND pins.

ABSOLUTE MAXIMUM RATINGS (1)

VIN to GND .....-0.3V to +6V
SW1, SW2 to GND .....-0.3V (-1.5V for <5ns)
……..to +6.5V (+7.5V for <5ns)
All other pins .....-0.3V to +6V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
WLCSP-15 (1.3mmx2.1mm)..... 2.23W (5)
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±1000V

Recommended Operating Conditions (3)

Start-up supply voltage (V_{ST}) .....1.8V to 5.5V
Operating voltage (V_{IN}) ..... 1.2V to 5.5V (4)
Output voltage (V_{OUT}).....1.5V to 5.5V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

WLCSP-15(1.3mmx2.1mm)		
EVL28162-C-00A (5)	..... 56	1.... °C/W
JESD51-7 (6)	..... 94	1.7 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If VCC is powered from a source exceeding 1.8V (such as V_{OUT}), the MP28162 can operate with V_{IN} as low as 1.2V, but the load capability is lower when V_{IN} = 1.2V due to the high $R_{DS(ON)}$ of SWA and low current limit.
5) Measured on the EVL28162-C-00A, a 2-layer, 1oz PCB (51mmx51mm).
6) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = V_{OUT} = 3.3V, T_J = -40°C to +125°C, typical value is tested at 25°C, unless otherwise noted. (7)

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$	Float VCC, rising V_{IN}, test V_{IN} when the IC starts up	1.55	1.7	1.77	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_F}$	V_{OUT} = 3.3V, falling V_{IN}		0.69		V
V_{CC} UVLO falling threshold	$V_{CC\_UVLO\_F}$	V_{IN} = 1.2V, falling V_{CC}	1.45	1.56	1.67	V
Feedback reference voltage	V_{REF}	T_J = 25°C	495	500	505	mV
		T_J = -40°C to +125°C	492.5	500	507.5	mV
Switching frequency	f_{REQ}		1700	2000	2300	kHz
Synchronization frequency range			1000		3000	kHz
Switching current limit	I_{SW}		1.3	1.5	1.85	A
N-MOSFET on resistance	$R_{DS(ON)\_N}$	SWB, SWC		35		mΩ
P-MOSFET on resistance	$R_{DS(ON)\_P}$	SWA, SWD		45		mΩ
Quiescent current	I_Q	V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, test V_{OUT}		25		µA
		V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, test V_{IN}		3.3		µA
Shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C			3	µA
Soft-start time (8)	t_{SS}	Internal V_{REF} from 0V to 0.5V		2		ms
EN/MODE low input voltage					0.4	V
EN/MODE high input voltage			1.2			V
EN input current	I_{EN}	V_{EN} = 3.3V		2.1		µA
		V_{EN} = 0V		0		µA
Thermal shutdown (8)	T_{SHDN}			160		°C
Thermal shutdown hysteresis (8)	T_{HYS}			20		°C

Notes:

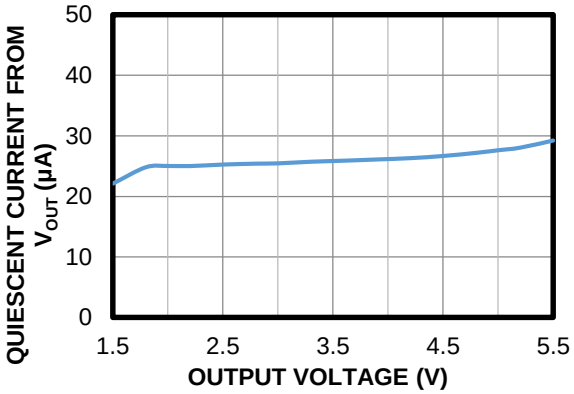
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Not tested in production. Guaranteed by sample characterization.

TYPICAL CHARACTERISTICS

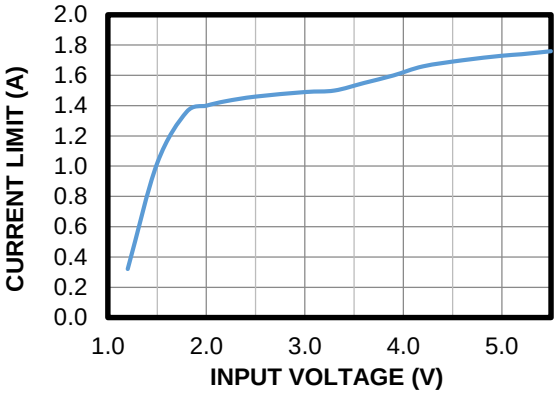
V_{IN} = 3.3V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Quiescent Current From V_{OUT}

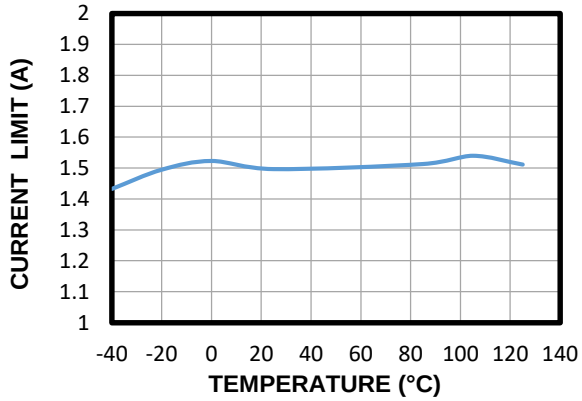
V_{IN} = 1.2V, V_{EN} = high



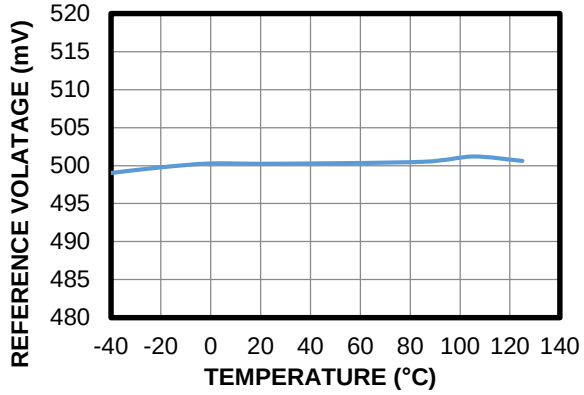
Current Limit vs. Input Voltage



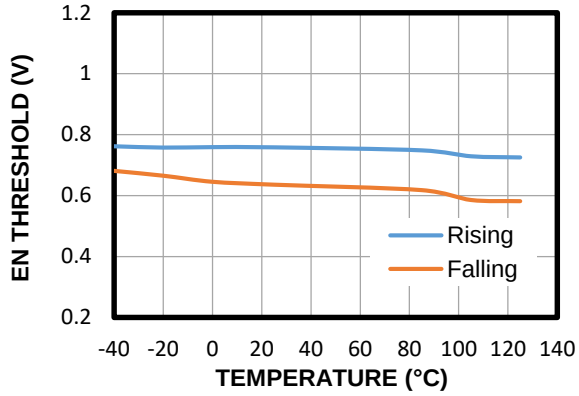
Current Limit vs. Temperature



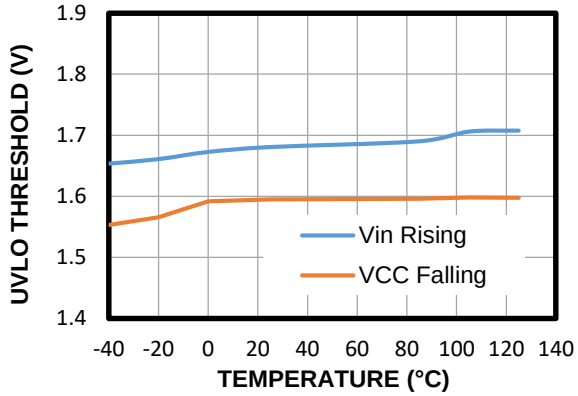
Reference Voltage vs. Temperature



EN Threshold vs. Temperature



UVLO Threshold vs. Temperature

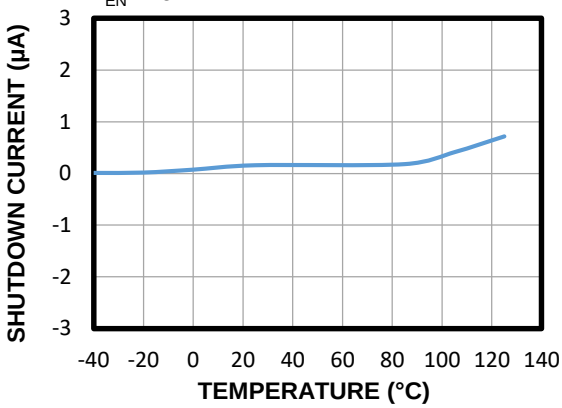


TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

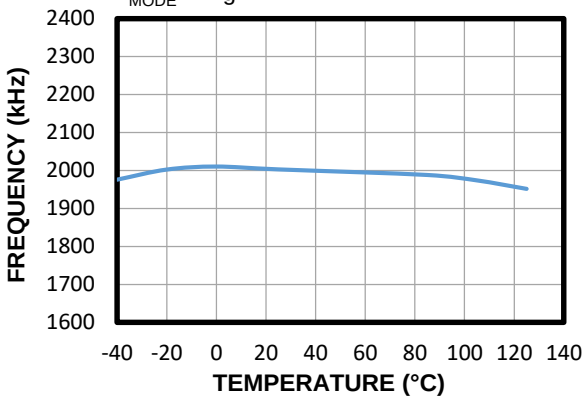
Shutdown Current

V_{EN} = low



Frequency vs. Temperature

V_{MODE} = high

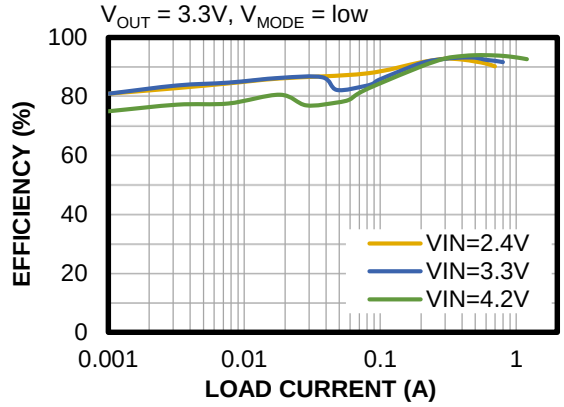


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 3 x 22µF, T_A = 25°C, unless otherwise noted.

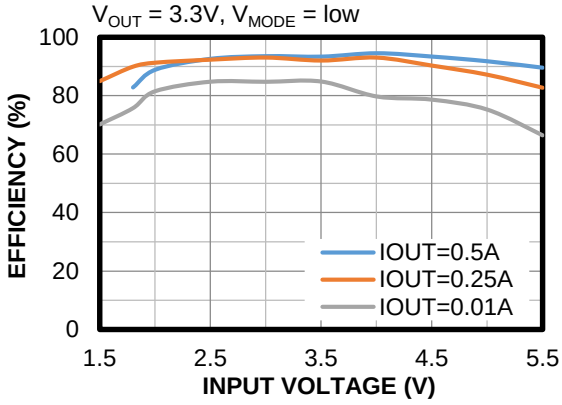
Efficiency vs. Load Current

V_{OUT} = 3.3V, V_{MODE} = low



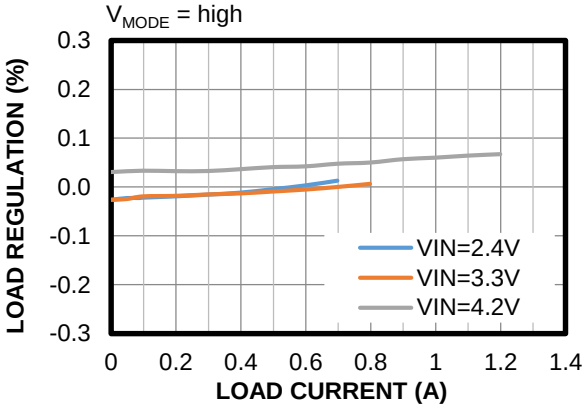
Efficiency vs. Input Voltage

V_{OUT} = 3.3V, V_{MODE} = low



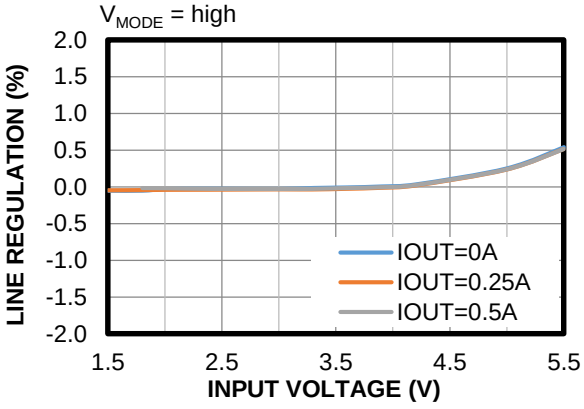
Load Regulation

V_{MODE} = high



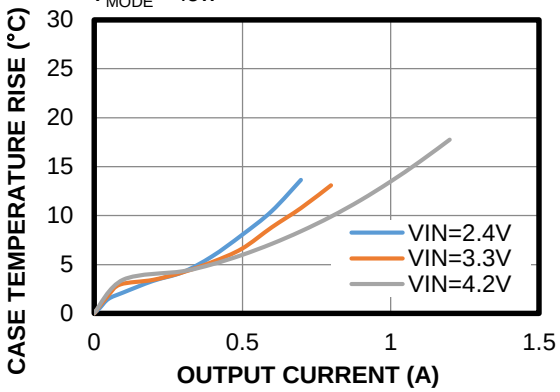
Line Regulation

V_{MODE} = high



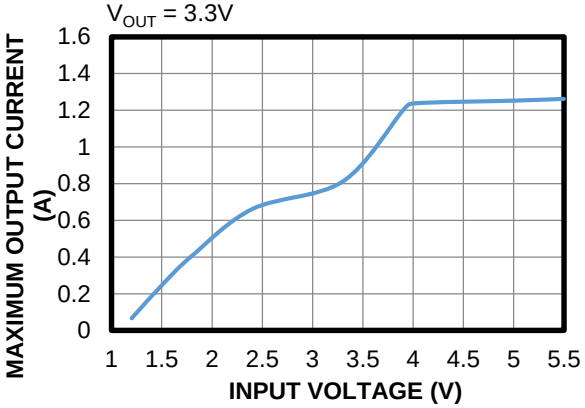
Case Temperature Rise

V_{MODE} = low



Maximum Output Current vs. Input Voltage (9)

V_{OUT} = 3.3V



Note:

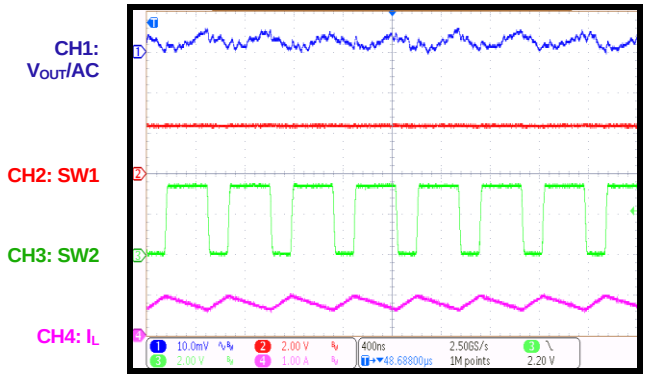
9) Tested with the MP28162, which has a 1.3A I_{LIMIT} at V_{IN} = 3.3V.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 3 x 22µF, T_A = 25°C, unless otherwise noted.

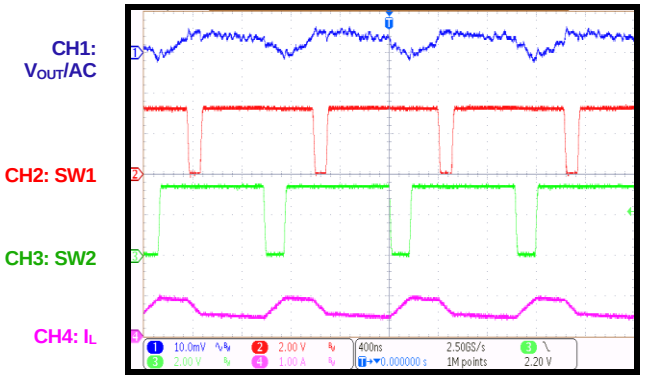
Steady State

V_{IN} = 2.4V, I_{OUT} = 0.5A, V_{MODE} = low



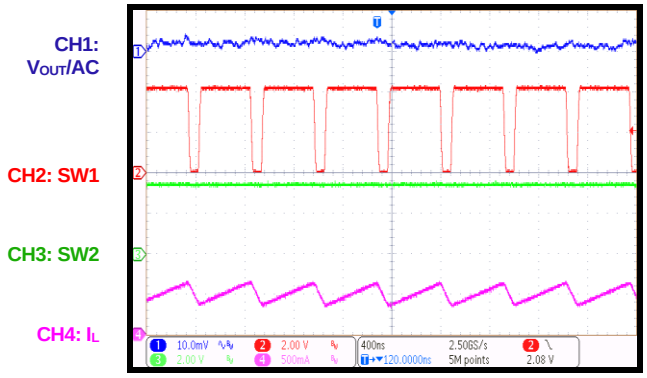
Steady State

V_{IN} = 3.3V, I_{OUT} = 0.5A, V_{MODE} = low



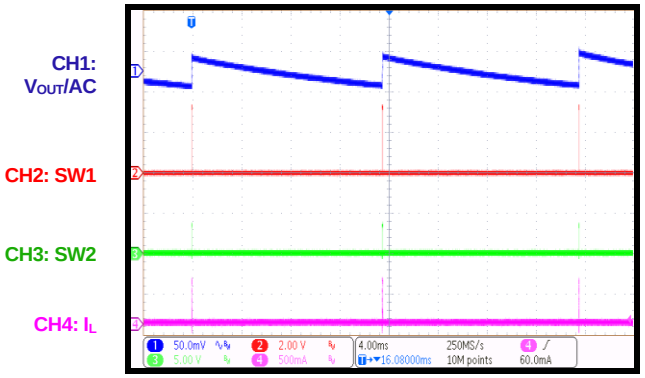
Steady State

V_{IN} = 4.2V, I_{OUT} = 0.5A, V_{MODE} = low



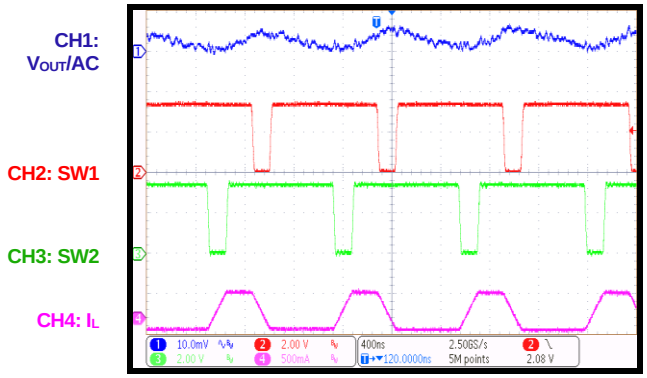
Steady State

V_{IN} = 3.3V, I_{OUT} = 0A, V_{MODE} = low



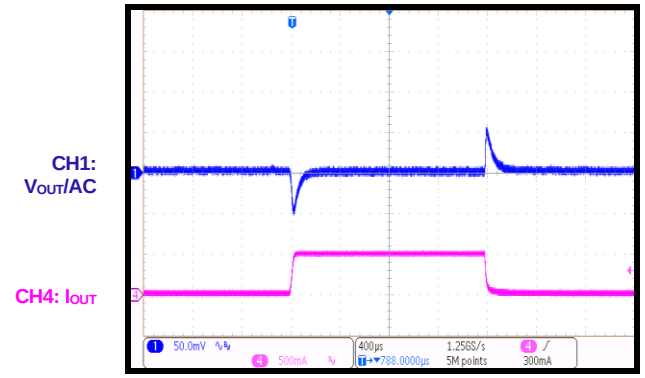
Steady State

V_{IN} = 3.3V, I_{OUT} = 0A, V_{MODE} = high



Transient Response

V_{IN} = 3.3V, I_{OUT} = 0A to 0.5A, V_{MODE} = high

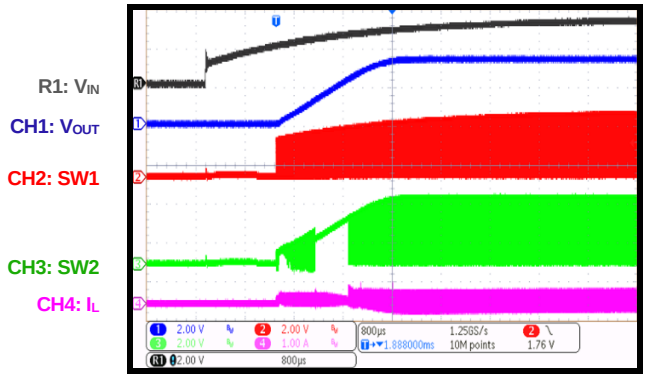


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 3 x 22µF, T_A = 25°C, unless otherwise noted.

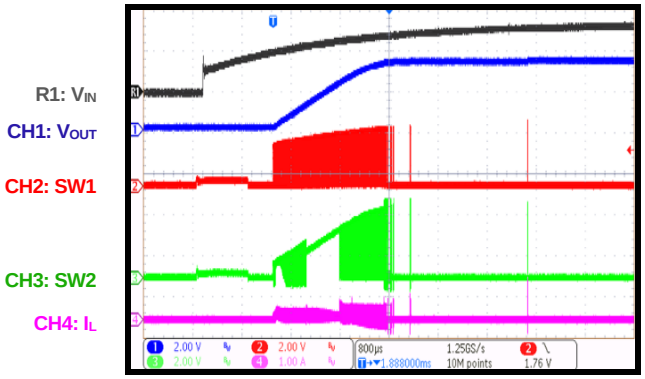
Start-Up

I_{OUT} = 0A, V_{MODE} = high



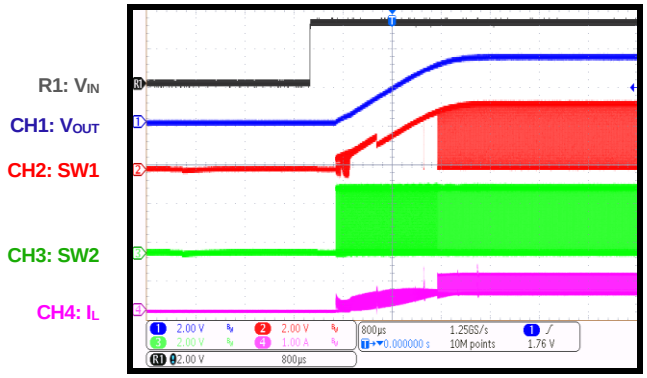
Start-Up

I_{OUT} = 0A, V_{MODE} = low



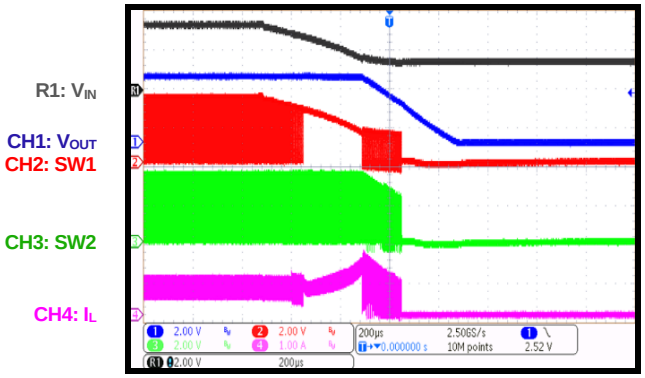
Start-Up

I_{OUT} = 0.5A, V_{MODE} = low



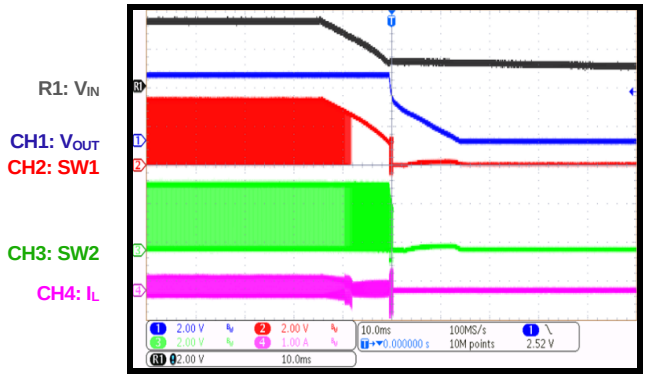
Shutdown

I_{OUT} = 0.5A, V_{MODE} = low



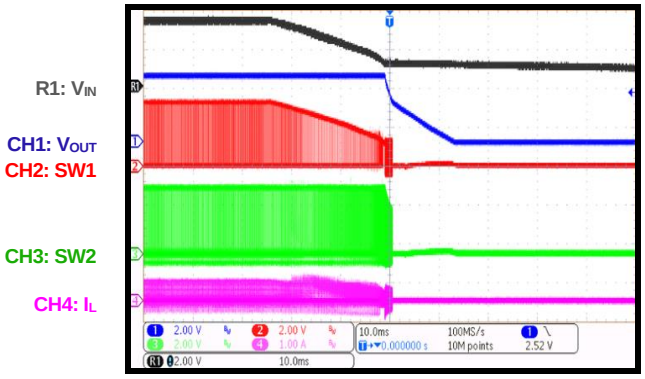
Shutdown

I_{OUT} = 0.01A, V_{MODE} = high



Shutdown

I_{OUT} = 0.01A, V_{MODE} = low

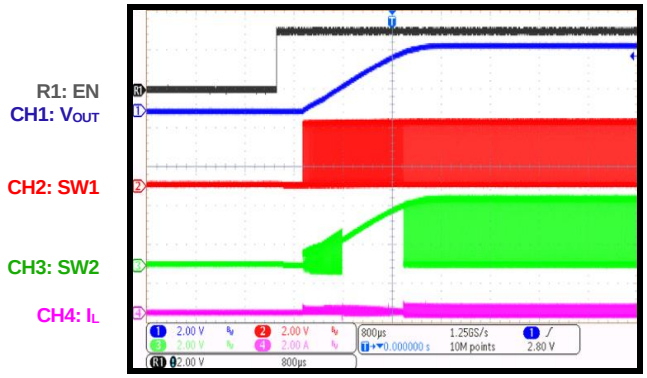


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 3 x 22µF, T_A = 25°C, unless otherwise noted.

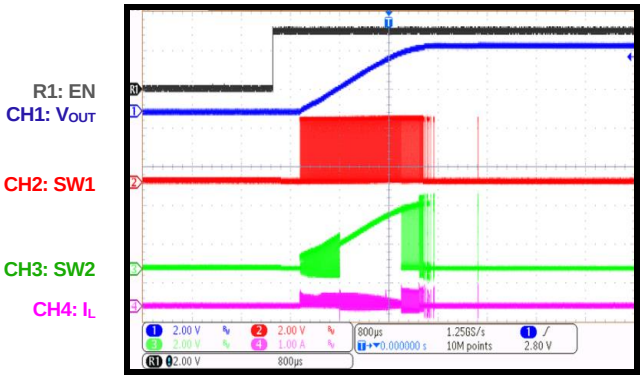
Start-Up through EN

I_{OUT} = 0A, V_{MODE} = high



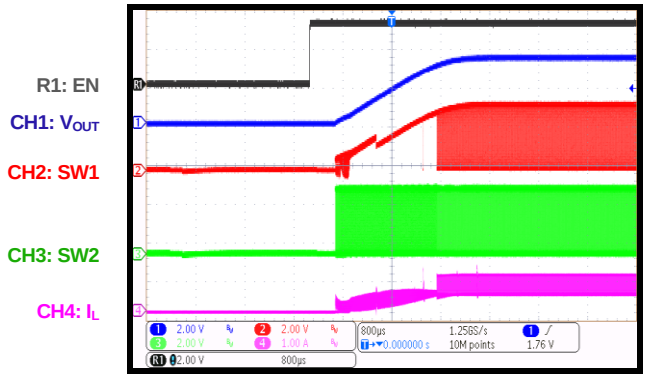
Start-Up through EN

I_{OUT} = 0A, V_{MODE} = low



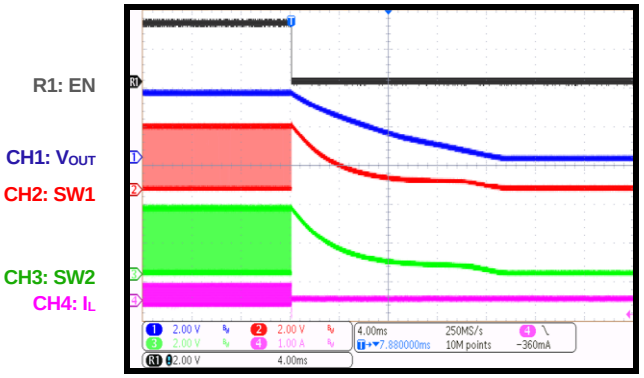
Start-Up through EN

I_{OUT} = 0.5A, V_{MODE} = low



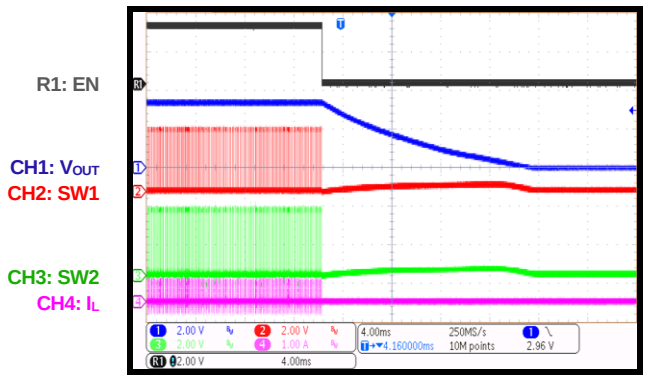
Shutdown through EN

I_{OUT} = 0.01A, V_{MODE} = high



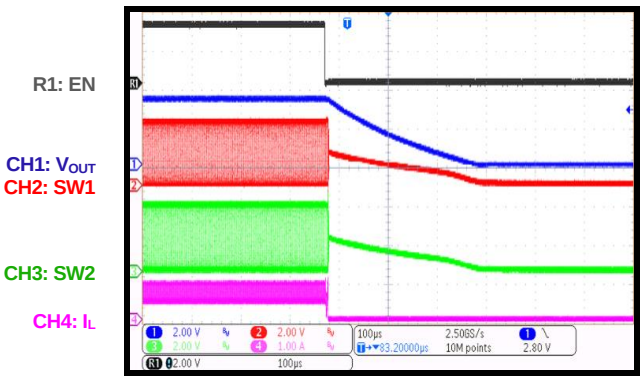
Shutdown through EN

I_{OUT} = 0.01A, V_{MODE} = low



Shutdown through EN

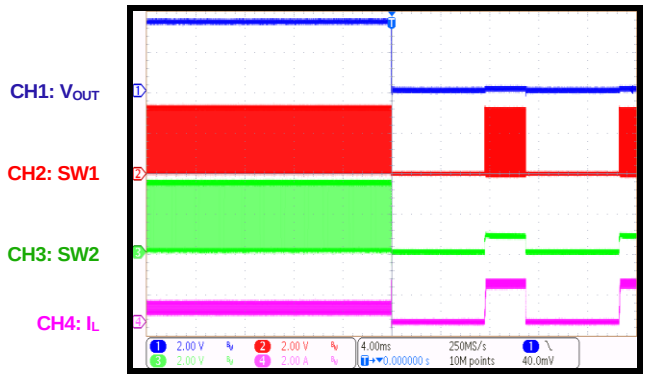
I_{OUT} = 0.5A, V_{MODE} = low



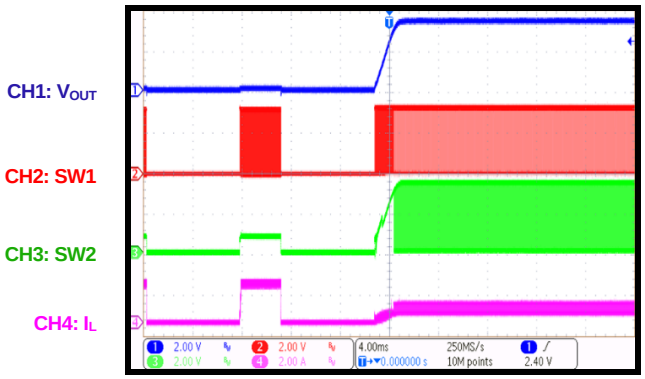
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 3 x 22µF, T_A = 25°C, unless otherwise noted.

SCP Entry



SCP Recovery



FUNCTIONAL BLOCK DIAGRAM

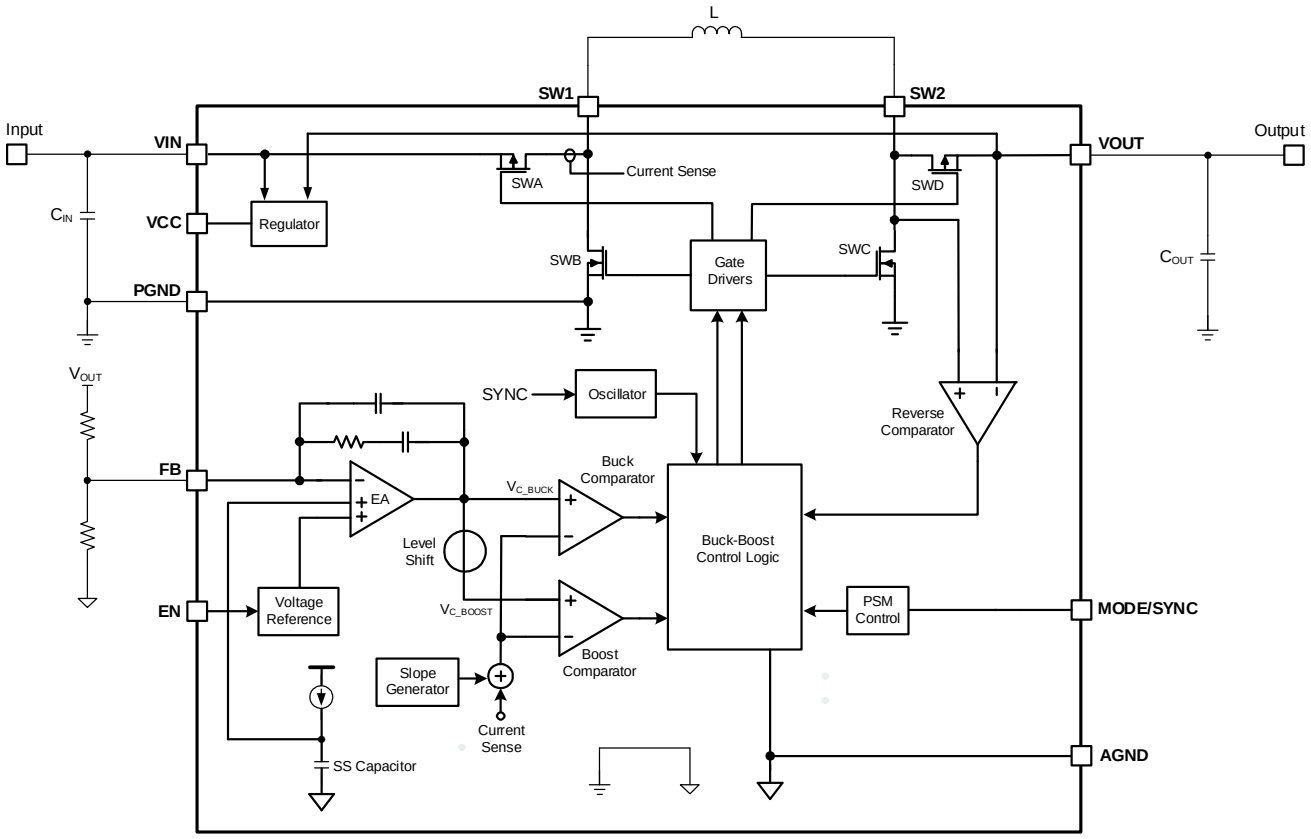


Figure 1: Functional Block Diagram

OPERATION

The MP28162 is a high-efficiency, dual-mode, buck-boost converter that provides an output voltage (V_{OUT}) exceeding, below, equal to the input voltage (V_{IN}). V_{OUT} is sensed via the FB pin through an external resistor divider connected from the output to ground (see Figure 1 on page 12). The difference between the FB pin voltage (V_{FB}) and the internal reference voltage (V_{REF}) is amplified by the error amplifier (EA) to generate a control signal (V_{C_BUCK}). By comparing V_{C_BUCK} with the internal current ramp signal (the sensed SWA current with slope compensation) via the buck comparator, a pulse-width modulation (PWM) control signal for the buck legs (SWA and SWB) is generated.

Another control signal (V_{C_BOOST}) is derived from V_{C_BUCK} through the level shift. V_{C_BOOST} is compared with the sensed SWA current with slope compensation via the boost comparator and generates a PWM control signal for the boost legs (SWC and SWD). Figure 2 shows the buck-boost converter's switching topology.

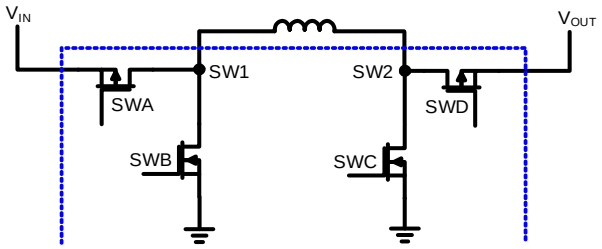


Figure 2: **Buck-Boost Switching Topology**

Buck Region ($V_{IN} > V_{OUT}$)

If V_{IN} significantly exceeds V_{OUT}, the MP28162 can deliver energy to the load within SWA's maximum duty cycle by switching SWA and SWB. The converter operates in buck mode. In this mode, SWD remains on and SWC is off. V_{C_BUCK} is typically compared with the current ramp signal to generate a PWM output. Therefore, SWA and SWB are pulse-width modulated to produce the required duty cycle and eventually support V_{OUT}.

Buck-Boost Region ($V_{IN} \approx V_{OUT}$)

If V_{IN} is close to V_{OUT}, the MP28162 is unable to provide sufficient energy to the load due to SWA's maximum duty cycle. As a result, the current ramp signal cannot trigger V_{C_BUCK} during the first period, and SWA remains on with 100% duty cycle. If SWB does not turn on during the first period, the converter enters boost mode in the secondary period (where SWC switches) and an offset voltage is added to the current ramp signal to enable it to reach V_{C_BUCK}. SWC turns off when the current ramp signal intersects with V_{C_BOOST} during the secondary period, and SWD conducts the inductor current (I_L) when SWC is off. This is called boost operation.

SWA turns off when the current ramp signal intersects with V_{C_BUCK} in the secondary period, and SWB turns on to conduct I_L after SWA turns off. This is called buck operation.

If SWB turns on during the secondary period, boost operation (SWC on) is disabled in the following cycle. If SWA continues to conduct with 100% duty in the secondary cycle, the boost operation is also enabled in the following duty cycle. SWA and SWB, and SWC and SWD switch during this condition simultaneously. This is called buck-boost mode.

Boost Region ($V_{IN} < V_{OUT}$)

If V_{IN} is significantly below V_{OUT}, V_{C_BUCK} remains above the current ramp signal. The offset voltage is added to the current signal, which prevents SWB from turning on in all cycles. The boost operation (SWC on) is enabled in every cycle based on the logic, resulting in only SWC and SWD switching. This is called boost mode. In this mode, SWC and SWD are pulse-width modulated to produce the required duty cycle and eventually support V_{OUT} regulation.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the device from operating at an insufficient V_{IN}. The MP28162's UVLO circuit monitors V_{CC}. During start-up, V_{IN} must exceed its UVLO rising threshold ($V_{IN\_UVLO\_R}$) to support a sufficient V_{CC} and enable the IC. After the IC is enabled, VCC is powered by V_{IN} or V_{OUT}, depending on which value is higher. Thus, the IC can work even if V_{IN} drops to 1.2V, unless V_{CC} drops to its UVLO falling threshold ($V_{CC\_UVLO\_F}$).

During start-up, if VCC has a biased voltage from another power supply, the MP28162 can work with a 1.2V V_{IN}. If V_{IN} is below 1.2V significantly, SWA's on resistance ($R_{DS(ON)}$) is high, and the MP28162 cannot supply a large amount of power to the output. If V_{IN} drops to 0.69V, the MP28162 stops working.

VCC Power Supply

When the EN pin is high and V_{IN} ramps up, V_{IN} charges VCC. If V_{IN} exceeds $V_{IN\_UVLO\_R}$, the MP28162 begins working. All the MP28162's internal circuits are supplied by VCC, which is decoupled with a ceramic capacitor. After the system starts up, VCC is powered internally by the higher value between V_{IN} or V_{OUT}. If VCC is powered by V_{OUT}, the MP28162 does not shut down until V_{IN} drops to $V_{IN\_UVLO\_F}$ (0.69V) or V_{CC} drops to $V_{CC\_UVLO\_F}$ (1.56V). It is not recommended to supply the MP28162 with V_{IN} below 1.2V, even if VCC has a biased voltage due to SWA (P-MOSFET) having an $R_{DS(ON)}$ that is too high when V_{IN} is low. Even with a 1.2V V_{IN}, the load capability is weaker than the high input condition due to the $R_{DS(ON)}$.

Internal Soft Start (SS)

When EN is high and V_{IN} exceeds $V_{IN\_UVLO\_R}$, the MP28162 starts up with a soft-start (SS) function. The internal SS signal ramps up and controls the feedback V_{REF}. After a blank time of 3.5ms, if V_{OUT} does not rise to 60% of the normal V_{OUT}, or if V_{OUT} is pulled down to 60% of the normal V_{OUT} due to an overload, then the SS signal is pulled down to GND and hiccup protection is triggered. During start-up or hiccup recovery, an internal SS signal is clamped to V_{FB} + 0.3V if V_{OUT} does not increase. This limit can prevent a V_{OUT} overshoot if the heavy load disappears suddenly during start-up.

During start-up or recovery from hiccup, if there is already some voltage on the output, this voltage is discharged by the negative current limit (-1A when the MP28162 operates in PWM mode regardless of the MODE/SYNC configuration) to reach the SS voltage (V_{SS}). V_{OUT} then rises normally.

MODE/SYNC Configuration

The MP28162 can be configured to pulse-skip mode or fixed-frequency PWM mode under light-load conditions via the MODE/SYNC pin. When MODE/SYNC is pulled high, the MP28162 operates in fixed-frequency PWM mode. The current conducts while the I_L direction reverses. In this mode, the V_{OUT} ripple is below the ripple in power-save mode (PSM), but the power loss is higher due to the high-frequency switching.

When MODE/SYNC is pulled low, the MP28162 enters PSM automatically when the load decreases. In PSM, a group of switching pulses are initiated when the internal V_{C_BUCK} exceeds the PSM threshold (where the group of pulses starts with SWA and SWC on and ends with SWB and SWD on). SWD turns off if the SWD current flows from VOUT to SW2 in each period.

During start-up or short-circuit protection (SCP) recovery, the MP28162 works in fixed-frequency PWM mode, even if MODE/SYNC is low. The negative I_L is limited to about -1A, which is the same in constant frequency mode.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP) with Two Current Limits

The MP28162 has one switching peak current limit (1.5A typically).

In overload or short-circuit conditions, V_{OUT} drops due to the switching current limit (I_{SW}). If V_{OUT} drops below 60% of its normal output, the MP28162 stops switching and recovers after

~8ms with hiccup mode protection. After switching stops in hiccup protection, the internal SS signal is clamped to V_{FB} + 0.3V, where V_{FB} is the divided voltage from the residual V_{OUT}. This smooths the SS process when the MP28162 recovers from hiccup protection.

During the SS time (t_{SS}), the MP28162 blanks during hiccup protection for about 3.5ms. After the 3.5ms blank time, if V_{OUT} remains below 60% of the normal voltage, the MP28162 resumes hiccup mode. If V_{OUT} exceeds 60% of the normal value, the MP28162 enters normal operation.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds the typical over-voltage protection (OVP) value (6.3V), switching stops. This helps protect the device from high-voltage stress. After V_{OUT} drops to about 5.3V, switching recovers automatically.

Over-Temperature Protection (OTP)

An internal temperature sensor continuously monitors the IC's junction temperature (T_J). If T_J exceeds 160°C, the device stops operating. Once T_J falls below 140°C, the device resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT}. Select the R2 value first. A small R2 value leads to considerable quiescent current (I_Q) loss while a too large R2 value makes the FB sensitive to noise. It is recommended to choose a value between 10kΩ and 100kΩ for R2. R1 can then be calculated with Equation (1):

$$R1 = (\frac{V_{OUT}}{V_{FB}} - 1) \times R2 \quad (1)$$

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AT2010 Series**

With one buck-boost topology circuit, the inductor must support the buck application with the maximum V_{IN} (V_{IN_MAX}) and boost application with the minimum V_{IN} (V_{IN_MAX}). The minimum buck inductance (L_{MIN_BUCK}) can be determined based on the buck mode current ripple, which is calculated with Equation (2):

$$L_{MIN\_BUCK} = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times f_{REQ} \times \Delta I_L} \quad (2)$$

Where f_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak I_L ripple.

The minimum boost inductance (L_{MIN_BOOST}) can be determined based on the boost mode current ripple, which is calculated with Equation (3):

$$L_{MIN\_BOOST} = \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (3)$$

The minimum inductance for the application must exceed the calculated L_{MIN_BUCK} and L_{MIN_BOOST} from Equation (2) and Equation (3), respectively.

The inductor must also support the peak buck current (I_{PEAK_BUCK}) and peak boost current (I_{PEAK_BOOST}) to avoid saturation:

I_{PEAK_BUCK} can be calculated Equation (4):

$$I_{PEAK\_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{IN\_MAX} \times f_{REQ} \times L} \quad (4)$$

I_{PEAK_BOOST} can be calculated with Equation (5):

$$I_{PEAK\_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN}} + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (5)$$

Where η is the estimated efficiency.

MPS inductors are optimized and tested for use with a complete line of integrated circuits. Table 1 lists the power inductor recommendations. Select a part number based on the design requirements.

Table 1: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AT2010-1R0	1μH	MPS
MPL-AT2010-1R5	1.5μH	
MPL-AT2010-2R2	2.2μH	

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input and Output Capacitors

It is recommended to select ceramic capacitors with a low ESR for the input capacitor (C_{IN}) and output capacitor (C_{OUT}). This filters any disturbances in the input and output line and achieves stable operation.

C_{OUT} affects loop stability. C_{IN} and C_{OUT} must be placed as close as possible to the device. See Figure 4 on page 18 for more details on optimizing the capacitor selection.

Design Example

Table 2 shows a design example following the application guidelines for the specifications below.

Table 2: Design Example

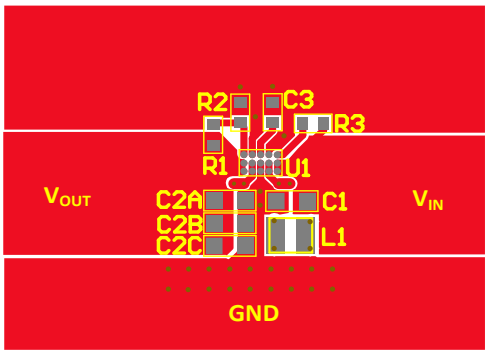
Start-Up V_{IN} (V)	Operating V_{IN} (V)	V_{OUT} (V)
1.8 to 5.5	1.2 to 5.5	3.3

Figure 4 on page 18 shows the detailed application circuit. The typical performance and waveforms are shown in the Typical Performance Characteristics section on page 7.

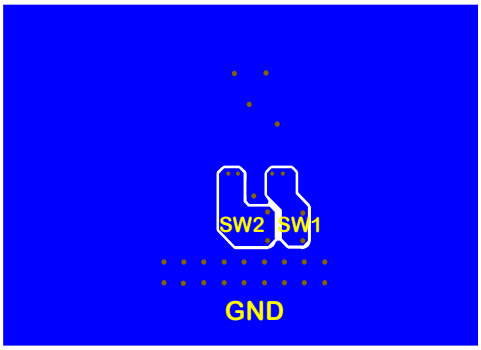
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place C_{IN} and C_{OUT} close to VIN, VOUT, and PGND.
2. Place the VCC decoupling capacitor close to VCC and AGND.
3. Keep the feedback resistor divider very close to FB.
4. Keep the feedback trace far away from noise sources such as SW1 and SW2.
5. Use wide copper layout for GND, VIN, and VOUT to conduct current and decrease the case temperature rise.
6. Place vias in the GND copper around the chip to improve thermal performance.



Top Layer



Bottom Layer

Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

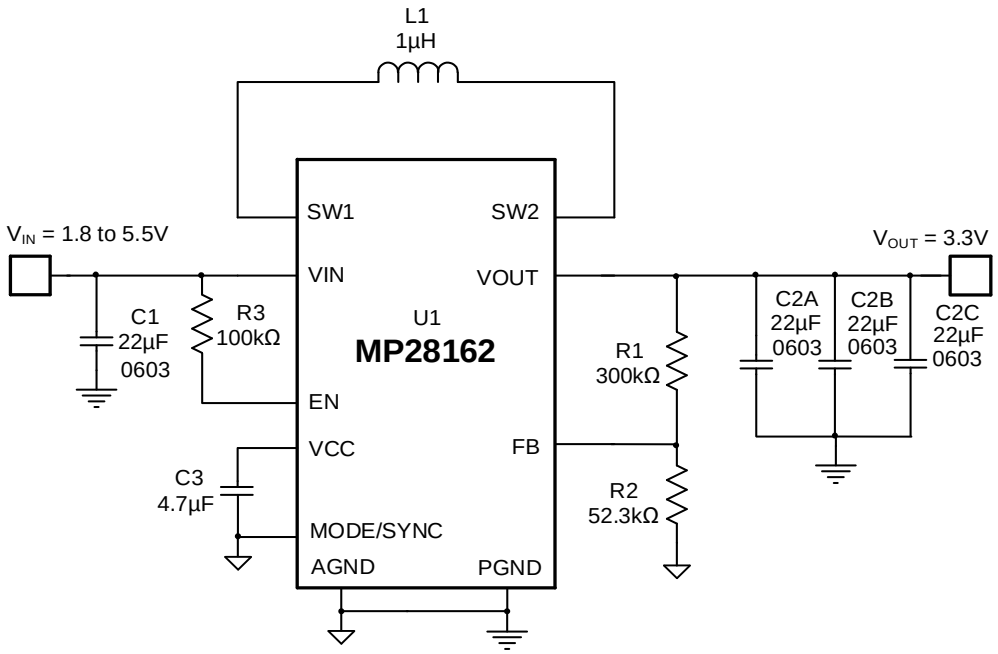
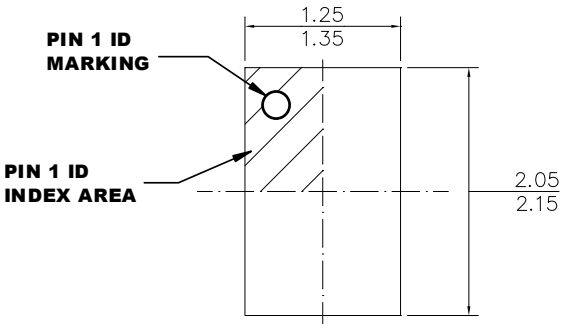


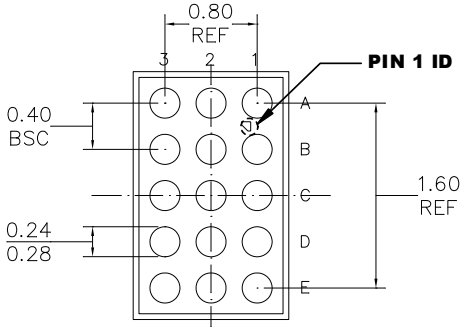
Figure 4: Typical Application Circuit (V_{OUT} = 3.3V)

PACKAGE INFORMATION

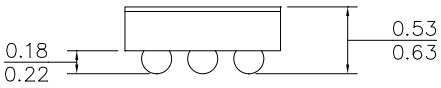
WLCSP-15 (1.3mmx2.1mm)



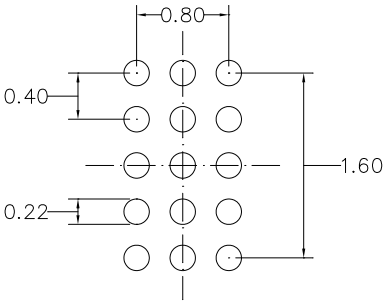
TOP VIEW



BOTTOM VIEW



SIDE VIEW

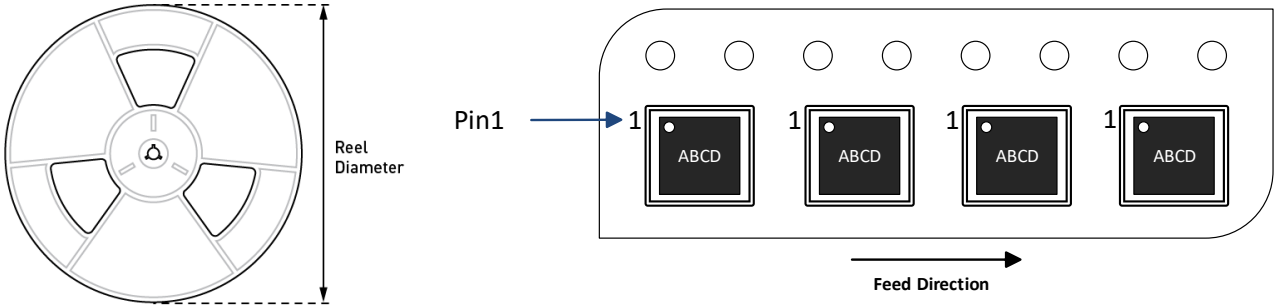


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28162GC-Z	WLCSP-15 (1.3mmx 2.1mm)	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/16/2023	Initial Release	-