MP3275

Fault Protected 16 Channel, 12-Bit Data Acquisition Subsystem

FEATURES

- **Fault Protected 16-Channel 12-Bit A/D Converter with Sample & Hold, Reference, Clock and 3-State Outputs**
- **Fast Conversion, less than 15μS**
- **2's Complement and Serial Data Output**
- **Remote Analog Ground Sensing**
- **Overvoltage Protected Input (±50 V over the Supply Voltages)**
- **Precision Reference for Long Term Stability and Low Gain T.C.**
- **Guaranteed Linearity Over Temperature**
- **Guaranteed Performance at +12/–5 V, ±12 & ±15 V**
- **Low Power (7 mW per Channel Typical)**
- **Parallel Version: MP3276**
- **32 Channel Version: MP3274**

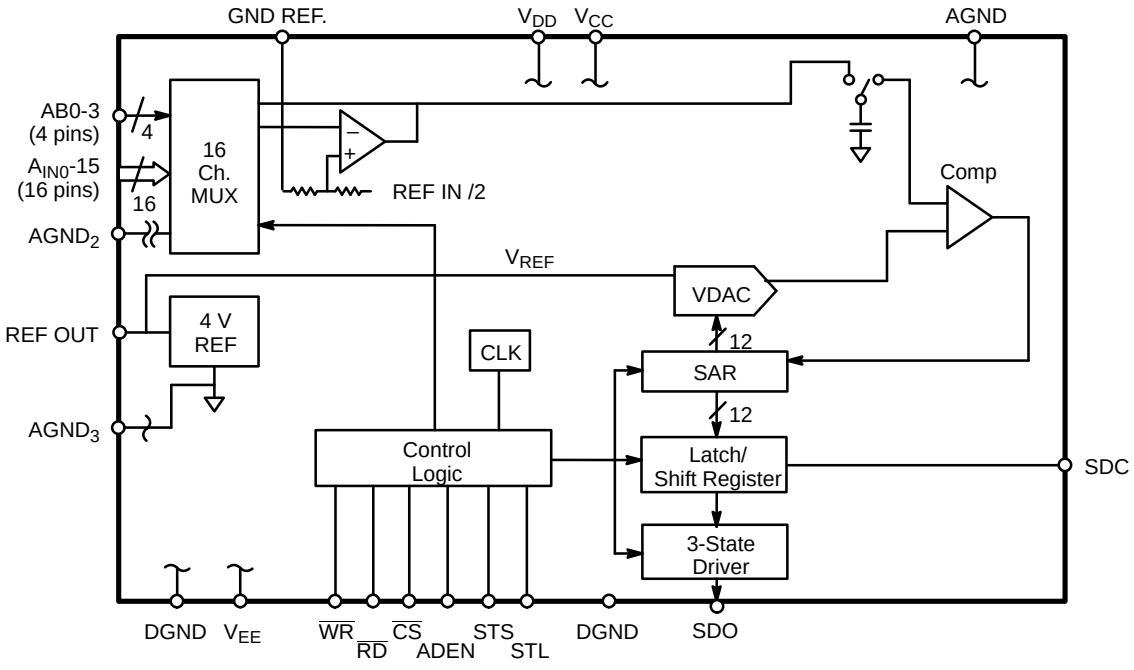
GENERAL DESCRIPTION

The MP3275 is a complete 16-channel, 12-bit Data Acquisition Subsystem with serial data port. Implemented using an advanced BiCMOS process, the converter combines a 16-channel passive overvoltage-protected multiplexer instrumentation amp, a sample & hold, a SAR, a 12-bit decoded D/A, a comparator, a precision reference and the control logic to achieve an accurate conversion in less than 15μs, and a mux/instrumentation amp settling period of less than 10μs.

A unique input design provides input overvoltage protection to ±50 V over the supply voltages. The circuit design can allow for an overvoltage condition on unselected channels without disrupting the measured channel or operation of the MP3275! The internal 4 V reference has sufficient output current to provide other system reference needs. Precision thin film scaling and offset resistors are laser trimmed to provide for less than 2 LSB INL for ±10 V inputs on all channels.

In addition, the MP3275 will output either full scale (0111 ....) for overrange and – full scale (1000....) for underrange conditions. This greatly simplifies microprocessor software development.

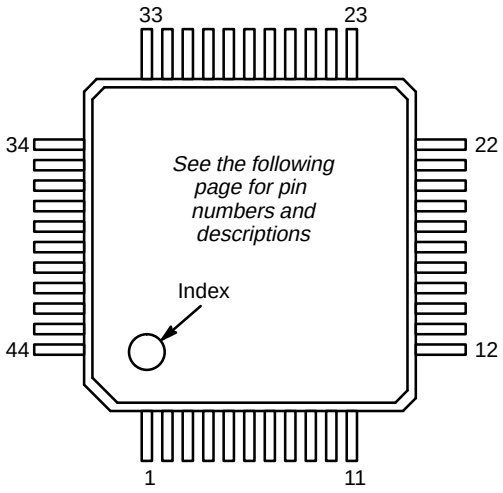
SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP3275AE	±2	±2

PIN CONFIGURATIONS



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{EE}	– Analog Supply. –4.75 To – 16.5
2	$A_{IN}12$	Channel 12 Analog Input, 1100
3	$A_{IN}13$	Channel 13 Analog Input, 1101
4	$A_{IN}14$	Channel 14 Analog Input, 1110
5	$A_{IN}15$	Channel 15 Analog Input, 1111
6	GNDREF	+ Input To Mux / Instrumentation Amp
7	AGND	A/D Section Analog Ground
8	REF	Reference Output
9	$AGND_3$	Reference Analog Ground
10	DGND	Digital Logic And Output Ground
11	SDC	Serial Data Clock
12	N/C	No Connection
13	N/C	No Connection
14	N/C	No Connection
15	N/C	No Connection
16	SDO	Serial Data Out
17	STS	Conversion Status, Converting=1
18	STL	Input Settling Period State = 1
19	DGND	Digital Gnd, Low Current
20	$\overline{RD}$	Enable Serial Data Out
21	$\overline{CS}$	Chip Select
22	$\overline{WR}$	Input Address And Conversion Control

PIN NO.	NAME	DESCRIPTION
23	ADEN	Address Update Enable=1, Ignore=0
24	AB3	Input Address Bit 3, (MSB)
25	AB2	Input Address Bit 2
26	AB1	Input Address Bit 1
27	AB0	Input Address Bit 0, (LSB)
28	V_{DD}	Digital Logic & Output Supply, +4.75 to + 5.25 Volts
29	V_{CC}	Analog + Supply, +11.4 to + 16.5 Volts
30	$A_{IN}0$	Channel 0 Analog Input, 0000
31	$A_{IN}1$	Channel 1 Analog Input, 0001
32	$A_{IN}2$	Channel 2 Analog Input, 0010
33	$A_{IN}3$	Channel 3 Analog Input, 0011
34	N/C	No Connection
35	$A_{IN}4$	Channel 4 Analog Input, 0100
36	$A_{IN}5$	Channel 5 Analog Input, 0101
37	$A_{IN}6$	Channel 6 Analog Input, 0110
38	$A_{IN}7$	Channel 7 Analog Input, 0111
39	$AGND_2$	Agnd For Input Mux Section
40	$A_{IN}8$	Channel 7 Analog Input, 1000
41	N/C	No Connection
42	$A_{IN}9$	Channel 9 Analog Input, 1001
43	$A_{IN}10$	Channel 10 Analog Input, 1010
44	$A_{IN}11$	Channel 11 Analog Input, 1011

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, V_{CC} = 15 V, V_{EE} = –15 V, GNDRef = 0 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
Resolution (All Grades)	N	12				12		Bits
KEY FEATURES								
Resolution		12				12	Bits	
Conversion Time, Per Channel	t_{CONVR}			15		15	µs	
ACCURACY (A Grade)[1]								Refer to *Table 6.* for output coding
Differential Non-Linearity	DNL		3/4	2		2	LSB	
Integral Non-Linearity	INL		1	2		2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Code Error	EZS		2	±5		±10	LSB	fff to 000 [hex] transition
Full Scale Error	EFS		0.1	±0.35		±0.5	%	V_{REF}IN = 4.000 V
POWER SUPPLY REJECTION								Max change in Full Scale Calibration
V_{CC} = 15 V ±1.5 V or 12 V ±0.6 V				±1		±1	LSB	
V_{DD} = 5 V ±0.25 V				±2		±2.5	LSB	
V_{EE} = –15 V ±1.5 V or –12 V ±0.6 V –5 V ±0.25 V				±1		±1	LSB	
REFERENCE VOLTAGES								
Voltage Output	$V_{REF(+)}$	3.975	4.0	4.025	3.970	4.030	V	
Ref. Source Current		3.0	4.0		3.0		mA	
Ref. Sink Current			20				µA	
ANALOG INPUT								
Input Voltage Range[3]	V_{IN}	–10		10	–10	10	V	
Ground Reference	GND Ref.							
CM Range[2]		–3		+3	–3	3	V	
CM RR			TBD				LSB/V	
Input Resistance	R_{IN}	100	130		100		kΩ	
Input Capacitance[2]	C_{IN}		5				pF	
Aperture Delay[2]	t_{AP}		180				ns	From $\overline{WR}$ low to high after STL high to low
Channel-to-Channel Isolation[2]			–80	–70			dB	DC
DIGITAL INPUTS $\overline{WR}$, RD AB0-AB4, ADEN, SDC								
Logical “1” Voltage	V_{IH}	2.4		5.5	2.4	5.5	V	
Logical “0” Voltage	V_{IL}	–0.5		0.8	–0.5	0.8	V	
Leakage Currents[4]	I_{IN}	–5		5	–10	10	µA	V_{IN}=GND to V_{DD}
Input Capacitance[2]			5				pF	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS (Data Format 2's Complement) SDO, STS, STL								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.0			2.4		V	I_{SOURCE} = 0.5 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{SINK} = 1.6 mA
Tristate Leakage	I_{OZ}	–5		5	–5	5	µA	V_{OUT}=GND to V_{DD}
POWER SUPPLIES								
Operating Range								
V_{DD}		+4.5		+5.5	+4.5	+5.5	V	
V_{CC}		+11.4		+16.5	+11.4	+16.5	V	
V_{EE}		–4.75		–16.5	–4.75	–16.5	V	Tested at –11.4 and –16.5 only
Operating Current								
I_{DD}			2	7		7	mA	
I_{CC}			5	8		8	mA	
I_{EE}			1.5	3		3	mA	
Power Dissipation			110	200		200	mW	

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage
2. Guaranteed. Not tested.
3. All channel input pins and ground reference pin have protection which becomes active above ±60 V.
4. All digital inputs have diodes to V_{DD} and AGND. Input DC currents will not exceed specified limits for any input voltage between AGND and V_{DD}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... 0 to +16.5 V
V_{EE} to AGND ..... 0 to –16.5 V
V_{DD} to AGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Digital Inputs or Outputs ($\overline{WR}$, $\overline{RD}$, $\overline{CS}$, AB0-AB4, ADEN, SDC) to DGND ..... –0.5 V to V_{DD} +0.5 V
Analog Inputs ($A_{IN}0$ – $A_{IN}15$, GND REF) to AGND ..... ±60 V
REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating to 75°C
PQFP ..... 750 mW
Derates above 75°C ..... 10 mW/°C
Lead Temperature, Soldering ..... 300°C, 10 Sec
Storage Temperature (Ceramic) ..... –65°C to +150°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

PRODUCT INFORMATION

Basic Description

The MP3275 is a fault protected data acquisition subsystem available in monolithic form. This product contains all of the circuitry necessary to acquire 16 channels of quasi differential or single-ended analog signals at ±10 V input range and 15kHz bandwidth. Connections to power, the analog input signals and the digital system are all that is required. The MP3275's input circuitry is protected against active input signals present with the MP3275 power off. This is also the case for any channel exceeding the MP3275 analog input dynamic range without interfering with the channel being digitized. The channel address and channel conversion can be managed in two ways: random channel conversion or same channel conversion. Circuitry on the chip adds a MUX/instrumentation amp settling delay of 10µs max, when a new channel is selected (ADEN = 1). Conversion start is initiated without delay for the single-channel case (ADEN = 0). Data is available in serial format.

TIMING

Control and Timing Considerations

The MP3275 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 4 control lines: ADEN, $\overline{WR}$, $\overline{CS}$ and $\overline{RD}$ with their functions described in *Table 1.*

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	Comments
ADC Channel Select and Start Convert *(See Figure 1. and Table 2.)*							
1	X	X	X	—	0	0	No operation
0	↓	1	0	Hi-Z	0	0	No operation if ADEN = 0
0	↓	1	1	Hi-Z	↑	0	Input MUX channel selected, STL set on $\overline{WR}$ falling edge
0	0	1	X	Hi-Z	1	0	MUX select disabled
0	↑	1	X	Hi-Z	0	↑	Start convert on $\overline{WR}$ rising edge
0	1	1	X	Hi-Z	↓	↑	Start convert on STL falling edge
0	1	1	X	Hi-Z	0	↓	STS goes low at end of conversion
Read ADC Data *(See Figure 2. and Table 3.)*							
0	1	↓	X	—	0	0	SDO enabled
0	X	0	X	ADC	0	0	Data from previous conversion on SDO
0	X	↑	X	Hi-Z	0	0	SDO disabled
0	1	X	X	Hi-Z	0	1	SDO/$\overline{RD}$ disabled while STS high
0	X	0	X	Last ADC	1	0	Data from last conversion on SDO
0	⊓	0	0	Hi-Z	0	↑	STL, MUX select disabled with ADEN = 0, SDO disabled on STS rising edge
0	⊓	0	X	ADC	0	↓	New data appears on SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, SDO remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the SDO.

Table 1. Logic Truth Table

The MP3275 is easily interfaced to a wide variety of digital systems. Discussion of the timing requirements of the MP3275 control signals follows.

Figure 1. shows a complete timing diagram for the MP3275 convert start operation.

$\overline{WR}$ is used to initiate a conversion.

A conversion is started by taking $\overline{WR}$ low, then high again (conversion is enabled on the rising edge of $\overline{WR}$). There are two possible conditions that will affect conversion timing.

1. ADEN = 1. At the falling edge of $\overline{WR}$, the input channel is determined by the data present on the address bits. The track and hold begins to settle after which STL returns low, indicating that the multiplexer, buffer amp, and sample/hold have settled to less than 1/2 LSB of final value. If the rising edge of $\overline{WR}$ returns high prior to STL going low, conversion will begin on the falling edge of STL. If the rising edge of $\overline{WR}$ is delayed until after STL returns low, the input signal is sampled and the conversion is started at the rising edge of $\overline{WR}$ giving the user better control of the sampling time.
2. ADEN = 0. At the falling edge of $\overline{WR}$ the data present at the address is ignored and the channel selected during the previous conversion remains selected. In this case the track and hold settling time is omitted and STL never goes high. At the rising edge of $\overline{WR}$ the input signal is sampled, and conversion is started.

There are two possible states that the data output could be in during a conversion.

1. If $\overline{RD}$ is held high during a conversion the output would remain high impedance throughout the conversion. This is the preferred method of operation as any noise present on SDO is rejected.
2. If $\overline{RD}$ is held low during a conversion, the data present SDO will be from the previous conversion until the present conversion is completed, when STS returns low. The data from the new conversion will be available through SDO. The state of $\overline{RD}$ should not change during a conversion.

Once a conversion is started and the STL or STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The SDO output buffer cannot be enabled during conversion. In addition, all input and output changes during conversion can introduce noise, and should be avoided when possible.

ADC Write Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
ADC Control Timing					
Address to $\overline{WR}$ Set-Up Time	t_3	0	0	ns min	
Address to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{WR}$ Pulse Width	t_5	80	80	ns min	
ADEN to $\overline{WR}$ Set-Up Time	t_6		0	ns min	
ADC Conversion Timing					
$\overline{WR}$ to STL ↑ Delay	t_7	150	150	ns max	Load ckt of Figure 5, C_L = 20 pF, ADEN = 1
STL High (Settling Period)	t_8	10	15	µs max	Load ckt of Figure 5, C_L = 20 pF
STL to STS Low (Converting)	t_9	15	20	µs max	Load ckt of Figure 5, C_L = 20 pF
$\overline{WR}$ to STS High (ADEN = 0)	t_{12}	200	250	ns max	STL = 0 when ADEN = 0
$\overline{WR}$ to STS Low (ADEN = 1)	t_{10}	15	20	µs max	
STS High to SDO Relinquish Time	t_{13}	150	150	ns max	Load ckt of Figure 4
STS Low to Data Valid ($\overline{RD}$ = 0)	t_{14}	50	50	ns max	Load ckt of Figure 3, C_L = 20 pF

Table 2. ADC Write Timing
(See Figure 1.)

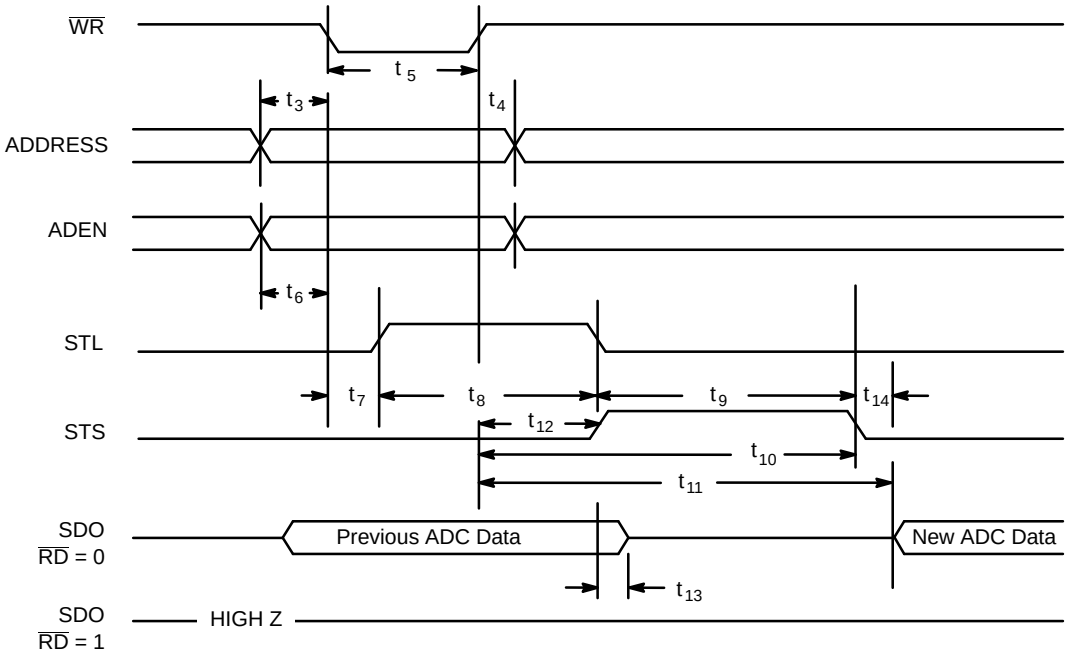


Figure 1. Timing for ADC Channel Select Start Conversion

ADC Read Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
$\overline{RD}$ to Data Valid Delay	t_{17}	100	150	ns max	Load ckt of *Figure 3.*, C_L = 20 pF
		150	200	ns max	Load ckt of *Figure 3.*, C_L = 100 pF
SDO Relinquish Time after $\overline{RD}$ High	t_{18}	100	150	ns max	Load ckt of *Figure 4.*
$\overline{RD}$ Pulse Width	t_{19}	100	150	ns min	

Table 3. ADC Read Timing
(*See Figure 2.*)

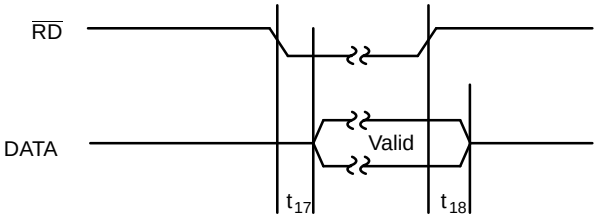
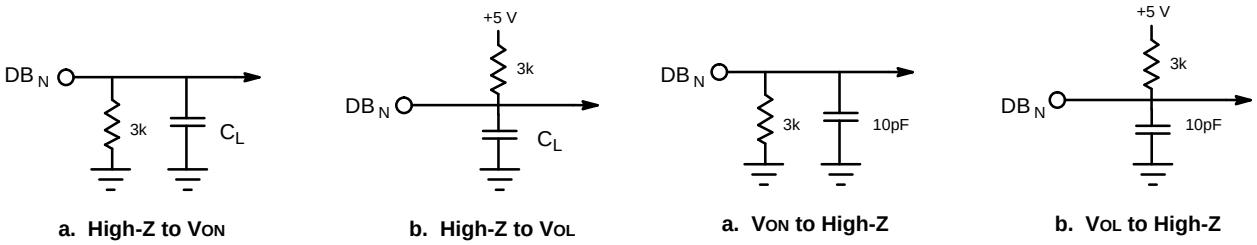


Figure 2. Timing for ADC Read



a. High-Z to VON b. High-Z to VOL a. VON to High-Z b. VOL to High-Z

Figure 3. Load Circuit for Data Access Time Test

Figure 4. Load Circuit for Bus Relinquish Time Test

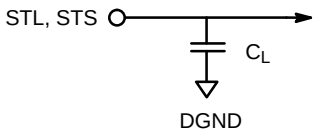


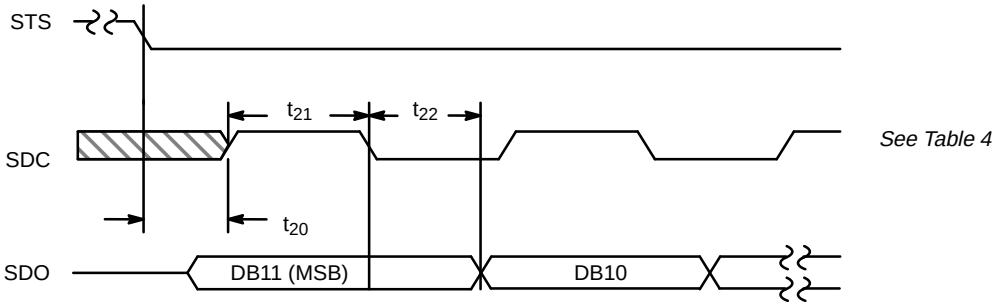
Figure 5. Load Circuit for $\overline{WR}$ to STS Delay

Serial Data Output

The serial data output sequence is MSB (DB11) first to LSB (DB0) last. The MSB (DB11) data bit appears at SDO when STS goes low. The second most significant bit appears at SDO on the SDC high-to-low transition next. The LSB (DB0) is present at SDO on the 11th SDC high-to-low transition.

Further information regarding serial control and timing is shown in *Figure 6., Table 4.* and *Table 5.*

For a minimum interconnect serial environment, the channel address state can be generated in at least two ways, using an address counter, or using an address serial to parallel converter. $\overline{WR}$ can then be used as the counter clock or shift register load signal as well as the A/D converter start convert signal on the rising edge. (Note that the falling edge loads the address present at the address port.)



SDC should be in a high state during the STS high period. SDC can make the first high to low transition after t_{21}.

Figure 6. Serial Data Mode Timing

Serial Data Output Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
STS low to SDO Valid, $\overline{RD}$ = 0	t_{20}	50	50	ns max	Load Ckt 4 of *Figure 3.*
Minimum clock high pulse width	t_{21}	50	80	ns max	
SDC low to data valid delay	t_{22}	150	200	ns max	Load ckt of *Figure 3.*, C_L = 20pF
		200	250	ns max	Load ckt of *Figure 3.*, C_L = 100pF

Table 4. Serial Data Output Mode Timing
(*See Figure 6.*)

$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	DB0/SDC	Comments
ADC Channel Select and Start Convert							
↓	1	0	Hi-Z	0	0	X	No operation if ADEN = 0
↓	1	1	Hi-Z	↑	0	X	Input MUX channel selected, STL set on falling edge of $\overline{WR}$
0	1	X	Hi-Z	1	0	X	MUX select disabled
↑	1	X	Hi-Z	0	↑	X	Start convert on $\overline{WR}$ rising edge
1	1	X	Hi-Z	↓	↑	X	Start convert on STL falling edge
1	1	X	Hi-Z	0	↓	X	STS goes low at end of conversion
Read ADC Data (*See Figure 6. and Table 4.*)							
1	↓	X	—	0	0	1	Serial output (SDO) and serial clock input (SDC) enabled
X	X	X	MSB (DB11)	0	0	1	MSB data available at SDO
X	0	X	DB10	0	0	↓	Next significant bit shifted out to SDO
X	0	X	DB10	0	0	0	No Operation
X	0	X	DB10	0	0	↑	No Operation
X	0	X	DB9	0	0	↓	Next significant bit shifted out to SDO
X	↑	X	Hi-Z	0	0	X	Data outputs/SDC input disabled
1	X	X	Hi-Z	0	1	X	Data outputs/$\overline{RD}$ disabled when STS = 1
⊓	0	0	Hi-Z	0	↑	1	STL, MUX select disabled when ADEN = 0
⊓	0	X	MSB (DB11)	0	↓	1	New data appears at SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 5. Logic Truth Table – Serial Data Output

2's Complement Output Code (Hexidecimal)						Ideal Transition Voltage
0111	1111	1110 (7fe) to	0111	1111	1111 (7ff)	+FS – 1 1/2 LSB
0000	0000	0000 (000) to	0000	0000	0001 (001)	0 V +1/2 LSB
1111	1111	1111 (fff) to	0000	0000	0000 (000)	0 V –1/2 LSB
1000	0000	0000(800) to	1000	0000	0001 (801)	–FS +1/2 LSB

Table 6. Key Output Codes vs. Input Voltage (2's Complement Code)

APPLICATION INFORMATION

The MP3275 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor.

Successful application of the MP3275 requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Control and Timing considerations.

Physical Layout

The 12-bit accuracy of the MP3275 represents a dynamic range of 72dB. Precautions must be taken to avoid any interfering signals, whether conducted or radiated, to assure that this is not degraded.

- Avoid placing the chip and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles. The GND Ref. is the positive terminal of the MUX/Instrumentation amplifier and will provide common mode noise rejection. It should be close to and shielded together with the channel inputs in order to take advantage of this feature.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1µF ceramic cap and a 10-47 µF tantalum type, in parallel.

"Stand-Alone" Operation

The MP3275 can be used in "stand-alone" operation, which is useful in systems not requiring full computer bus interface capability.

For this operation, $\overline{CS}$ = 0, ADEN = 1, and conversion is controlled by $\overline{WR}$. The 3-state buffer SDO is enabled when $\overline{RD}$ goes low. There are two possible conditions that the 3-state buffer could be in during a conversion. If $\overline{RD}$ goes low prior to $\overline{WR}$ the output buffer is enabled and the data from the previous conversion is available at the outputs during STL = 1. At the end of the present conversion which is initiated at the rising edge of $\overline{WR}$, STS returns low and the new conversion result is placed on the output data buffer.

If $\overline{WR}$ goes low prior to $\overline{RD}$, the data buffer remains in a high impedance state and conversion is initiated at the rising edge of $\overline{WR}$. Upon the end of the conversion the STS returns low and the conversion result is placed on the output data buffers.

Ground Reference

The ground reference pin can be used for remote ground sensing of a common mode input signal with a maximum 6 V p-p around AGND.

This common input can also be used to dither each input's "zero". By averaging multiple conversions digitally, higher resolution for each input conversion can be obtained. Patterns for this dither can be a ramp, a stair step, or white noise.

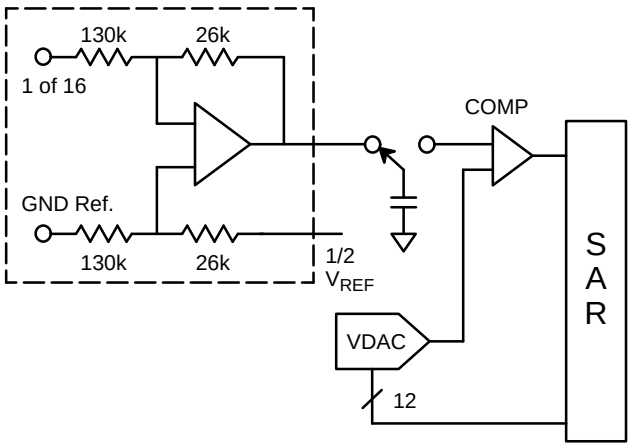


Figure 7. Equivalent Input Circuit

Quasi Differential Sampling

Method 1

For remote ground sensing where the remote ground does not change more than ±3 V from the A/D ground, connect GND Ref to the remote ground.

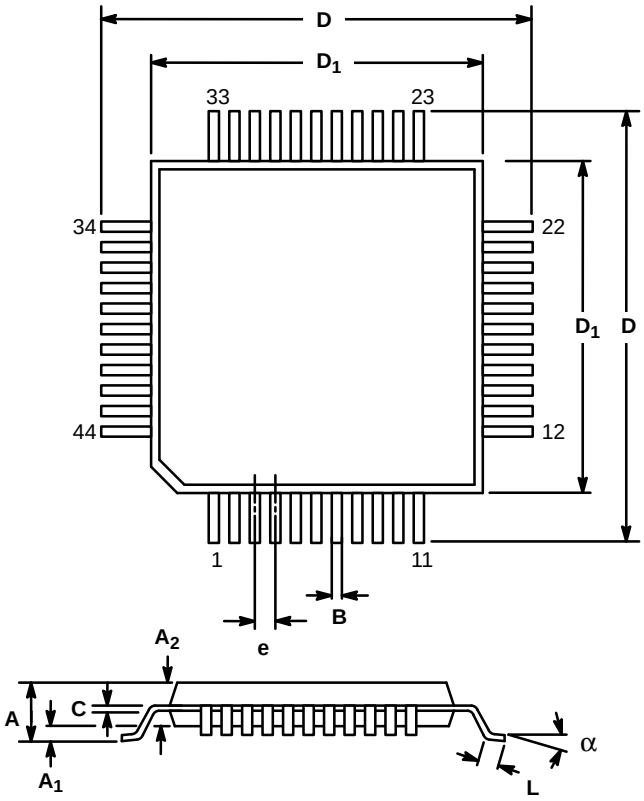
Method 2

Where Method 1 applies to each channel or group of channels, add a mux to allow connecting the appropriate ground to GND Ref.

Method 3

Use two parts. Tie both GND Ref pins together and connect this node to the "common" remote GND. Control the sample point by connecting each STL through an "OR" gate whose output is "NAND" connect with WR (inverted $\overline{WR}$). Use this output as $\overline{WR}$ to both $\overline{WR}$ inputs. By controlling the $\overline{WR}$, sample delay differences between the two converters is minimized. Two parts from the same date code will further minimize this difference. Treat one A/D as the (+) terminal and the other as the (–) terminal of the differential signal. Now the difference can be taken digitally.

44 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q44



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	1.00 BSC		0.039 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

Notes

Notes

Notes

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