MP3320A

4-Channel, Charge Pump RGB LED Driver with I²C Interface

DESCRIPTION

The MP3320A is a 4-channel, self-adaptive, charge pump RGB LED driver that operates across a wide 1.8V to 5.5V input voltage (V_{IN}) range. Each channel can reach a maximum current of up to 51mA and a maximum output voltage (V_{OUT}) of up to 5.5V.

The MP3320A integrates an I²C interface with up to 16 configurable I²C addresses via an external resister. Each channel can be enabled or disabled through the I²C.

The MP3320A employs both separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel, as well as 10-bit PWM dimming and 8-bit analog dimming for each channel. Phase shift is also integrated during PWM dimming to reduce inrush current and eliminate audible noise.

To ensure system reliability, the MP3320A integrates rich protections including LED open protection, LED short protection, over-voltage protection (OVP), and over-temperature protection.

The MP3320A is available in a QFN-14 (2mmx2mm) package.

FEATURES

- 1.8V to 5.5V Input Voltage (V_{IN}) Range
- 5.5V Max Output Voltage (V_{OUT})
- 4 Channels, Max 51mA/Ch
- Enable/Disable for Each Channel
- Internal, Self-Adaptive Charge Pump
- Charge Pump Auto-Transfer Rate: 1x, 1.5x, and 2x
- 8-Bit Analog Dimming for Each Channel
- 10-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Configurable PWM Dimming Frequency (f_{PWM})
- 400kHz I²C-Compatible Interface
- Configurable Phase Shift
- High Efficiency
- LED Open Protection and LED Short Protection
- Over-Voltage Protection (OVP)
- Over-Temperature Protection
- Available in a QFN-14 (2mmx2mm) Package

APPLICATIONS

- Wearable Devices
- LED Indicators
- Smart and Intelligent Devices

TYPICAL APPLICATION

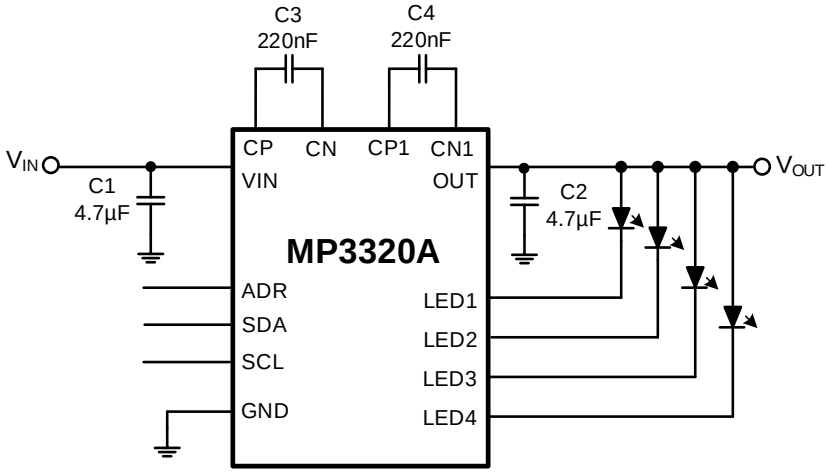


Figure 1: Typical Application Circuit (V_{IN} Is Not Sufficient to Drive LED1 to LED4)

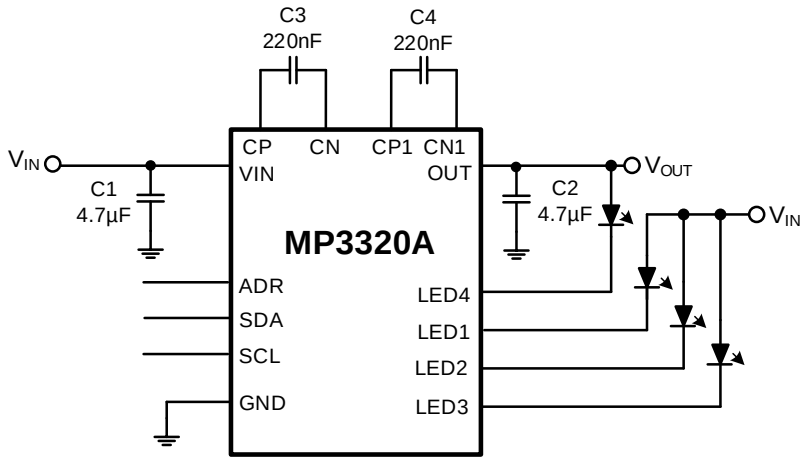


Figure 2: Typical Application Circuit (V_{IN} Is Sufficient to Drive LED1 to LED3 but Insufficient to Drive LED4)

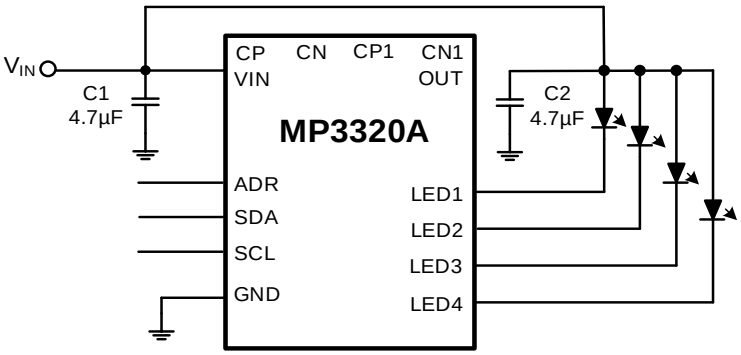


Figure 3: Typical Application Circuit (V_{IN} Is Sufficient to Drive LED1 to LED4)

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3320AGG	QFN-14 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP3320AGG-Z).

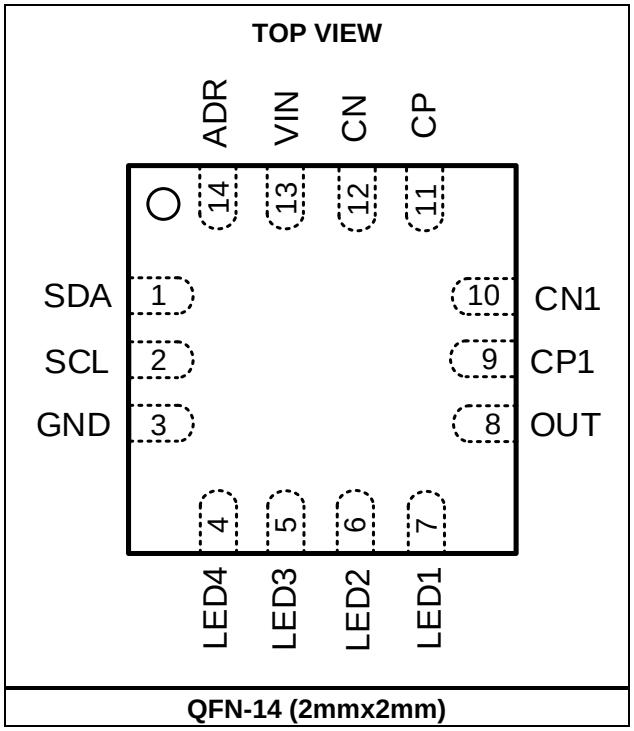
TOP MARKING

LPY

LLLL

LP: Product code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SDA	**I²C interface data input/output.**
2	SCL	**I²C interface clock input.**
3	GND	**Ground.**
4	LED4	**Channel 4's white LED current input.** Connect the LED channel 4 cathode to this pin.
5	LED3	**Channel 3's blue LED current input.** Connect the LED channel 3 cathode to this pin.
6	LED2	**Channel 2's green LED current input.** Connect the LED channel 2 cathode to this pin.
7	LED1	**Channel 1's red LED current input.** Connect the LED channel 1 cathode to this pin.
8	OUT	**Charge pump output.**
9	CP1	**Charge pump flying capacitor terminal 1.**
10	CN1	**Charge pump flying capacitor terminal 2.**
11	CP	**Charge pump flying capacitor terminal 3.**
12	CN	**Charge pump flying capacitor terminal 4.**
13	VIN	**Input power supply.** Place a bypass capacitor close to the VIN pin.
14	ADR	**I²C address setting.** Configure the I²C addresses by connecting a resistor between ADR and GND.

ABSOLUTE MAXIMUM RATINGS (1)

All pins ..... -0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-14 (2mmx2mm) 1.56W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 1.8V to 5.5V
LED load ..... <5V
Operating junction temp ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14 (2mmx2mm)……..80……..16...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Operating input voltage	V_{IN}		1.8		5.5	V
Standby current	I_{STB}	V_{IN} = 5.5V, I²C is enabled, EN = 0, no switching		1500	2000	nA
Quiescent current	I_Q	V_{IN} = 3.7V, EN = 1, no switching		1	1.5	mA
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge			1.8	V
V_{IN} UVLO hysteresis				110		mV
Charge Pump Block						
Switching frequency	f_{SW}	FSW[2:0] = 100b	0.9	1	1.1	MHz
MOSFET on resistance	$R_{DS(ON)}$	V_{IN} = 2.5V		0.9		Ω
LED Current Regulation						
LED current accuracy	I_{LED}	PWMx[10:0] = 0x400, ICHx[7:0] = 0x64	19.5	20	20.5	mA
		PWMx[10:0] = 0x400, ICHx[7:0] = 0x01		0.2		mA
LED current matching (5)		PWMx[10:0] = 0x400, ICHx [7:0] = 0x64		0.75		%
Pulse-width modulation (PWM) dimming frequency	f_{PWM}	DMBLK = 0, FPWM[7:0] = 0x10	-10%	1.95	+10%	kHz
PWM dimming pulse width	t_{PWM_MIN}	DMBLK = 0, FPWM[7:0] = 0x10, ICHx[7:0] = 0xC8 PWMx[10:0] = 0x002		1		µs
Blinking frequency	f_{BLK}	DMBLK = 1, CH4MD = 1, FBLK[7:0] = 0x20	-10%	1.907	+10%	Hz
Blinking pulse width	t_{BLK_MIN}	DMBLK = 1, CH4MD = 1, FBLK[7:0] = 0x20, DUTYBLK[7:0] = 0x01		16		ms
LED regulation headroom voltage	V_{HD}	I_{LED} = 20mA		300		mV
Protections						
LED short protection threshold	V_{SLP}	SLP[1:0] = 10b	2.8	3	3.2	V
LED short protection delay time	t_{SLP}			24		ms
Short protection delay time of all enabled LED channels (6)	t_{SLP_ALL}			100		ms
LED open protection threshold	V_{LED_UVP}		50	80	110	mV
LED open protection delay time	t_{OLP}			24		ms
Over-voltage protection (OVP) threshold	V_{OVP}	Rising edge	5	5.5	6	V
OVP hysteresis		Hysteresis		500		mV
Over-temperature protection threshold	T_{ST}	Rising edge		150		°C
	T_{ST_HYS}	Hysteresis		25		°C

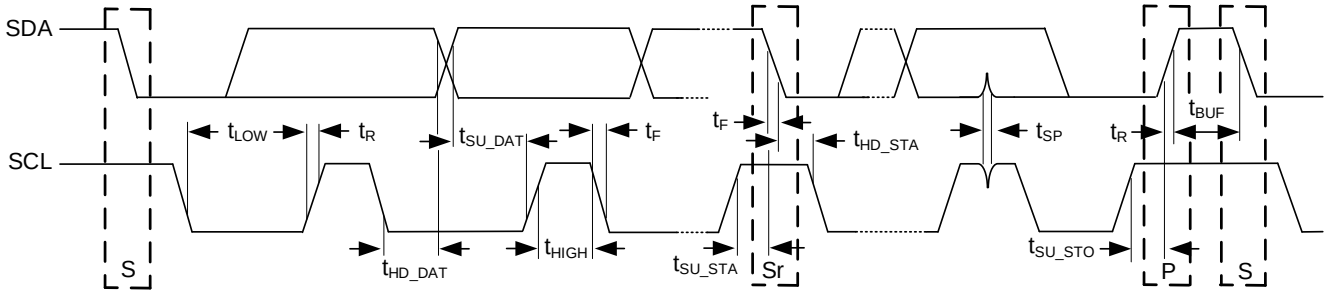
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} =3.7V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface						
Input logic low	V_{IL}				0.99	V
Input logic high	V_{IH}		2.31			V
Output logic low (6)	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (6)	f_{SCL}				400	kHz
SCL high time (6)	t_{HIGH}		0.26			µs
SCL low time (6)	t_{LOW}		0.5			µs
Data set-up time (6)	t_{SU_DAT}		50			ns
Data hold time (6)	t_{HD_DAT}		0			µs
Set-up time for a repeated start condition (6)	t_{SU_STA}		0.26			µs
Hold time for a start condition (6)	t_{HD_STA}		0.26			µs
Bus free time between a start and a stop condition (6)	t_{BUF}		0.5			µs
Set-up time for a stop condition (6)	t_{SU_STO}		0.26			µs
Rise time of SCL and SDA (6)	t_R				120	ns
Fall time of SCL and SDA (6)	t_F				120	ns
Pulse width of suppressed spike (6)	t_{SP}		0		50	ns
Capacitance for each bus line (6)	C_B				400	pF

Notes:

5) Matching is defined as the difference between the maximum current and minimum current, divided by 2 times the average current.
6) Not tested in production. Guaranteed by characterization.



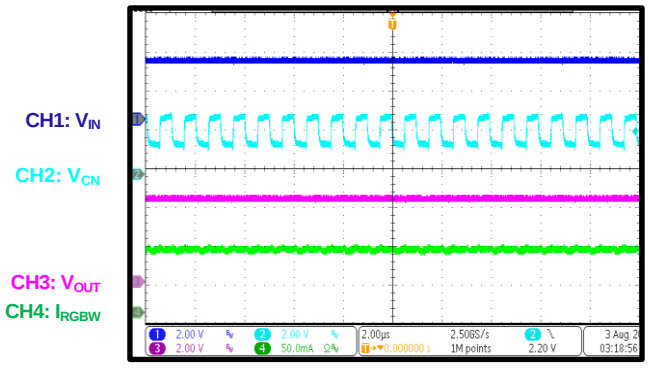
S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

Figure 4: I²C-Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

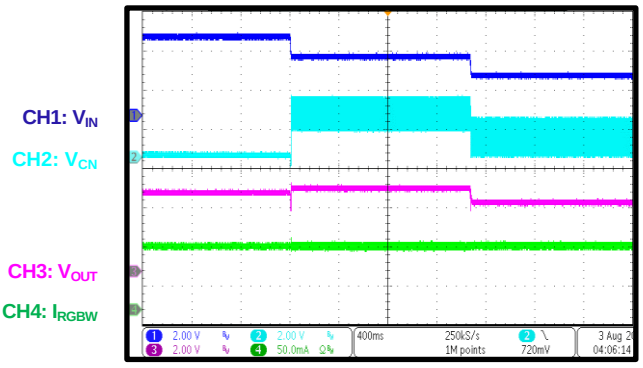
V_{IN} = 3V, RGBW LED load = 20mA/channel, self-adaptive charge pump mode, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

Steady State



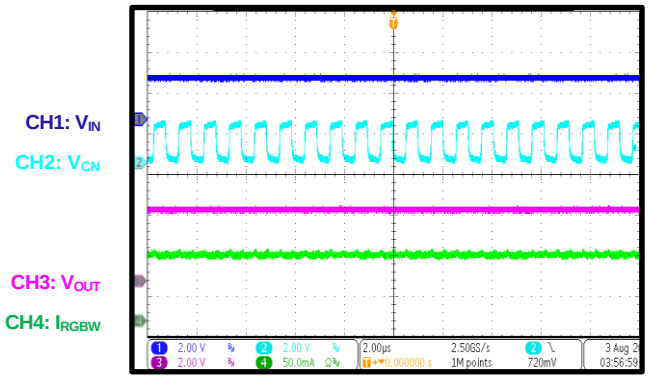
Steady State

V_{IN} changes from 4V to 3V to 2V

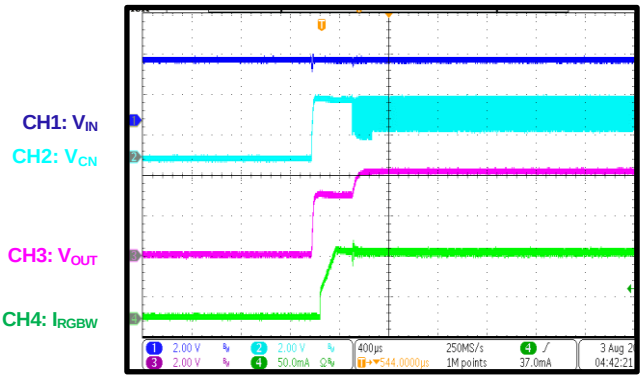


Steady State

Fixed charge pump mode (V_{OUT} = 2 x V_{IN}), V_{IN} = 2V

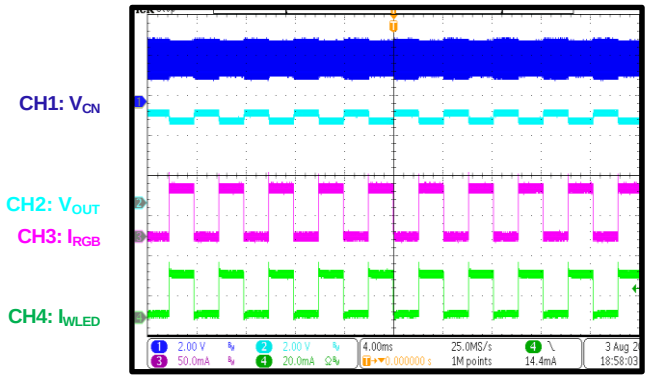


Start-Up through EN



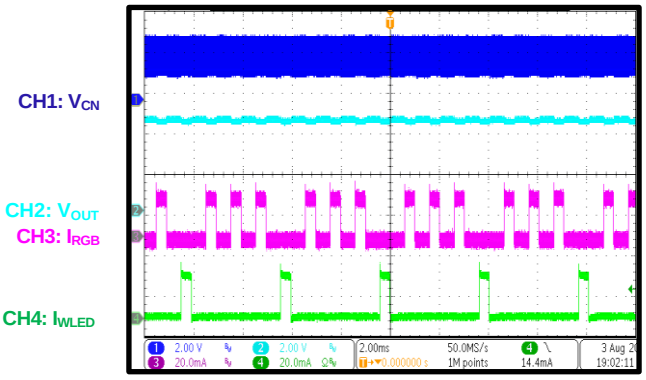
PWM Dimming

f_{PWM} = 244Hz, D_{PWM} = 50%



PWM Dimming with Phase Shift

f_{PWM} = 244Hz, D_{PWM} = 10%, 90° phase shift

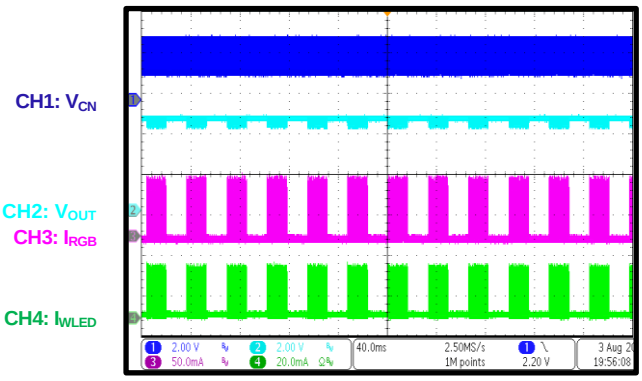


TIPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3V, RGBW LED load = 20mA/channel, self-adaptive charge pump mode, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

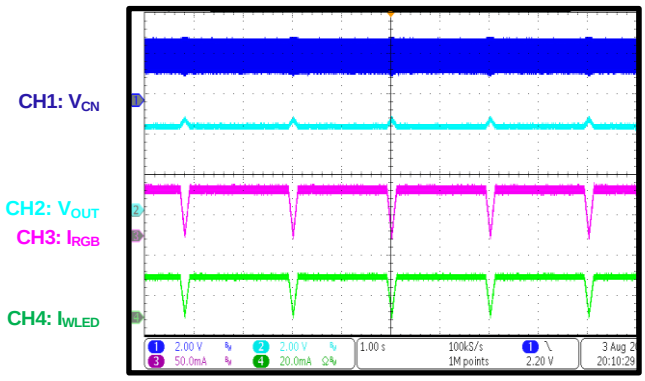
Blinking Mode

f_{PWM} = 1.95kHz, D_{PWM} = 50%, all channels blinking (30Hz/50% infinitely)



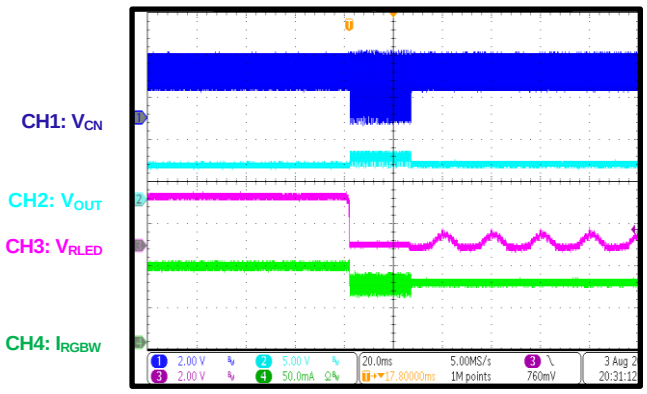
Breathing Light Mode

D_{PWM} = 100%, all channels blinking (0.5Hz/95% infinitely), t_{STEP_UP} = t_{STEP_DOWN} = 1ms/step



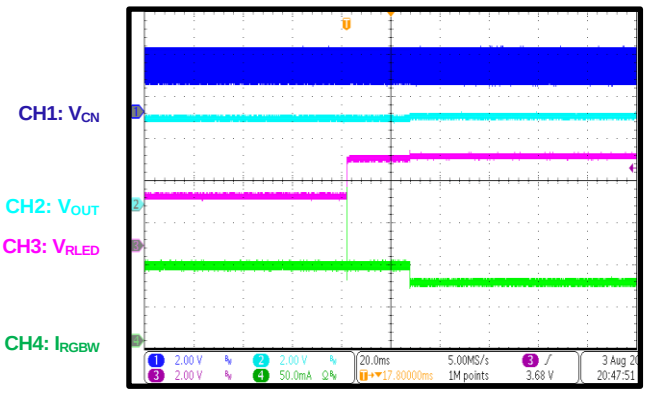
LED Open Protection

OLP_MD[1:0] = 10b, open RLED under normal operation



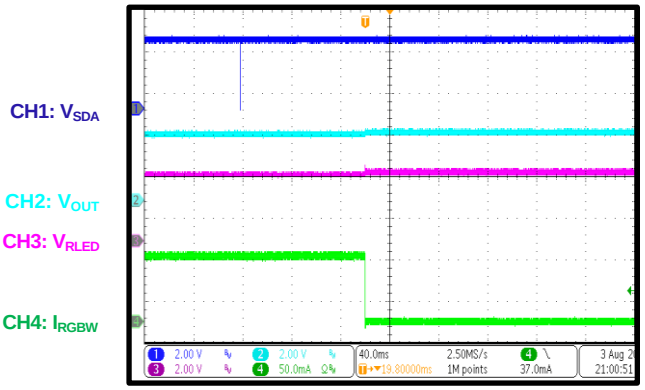
LED Short Protection

SLP_MD[1:0] = 10b, short RLED under normal operation



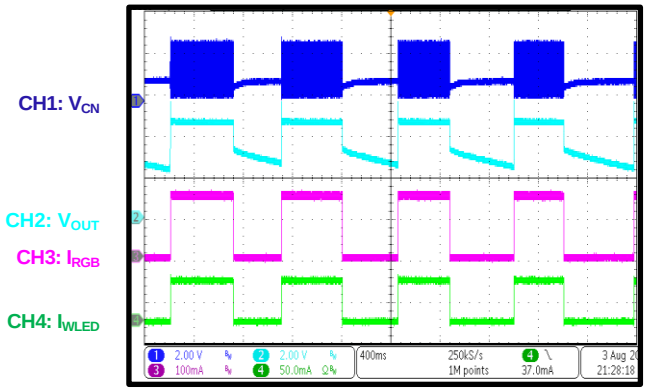
Short All LED Protections

V_{IN} = 3.3V, short RGBW LED, change SLP_MD[1:0] from 00b to 10b



Over-Temperature Protection

50mA/channel



FUNCTIONAL BLOCK DIAGRAM

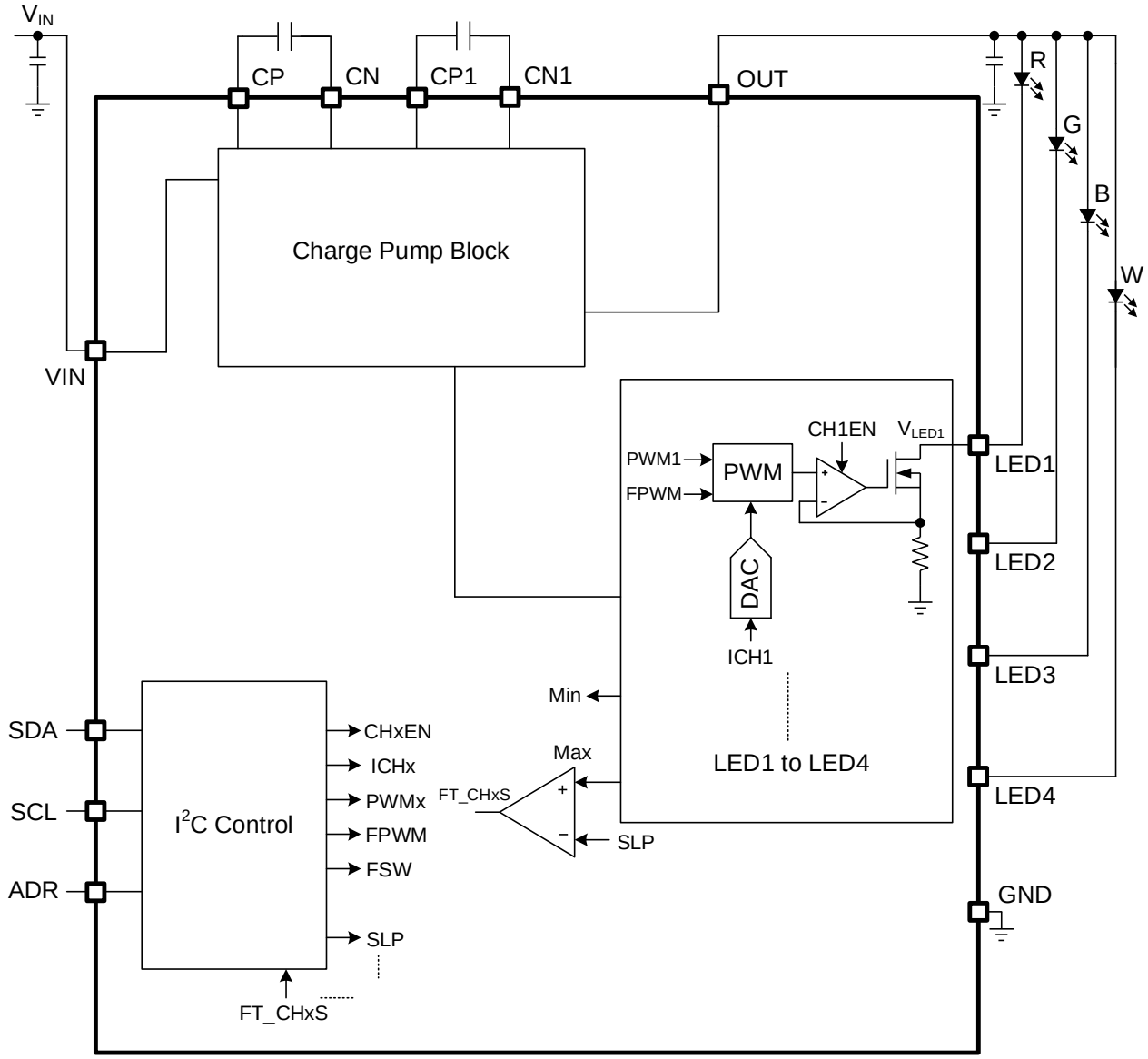


Figure 5: Functional Block Diagram

OPERATION

The MP3320A is a RGBW LED driver that integrates a self-adaptive charge pump block and an I²C interface, and is ideal for LED indicators and smart device lighting. The device has up to 4 channels of regulated current sources with 8-bit analog dimming and 10-bit pulse-width modulation (PWM) dimming.

System Start-Up

When the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold, the MP3320A enters standby mode and the I²C is enabled. Set the EN bit high to enable the IC and start up the system.

Channel Selection

The four channels can be enabled by setting the corresponding CHxEN bit (where x = 1, 2, 3, or 4) high; the channels can be disabled by setting the corresponding CHxEN low. If V_{IN} significantly exceeds channel x's LED forward voltage, set the CLEDx bit (where x = 1, 2, 3, or 4) high to directly connect the anode to VIN and select the corresponding channel as a pure current source without requiring loop control.

Charge Pump Converter

The MP3320A integrates a self-adaptive charge pump block that can be configured to work in different modes when enabled. Figure 6 shows the charge pump block's structure diagram.

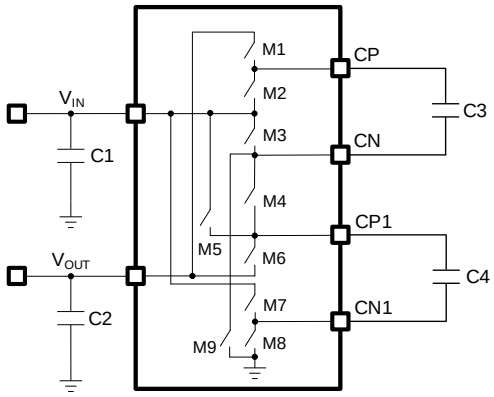


Figure 6: Charge Pump Block Structure Diagram

Enable and Disable

Set the EN_CP bit high to enable the charge pump block; set EN_CP low to disable the charge pump block. If disabled, the output voltage (V_{OUT}) is disconnected from the IC's internal input voltage (V_{IN}) and M1~M9 turn off. Once V_{IN} is sufficiently high to drive the LED load of all the enabled channels and VIN is externally connected to the LED channel anodes, EN_CP can be reset to disable the charge pump block and the corresponding CLEDx bit (where x = 1, 2, 3, or 4) can be set to use all the enabled channels as pure current sources.

Fixed Charge Pump Mode

VOUT[1:0] sets the charge pump mode. If VOUT[1:0] = 01b (V_{OUT} = V_{IN}), V_{IN} is directly connected to V_{OUT}. Figure 7 shows the equivalent circuit of VOUT[1:0] = 01b.

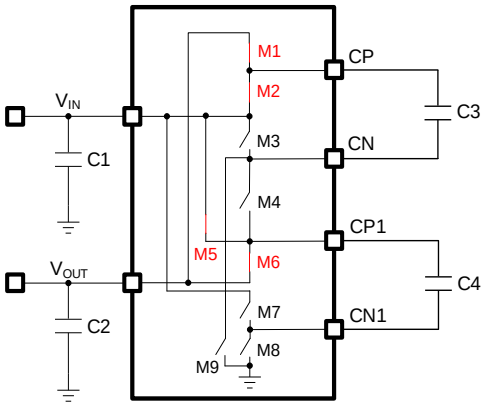


Figure 7: VOUT[1:0] = 01b Equivalent Circuit

If VOUT[1:0] = 10b (V_{OUT} = 1.5 x V_{IN}), there are two phases in each switching cycle. In phase 1, V_{IN} charges C3 and C4 in series, and C2 supplies power to the load (see Figure 8).

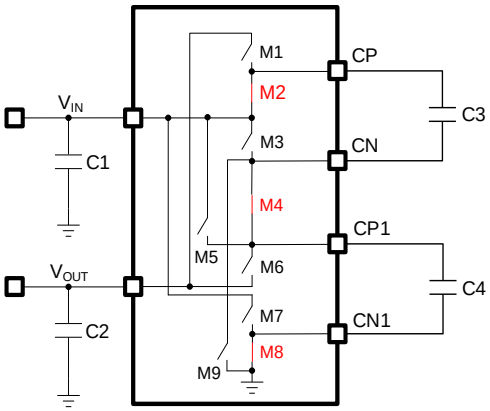


Figure 8: Phase 1 of VOUT[1:0] = 10b Equivalent Circuit

In phase 2, V_{IN} connects C3 or C4 in series to charge C2 and supply power to the load (see Figure 9 on page 11).

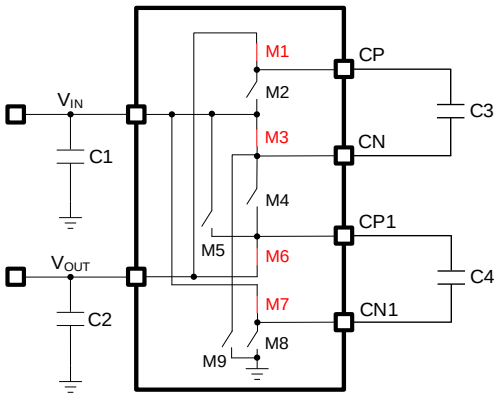


Figure 9: Phase 2 of VOUT[1:0] = 10b Equivalent Circuit

If VOUT[1:0] = 11b (V_{OUT} = 2 x V_{IN}), there are also two phases in each switching cycle. In phase 1, V_{IN} charges C3 and connects C4 in series to charge C2 and supply power to the load (see Figure 10).

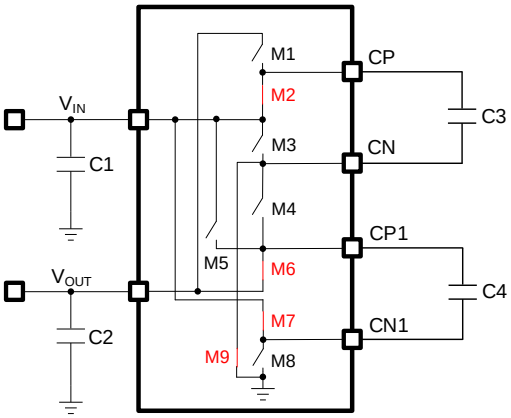


Figure 10: Phase 1 of VOUT[1:0] = 11b Equivalent Circuit

In phase 2, V_{IN} charges C4 and connects C3 in series to charge C2 and supply power to the load (see Figure 11).

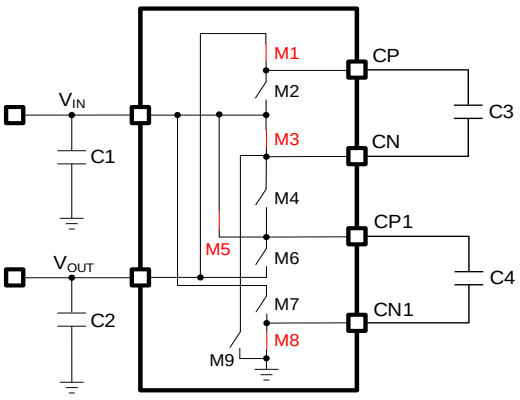


Figure 11: Phase 2 of VOUT[1:0] = 11b Equivalent Circuit

For fixed charge pump mode, a suitable voltage rate must be selected to prevent V_{OUT} from repeatedly reaching the over-voltage protection (OVP) threshold.

Self-Adaptive Charge Pump Mode

If VOUT[1:0] = 00b, the charge pump block works in self-adaptive mode, where the initial conversion rate is 1x when the system starts up. The converter then automatically selects the lowest active headroom voltage (V_{LEDx_MIN}) of CHxEN = 1 and CLEDx = 0 as the feedback voltage to regulate the conversion rate.

If V_{LEDx_MIN} is below 0.3V, the conversion rate rises a step. For example, a 1x current rate rises to 1.5x, and a 1.5x current rate rises to 2x. If V_{LEDx_MIN} exceeds 0.5 x V_{IN} + 0.5V, the conversion rate decreases by a step. For example, a 1.5x current rate drops to 1x, and a 2x current rate drops to 1.5x.

If V_{OUT} reaches the OVP threshold five times and each time interval is less than 1ms, then the conversion rate decreases by a step.

Dimming and Blinking Control

Dimming Control

The MP3320A supports independent analog and PWM dimming for each channel, where each channel has an 8-bit analog dimming register and 10-bit PWM dimming register.

For analog dimming, channel x's LED current (I_{LEDx}) varies with the I_{LEDx} setting register value. Adjust the code of ICHx[7:0] (where x = 1, 2, 3, or 4) to achieve the corresponding channel's analog dimming. I_{LEDx} can be calculated with Equation (1):

$$I_{LEDx} = 0.2 \times ICHx[7:0]\ (mA) \quad (1)$$

If ICH1[7:0] = 0x64, channel 1's current amplitude is 20mA.

Figure 12 shows analog dimming for the RGBW LED.

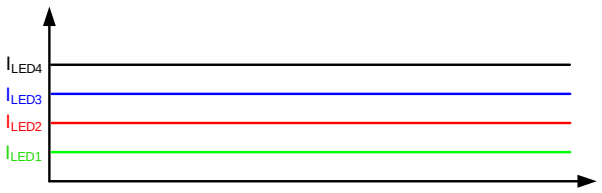


Figure 12: Analog Dimming for RGBW LED

During PWM dimming, I_{LEDx} is chopped. The I_{LEDx} amplitude remains unchanged while the I_{LEDx} duty (D_{ILEDx}) varies with the PWM duty setting register, PWMx[10:0] (where x = 1, 2, 3, or 4). The PWMx[10:0] range is from 0x000 to 0x400. D_{ILEDx} can be calculated with Equation (2):

$$D_{ILEDx} = \frac{PWMx[10:0]}{1024} \quad (2)$$

The PWM dimming frequency (f_{PWM}) can be selected by FPWM[7:0]. The default is FPWM[7:0] = 0x10 with a 1.95kHz corresponding f_{PWM}.

Figure 13 shows the simultaneous application of analog dimming and PWM dimming for the RGBW LED.

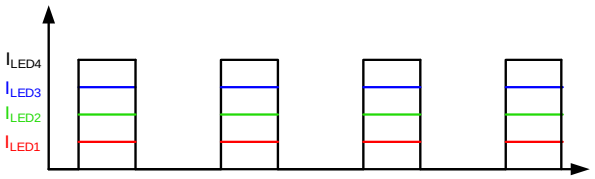


Figure 13: Analog and PWM Dimming for RGBW LED

Blinking Control

The MP3320A supports blinking control. Table 1 shows the blinking mode register configuration.

Table 1: Blinking Mode Register Configuration

CH4MD	Blinking Mode Register Configuration			
	DMBLK = 0b		DMBLK = 1b	
	CH1~3	CH4	CH1~3	CH4
0b	No blinking		Blinking	No blinking
1b	No blinking		Blinking	Blinking

For blinking control, the blinking frequency (f_{BLK}) can be set with FBLK[7:0] and calculated using Equation (3):

$$f_{BLK} = \frac{1}{t_{BLK}} = \frac{1}{16.384ms \times FBLK[7:0]} \quad (3)$$

The blinking on time (t_{BLK_ON}) can be set with DUTYBLK[7:0] and calculated using Equation (4):

$$t_{BLK\_ON} = 16.384 \times DUTYBLK[7:0] \ (ms) \quad (4)$$

Consider when FBLK[7:0] = 0x20 and DUTYBLK[7:0] = 0x03, f_{BLK} is about 1.9Hz and the blinking duty is about 10%. If t_{BLK_ON} exceeds the blinking period (t_{BLK}), the actual blinking duty is 100% and there is no blinking effect.

Figure 14 shows all four channels working in PWM and analog dimming modes while blinking.

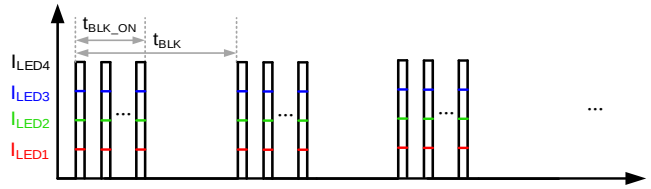


Figure 14: PWM Dimming, Analog Dimming, and Blinking for RGBW LED

Figure 15 shows channel 1, channel 2, and channel 3 working in both dimming and blinking mode, meanwhile channel 4 works in dimming mode without blinking.

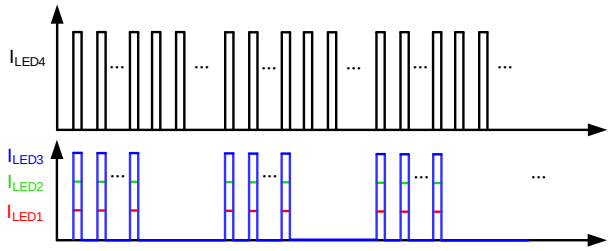


Figure 15: PWM Dimming, Analog Dimming, and Blinking for RGB LED vs. Dimming Without Blinking for WLED

BLK_TIMES[7:0] sets the blinking cycles. If BLK_TIMES[7:0] = 0x00, the MP3320A continues to operate in blinking mode. If BLK_TIMES[7:0] = 0xFF, the blinking lasts for 255 cycles. Once the blinking ends, the IC remains in dimming mode if BLK_PWM = 1b or enters standby mode if BLK_PWM= 0b.

Breathing Light

To achieve a breathing effect, all four channels must work in blinking mode (DMBLK = 1b, CH4MD = 1b) and the I_{LEDx} duty must reach 100% (PWMx[10:0] = 0x400, where x = 1, 2, 3, or 4). Under these conditions, STEP_UP[3:0] and STEP_DOWN[3:0] can be configured to achieve the breathing effect.

In breathing mode, t_{BLK_ON} begins from the first step-up moment to the first step-down moment. If the required total time from the first step-up moment to the I_{LEDx} amplitude exceeds t_{BLK_ON}, I_{LEDx} steps down from the present value once t_{BLK_ON} ends.

If I_{LEDx} does not step down to 0 until the end of one blinking cycle, I_{LEDx} steps up from the present value in the next blinking cycle.

Figure 16 shows I_{LEDx} under the breathing light.

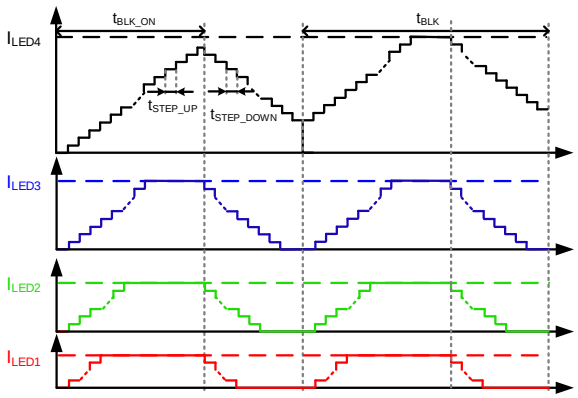


Figure 16: I_{LEDx} under Breathing Light

Phase Shift

The MP3320A integrates phase shift to eliminate audible noise and reduce inrush current in PWM dimming. The phase shift function is enabled by setting PS[1:0]. When the phase shift function is enabled, the rising edge sequence of I_{LED1} to I_{LED4} follows: channel 4, channel 3, channel 2, channel 1. The PS[1:0] setting determines the shifted phase, described below:

- If PS[1:0] = 00b, phase shift is disabled.
- If PS[1:0]= 01b, phase shift is enabled and the shifted phase is 90°.
- If PS[1:0]= 10b, phase shift is enabled and the shifted phase is 120°.
- If PS[1:0] = 11b, phase shift is enabled and the shifted phase is 180°.

Note that the rising edge sequence and shifted phase of I_{LED1} to I_{LED4} remain unchanged even when certain channels are disabled. When PS[1:0] = 01b and channel 2 is disabled, the I_{LED1} rising edge delays 180° after the I_{LED3} rising edge.

Protections

The MP3320A integrates LED open protection, LED short protection, OVP, and over-temperature protection. All channels include a corresponding LED open and LED short fault indicator bit.

LED Open Protection

LED open protection is achieved by detecting the LEDx (where x = 1, 2, 3, or 4) voltage (V_{LEDx}). V_{LEDx} drops when an LED is open. If V_{LEDx} drops below the LED open protection threshold and lasts for 24ms, LED open protection is triggered by setting OLP_MD [1:0]. Once an LED open protection is triggered, the IC has different actions depending on the OLP_MD[1:0] setting, described below:

- If OLP_MD[1:0] = 00b, the IC has no action.
- If OLP_MD[1:0] = 01b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4).
- If OLP_MD[1:0] = 10b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4), and turns off the fault channel.
- If OLP_MD[1:0] = 11b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4) and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.

LED Short Protection

The MP3320A monitors V_{LEDx} to determine whether a LED short fault occurs. If one or more LED strings are shorted, the LEDx pins tolerate high voltage stress. If V_{LEDx} exceeds the LED short protection threshold (configured by SLP[1:0]) and lasts for 24ms, LED short protection is triggered. If V_{LEDx} of all the enabled channels exceed the protection threshold, LED short protection can be triggered only when this fault condition lasts for 100ms. Once an LED short protection is triggered, the IC has different actions depending on the SLP_MD[1:0] setting, described below:

- If SLP_MD[1:0] = 00b, the IC has no action.
- If SLP_MD[1:0] = 01b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4).
- If SLP_MD[1:0] = 10b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4), and turns off the fault channel.

- If SLP_MD[1:0] = 11b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4) and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.

Over-Temperature Protection

To prevent the IC from operating at an exceedingly high temperature, over-temperature protection is implemented by detecting the silicon die temperature. If the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down and resumes normal operation when the die temperature drops below the lower threshold. Typically, the hysteresis value is 25°C.

One-Time Programmable (OTP) Memory

The MP3320A can change the register default values one time via the one-time programmable (OTP) memory function. MPS can provide a custom default value with a different -3320A suffix.

I²C INTERFACE

I²C Chip Address

The device address of the 7 most signifcant bits (MSB) is 0x60~0x6F, where A3~A0 is configured via an ADR resistor (R_{ADR}). Table 2 shows the various R_{ADR} ranges and recommended R_{ADR} configurations to set the I²C address.

Table 2: I²C ADR Resistor vs. Device Address

R_{ADR} Range (1% Accuracy) (kΩ)	Recommended R_{ADR} (kΩ)	I²C Address (A3A2A1A0)
<0.97	0	0000
1.7~2.9	2.2	0001
3.8~4.8	4.3	0010
5.8~6.8	6.2	0011
7.8~8.8	8.2	0100
9.9~11.4	11	0101
12.6~14	13	0110
15.3~17.3	16	0111
18.7~21.2	20	1000
22.8~25.8	24	1001
27.6~32.3	30	1010
34.4~38.8	36	1011
41.2~46.7	43	1100
49.3~71.5	62	1101
75.2~89.8	82	1110
>95	>150 or floating	1111

Figure 17 shows an I²C-compatible device address, where A0~A3 is configured by the ADR pin. After a start (S) condition, the I²C-compatible master sends a 7-bit address, followed by an eighth data direction bit (where 1 = read and 0 = write).

1	1	0	A3	A2	A1	A0	R/W

Figure 17: I²C-Compatible Device Address

I²C REGISTER MAP (7)

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
00h	00h	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01h	07h	NC	NC	NC	DMBLK	EN	CH4MD	BLK_ PWM	EN_CP
02h	20h	VOUT1	VOUT0	FSW2	FSW1	FSW0	NC	NC	NC
03h	0Fh	CLED4	CLED3	CLED2	CLED1	CH4EN	CH3EN	CH2EN	CH1EN
04h	11h	STEP_ UP3	STEP_ UP2	STEP_ UP1	STEP_ UP0	STEP_ DOWN3	STEP_ DOWN2	STEP_ DOWN1	STEP_ DOWN0
05h	10h	FPWM7	FPWM6	FPWM5	FPWM4	FPWM3	FPWM2	FPWM1	FPWM0
06h	20h	FBLK7	FBLK6	FBLK5	FBLK4	FBLK3	FBLK2	FBLK1	FBLK0
07h	03h	DUTY BLK7	DUTY BLK6	DUTY BLK5	DUTY BLK4	DUTY BLK3	DUTY BLK2	DUTY BLK1	DUTY BLK0
08h	00h	BLK_ TIMES7	BLK_ TIMES6	BLK_ TIMES5	BLK_ TIMES4	BLK_ TIMES3	BLK_ TIMES2	BLK_ TIMES1	BLK_ TIMES0
09h	A8h	SLP_MD1	SLP_MD0	OLP_MD1	OLP_MD0	SLP1	SLP0	PS1	PS0
0Ah	64h	ICH1[7:0]							
0Bh	64h	ICH2[7:0]							
0Ch	64h	ICH3[7:0]							
0Dh	64h	ICH4[7:0]							
0Eh	00h	NC					PWM1[2:0]		
0Fh	80h	PWM1[10:3]							
10h	00h	NC					PWM2[2:0]		
11h	80h	PMW2[10:3]							
12h	00h	NC					PWM3[2:0]		
13h	80h	PWM3[10:3]							
14h	00h	NC					PWM4[2:0]		
15h	80h	PMW4[10:3]							
16h	00h	FT_CH4S	FT_CH3S	FT_CH2S	FT_CH1S	FT_CH4O	FT_CH3O	FT_CH2O	FT_CH1O

Note:

7) All registers have a configurable OTP memory by default.

I²C REGISTER DESCRIPTION

REG00h: Device ID Register

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ID[7:0]	R	00	Enables the device ID.

REG01h: Blinking Mode Setting Register

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:5	RESERVED	R/W	3’b000	Reserved. Do not change the default value.
4	DMBLK	R/W	1’b0	Sets the dimming or blinking mode. 1’b0: Dimming mode 1’b1: Blinking mode
3	EN	R/W	1’b0	Enables the IC. After changing the EN bit from 1b to 0b, set a delay time that is longer than 1.5ms before performing other I²C read or write operations. 1’b0: Standby mode 1’b1: Enabled
2	CH4MD	R/W	1’b1	Enables channel 4 in blinking mode. 1’b0: Channel 4 does not work in blinking mode, and follows PWM dimming and analog dimming. 1’b1: If DMBLK = 1, channel 1 to channel 4 work in blinking mode; if DMBLK = 0, channel 1 to channel 4 do not work in blinking mode.
1	BLK_PWM	R/W	1’b1	Sets the operation mode after blinking completes. 1’b0: IC enters standby mode after blinking completes. 1’b1: IC follows PWM and analog dimming after blinking completes.
0	EN_CP	R/W	1’b1	Enables the charge pump block. 1’b0: Disabled 1’b1: Enabled When the charge pump block is disabled, channel 1 to channel 4 can only work in pure current source mode.

REG02h: Charge Pump Mode Setting Register

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	VOUT[1:0]	R/W	2’b00	Sets the charge pump mode. 2’b00: Minimum active V_{LEDx} control 2’b01: 1x 2’b10: 1.5x 2’b11: 2x
5:3	FSW[2:0]	R/W	3’b100	Sets the charge pump switching frequency (f_{SW}). 3’b000: 200kHz 3’b001: 400kHz 3’b010: 666kHz 3’b011: 800kHz 3’b100: 1MHz 3’b101: 1.33MHz 3’b110~3’b111: Reserved
2:0	RESERVED	R/W	3’b000	Reserved. Do not change the default value.

REG03h: Channel Setting Register

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CLED4	R/W	1’b0	Sets channel 4 to operate white LED in pure current source. 1’b0: Connects to the boost control loop 1’b1: Channel 4 works in pure current source
6	CLED3	R/W	1’b0	Sets channel 3 to operate blue LED in pure current source. 1’b0: Connects to the boost control loop 1’b1: Channel 3 works in pure current source
5	CLED2	R/W	1’b0	Sets channel 2 to operate green LED in pure current source. 1’b0: Connects to the boost control loop 1’b1: Channel 2 works in pure current source
4	CLED1	R/W	1’b0	Sets channel 1 to operate red LED in pure current source. 1’b0: Connects to the boost control loop 1’b1: Channel 1 works in pure current source
3	CH4EN	R/W	1’b1	Enables channel 4. 1’b0: Disables channel 4 1’b1: Enables channel 4
2	CH3EN	R/W	1’b1	Enables channel 3. 1’b0: Disables channel 3 1’b1: Enables channel 3
1	CH2EN	R/W	1’b1	Enables channel 2. 1’b0: Disables channel 2 1’b1: Enables channel 2
0	CH1EN	R/W	1’b1	Enables channel 1. 1’b0: Disables channel 1 1’b1: Enables channel 1

REG04h: Step-Up and Step-Down Time Setting Register

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	STEP_UP [3:0]	R/W	4’b0001	Sets the current step-up time (µs/step). 4’b0001: 2µs 4’b0010: 4µs 4’b0011: 8µs 4’b0100: 16µs 4’b0101: 32µs 4’b0110: 64µs 4’b0111: 128µs 4’b1000: 256µs 4’b1001: 512µs 4’b1010: 1ms 4’b1011: 2ms 4’b1100: 4ms 4’b1101: 8ms 4’b1110: 16ms 4’b1111: 32ms
3:0	STEP_DOWN [3:0]	R/W	4’b0001	Sets the current step-down time (µs/step). 4’b0001: 2µs 4’b0010: 4µs 4’b0011: 8µs 4’b0100: 16µs 4’b0101: 32µs 4’b0110: 64µs 4’b0111: 128µs 4’b1000: 256µs 4’b1001: 512µs 4’b1010: 1ms 4’b1011: 2ms 4’b1100: 4ms 4’b1101: 8ms 4’b1110: 16ms 4’b1111: 32ms

REG05h: PWM Dimming Frequency Setting Register

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	FPWM[7:0]	R/W	10	Sets the PWM dimming frequency (f_{PWM}). In dimming mode (DMBLK = 0), f_{PWM} can be set according to the following register values: 01: 31.25kHz 02: 15.625kHz 03: 10.42kHz 04: 7.81kHz 05: 6.25kHz 06: 5.2kHz 07: 4.46kHz 08: 3.906kHz 10: 1.95kHz 18: 1.30kHz 20: 976Hz 28: 781Hz 30: 651Hz 38: 558Hz 40: 488Hz 48: 434Hz 50: 390Hz 58: 355Hz 60: 325Hz 68: 300Hz 70: 279Hz 78: 260Hz 80: 244Hz Note that when f_{PWM} > 3.906kHz (FPWM[7:0] < 0x08), the PWM dimming duty resolution is below 10 bits if the clock frequency is 4MHz.

REG06h: Blinking Frequency Setting Register

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	FBLK[7:0]	R/W	20	In blinking mode (DMBLK = 1), the blinking frequency (f_{BLK}) can be calculated with the following equation: $f_{BLK} = 1/(16.384ms \times FBLK[7:0])$ f_{BLK} can be set according to the following register values: 01: 61Hz 02: 30.5Hz 03: 20.3Hz … 20: 1.907Hz … 3D: 1Hz … 7A: 0.5Hz … FF: 0.239Hz

REG07h: Blinking Duty Setting Register

Addr: 0x07				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	DUTYBLK[7:0]	R/W	03	In blinking mode, the blinking on time (t_{BLK_ON}) can be calculated with the following equation: $t_{BLK\_ON} = 16.384 \times DUTYBLK[7:0]$ (ms) If DUTYBLK[7:0] = 0x03 and FBLK[7:0] = 0x20, the blinking duty is about 10%.

REG08h: Blinking Cycles Setting Register

Addr: 0x08				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	BLK_TIMES [7:0]	R/W	00	Sets the blinking cycles. 00: Infinitely runs in blinking mode 01: 1 cycle 02: 2 cycles 03: 3 cycles … FF: 255 cycles

REG09h: Protection and Phase Shift Setting Register

Addr: 0x09				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	SLP_MD[1:0]	R/W	2’b10	Sets the IC action after triggering LED short protection. 2’b00: No action 2’b01: Sets corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4) 2’b10: Sets corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4), and turns off the fault channel 2’b11: Sets corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4), and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.
5:4	OLP_MD[1:0]	R/W	2’b10	Sets the IC action after triggering LED open protection. 2’b00: No action 2’b01: Sets corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4) 2’b10: Sets corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4), and turns off the fault channel 2’b11: Sets corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4), and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.
3:2	SLP[1:0]	R/W	2’b10	Sets the LED short protection threshold. 2’b00: 2V 2’b01: 2.5V 2’b10: 3V 2’b11: 3.5V
1:0	PS[1:0]	R/W	2’b00	Sets the phase shift function. 2’b00: No phase shift 2’b01: 90° phase shift 2’b10: 120° phase shift 2’b11: 180° phase shift

REG0Ah: Channel 1 LED Current Amplitude Setting Register

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ICH1[7:0]	R/W	64	Sets the channel 1 I_{LED} amplitude, where I_{LED1} can be calculated with the following equation: $I_{LED1} = 0.2 \times ICH1[7:0]$ (mA) Where if the ICH1[7:0] value increases by one step, then I_{LED1} increases by 0.2mA. The default value is 20mA.

REG0Bh: Channel 2 LED Current Amplitude Setting Register

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ICH2[7:0]	R/W	64	Sets the channel 2 I_{LED} amplitude, where I_{LED2} can be calculated with the following equation: $I_{LED2} = 0.2 \times ICH2[7:0]$ (mA) Where if the ICH2[7:0] value increases by one step, then I_{LED2} increases by 0.2mA. The default value is 20mA.

REG0Ch: Channel 3 LED Current Amplitude Setting Register

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ICH3[7:0]	R/W	64	Sets the channel 3 I_{LED} amplitude, where I_{LED3} can be calcuated with the following equation: $I_{LED3} = 0.2 \times ICH3[7:0]$ (mA) Where if the ICH3[7:0] value increases by one step, then I_{LED3} increases by 0.2mA. The default value is 20mA.

REG0Dh: Channel 4 LED Current Amplitude Setting Register

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ICH4[7:0]	R/W	64	Sets the channel 4 I_{LED} amplitude, where I_{LED4} can be calculated with the following equation: $I_{LED4} = 0.2 \times ICH4[7:0]$ (mA) Where if the ICH4[7:0] value increases by one step, then I_{LED4} increases by 0.2mA. The default value is 20mA.

REG0Eh and REG0Fh: Channel 1 LED Current PWM Dimming Duty Setting Register

Addr: 0x0E and 0x0F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
2:0 7:0	PWM1[10:0]	R/W	00 80	Sets the channel 1 I_{LED} PWM dimming duty (D_{ILED1}), which can be calculated with the following equation: D_{ILED1} = PWM1[10:0] / 1024 Where the default duty is 100%. PWM1[2:0] is valid after PWM1[10:3] is written.

REG10h and REG11h: Channel 2 LED Current PWM Dimming Duty Setting Register

Addr: 0x10 and 0x11				
Bits	**Bit Name**	**Access**	**Default**	**Description**
2:0 7:0	PWM2[10:0]	R/W	00 80	Sets the channel 2 I_{LED} PWM dimming duty (D_{ILED2}), which can be calculated with the following equation: D_{ILED2} = PWM2[10:0] / 1024 Where the default duty is 100%. PWM2[2:0] is valid after PWM2[10:3] is written.

REG12h and REG13h: Channel 3 LED Current PWM Dimming Duty Setting Register

Addr: 0x12 and 0x13				
Bits	**Bit Name**	**Access**	**Default**	**Description**
2:0 7:0	PWM3[10:0]	R/W	00 80	Sets the channel 3 I_{LED} PWM dimming duty (D_{ILED3}), which can be calculated with the following equation: D_{ILED3} = PWM3[10:0] / 1024 Where the default duty is 100%. PWM3[2:0] is valid after PWM3[10:3] is written.

REG14h and REG15h: Channel 4 LED Current PWM Dimming Duty Setting Register

Addr: 0x14 and 0x15				
Bits	**Bit Name**	**Access**	**Default**	**Description**
2:0 7:0	PWM4[10:0]	R/W	00 80	Sets the channel 4 I_{LED} PWM dimming duty (D_{ILED4}), which can be calculated with the following equation: D_{ILED4} = PWM4[10:0] / 1024 Where the default duty is 100%. PWM4[2:0] is valid after PWM4[10:3] is written.

REG16h: LED Open and Short Fault Status Indicator Register

Addr: 0x16				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	FT_CH4S	R	1’b0	Sets channel 4’s LED short protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No short fault 1’b1: Channel 4 is shorted
6	FT_CH3S	R	1’b0	Sets channel 3’s LED short protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No short fault 1’b1: Channel 3 is shorted
5	FT_CH2S	R	1’b0	Sets channel 2’s LED short protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No short fault 1’b1: Channel 2 is shorted
4	FT_CH1S	R	1’b0	Sets channel 1’s LED short protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No short fault 1’b1: Channel 1 is shorted
3	FT_CH4O	R	1’b0	Sets channel 4’s LED open protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No open fault 1’b1: Channel 4 is open
2	FT_CH3O	R	1’b0	Sets channel 3’s LED open protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No open fault 1’b1: Channel 3 is open
1	FT_CH2O	R	1’b0	Sets channel 2’s LED open protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No open fault 1’b1: Channel 2 is open
0	FT_CH1O	R	1’b0	Sets channel 1’s LED open protection fault indicator, which resets to 0 after readback or power reset. 1’b0: No open fault 1’b1: Channel 1 is open

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. C_{IN} impedance at the switching frequency (f_{SW}) should be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 4.7µF ceramic capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the output voltage ripple small and ensures feedback loop stability. C_{OUT} impedance must be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7µF ceramic capacitor is sufficient.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Place the bypass capacitor for VIN and the fly-cap capacitors as close to the MP3320A as possible to minimize the current loops.

Figure 18 shows the recommended PCB layout.

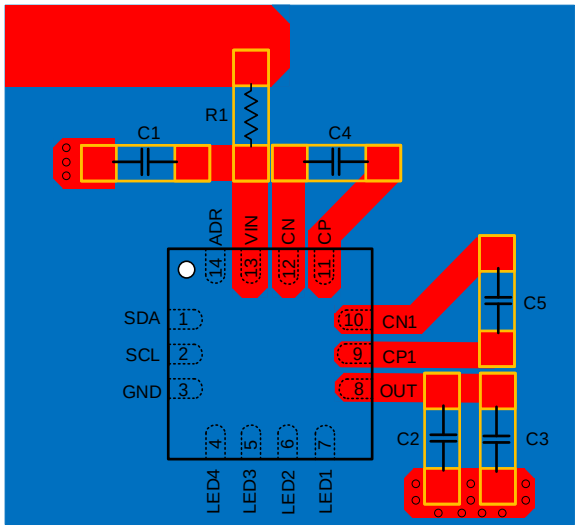


Figure 18: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

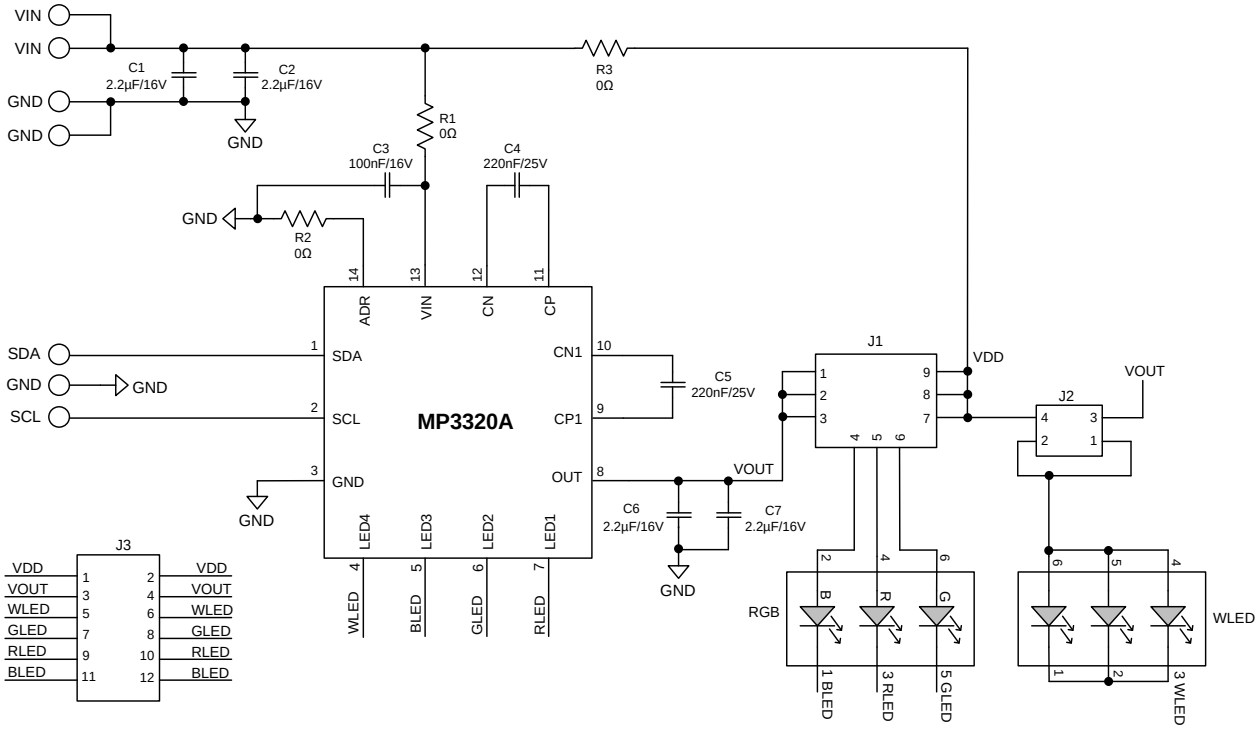
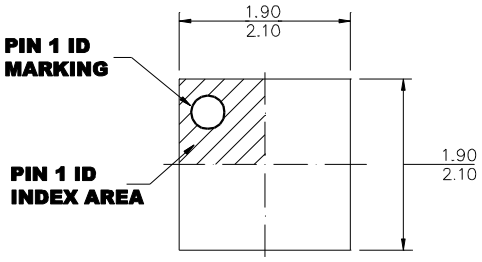


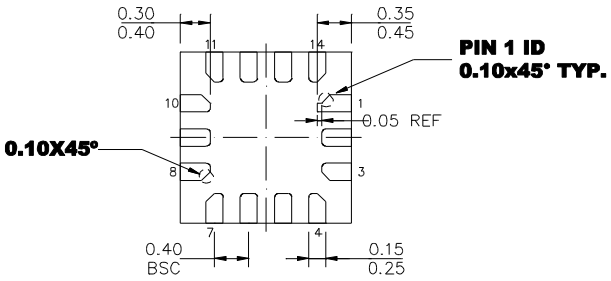
Figure 19: Typical Application Circuit

PACKAGE INFORMATION

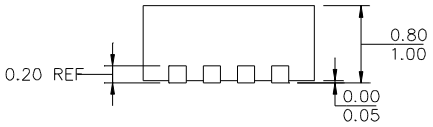
QFN-14 (2mmx2mm)



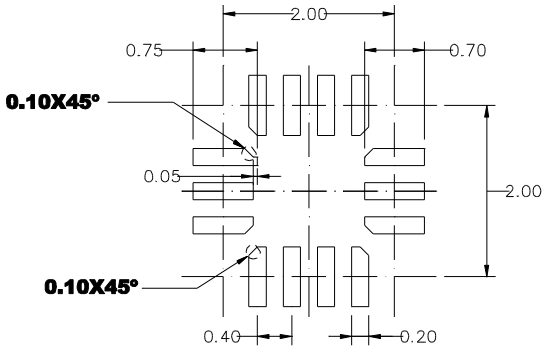
TOP VIEW



BOTTOM VIEW



SIDE VIEW

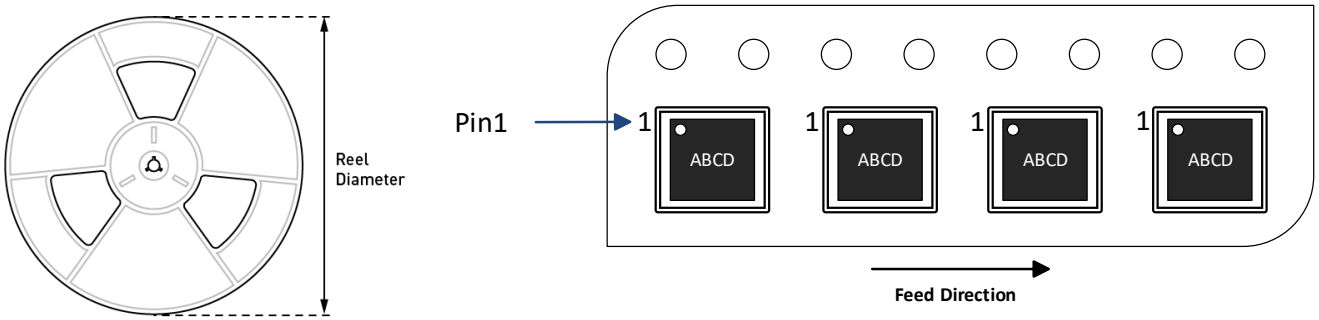


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3320AGG-Z	QFN-14 (2mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/3/2023	Initial Release	-
1.1	3/26/2024	Updated the EN bit (bit[3] of register 0x01) by adding, “After changing the EN bit from 1b to 0b, set a delay time that is longer than 1.5ms before performing other I²C read or write operations.”	17