MP3320B

4-Channel, Synchronous Boost RGBW LED Driver with I²C Interface

DESCRIPTION

The MP3320B is an 4-channel, synchronous boost RGBW LED driver that operates across a wide 2V to 5.5V input voltage voltage (V_{IN}) range. Each channel can reach a maximum current of up to 102mA and a maximum output voltage (V_{OUT}) of up to 5.4V.

The MP3320B integrates an I^2C interface with up to 16 configurable I^2C addresses via an external resistor. Each channel can be enabled or disabled via the I^2C.

The MP3320B employs both separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel, as well as 10-bit PWM dimming and 8-bit analog dimming for each channel. Phase shift is also integrated during PWM dimming to reduce inrush current and eliminate audible noise.

To ensure system reliability, the MP3320B integrates rich protections, including LED open protection, LED short protection, over-voltage protection (OVP) and over-temperature protection.

The MP3320B is available in a QFN-14 (2mmx2mm) package.

FEATURES

- 2V to 5.5V Input Voltage (V_{IN}) Range
- 5.4V Max Output Voltage (V_{OUT})
- 4 Channels, Max 102mA/Ch
- Enable/Disable for Each Channel
- Internal Synchronous Boost Converter
- 8-Bit Analog Dimming for Each Channel
- 10-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Configurable PWM Dimming Frequency (f_{PWM})
- 400kHz I^2C-Compatible Interface
- Configurable Phase Shift
- High Efficiency
- LED Open Protection and LED Short Protection
- Over-Voltage Protection (OVP)
- Over-Temperature Protection
- Available in a QFN-14 (2mmx2mm) Package

APPLICATIONS

- Wearable Devices
- LED Indicators
- Smart and Intelligent Devices

TYPICAL APPLICATION

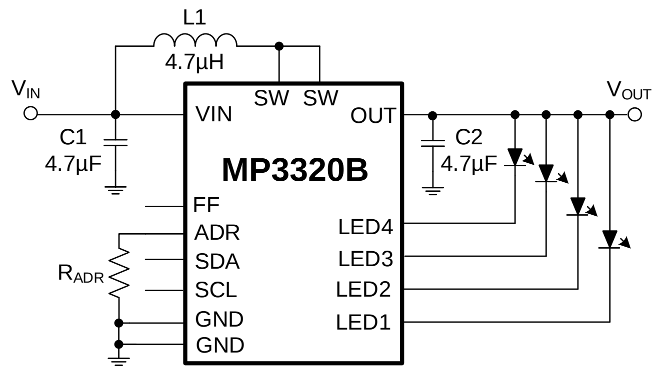


Figure 1: Typical Application (V_{IN} Is Insufficient to Drive LED1~LED4)

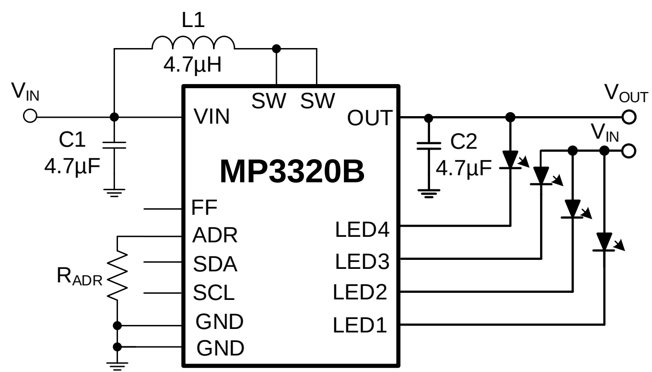


Figure 2:Typical Application (V_{IN} Is Sufficient to Drive LED1~LED3, but Insufficient to Drive LED4)

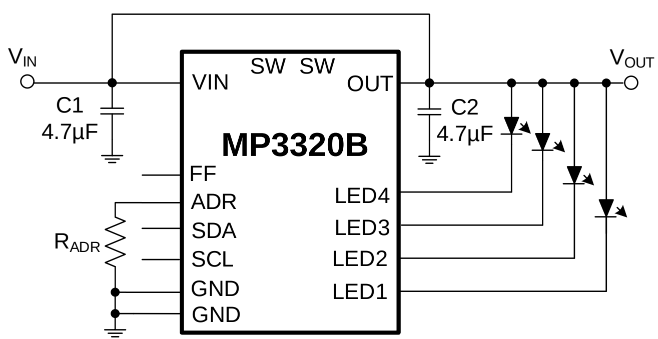


Figure 3: Typical Application (V_{IN} Is Sufficient to Drive LED1~LED4)

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3320BGG	QFN-14 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP3320BGG-Z).

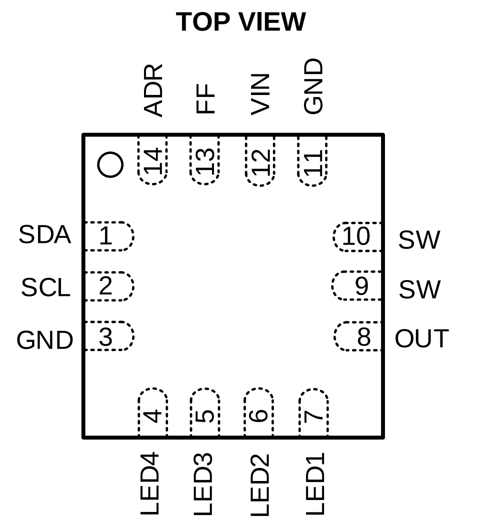
TOP MARKING

MHY

LLLL

MH: Product code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx2mm)

PIN FUNCTIONS

Pin#	Name	Description
1	SDA	**I²C interface data input/output.**
2	SCL	**I²C interface clock input.**
3, 11	GND	**Ground.**
4	LED4	**Channel 4's white LED current input.** Connect the LED channel 4 cathode to this pin.
5	LED3	**Channel 3's blue LED current input.** Connect the LED channel 3 cathode to this pin.
6	LED2	**Channel 2's green LED current input.** Connect the LED channel 2 cathode to this pin.
7	LED1	**Channel 1's red LED current input.** Connect the LED channel 1 cathode to this pin.
8	OUT	**Boost output.**
9, 10	SW	**Boost switching.** The SW pin is the drain for the internal low-side MOSFET (LS-FET).
12	VIN	**Input power supply**. Place an RC filter close to the VIN pin.
13	FF	**Fault flag.** The FF pin is an open drain during normal operation. If a fault occurs, FF is pulled low.
14	ADR	**I²C address setting.** Configure the I²C addresses by connecting a resistor between the ADR and GND pins.

ABSOLUTE MAXIMUM RATINGS (1)

All pins ....-0.3V to +6V
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-14 (2mmx2mm).............................. 1.56W

ESD Ratings

Human body model (HBM) .... ±2kV
Charged device model (CDM) .... ±2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ....2V to 5.5V
LED load ....<5V
Operating junction temp........... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14 (2mmx2mm)..............80….....16...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Operating input voltage	V_{IN}		2		5.5	V
Standby current	I_{STB}	V_{IN} = 5.5V, I²C is active, EN = 0b, no switching		1500	2000	nA
Quiescent current	I_Q	V_{IN} = 3.7V, EN = 1b, no switching		1.5	2	mA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	Rising edge			1.9	V
V_{IN} UVLO hysteresis				100		mV
Step-Up Converter						
Switching frequency	f_{SW}	FSW[2:0] = 100b	0.9	1	1.1	MHz
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)}$	V_{IN} = 2.5V		0.15		Ω
LED Current Regulation						
LED current accuracy	I_{LED}	PWMx[10:0] = 400h, ICHx[7:0] = 32h	19.5	20	20.5	mA
		PWMx[10:0] = 400h, ICHx[7:0] = E1h	87.7	90	92.3	mA
		PWMx[10:0] = 400h, ICHx[7:0] = 01h	0.36	0.4	0.44	mA
LED current matching (5)		PWMx[10:0] = 400h, ICHx[7:0] = 32h			1	%
PWM dimming frequency	f_{PWM}	FPWM[7:0] = 10h	1.73	1.95	2.17	kHz
PWM dimming pulse width	t_{PWM_MIN}	FPWM[7:0] = 10h, ICHx[7:0] = C8h, PWMx[10:0] = 002h		1		µs
Blinking frequency	f_{BLK}	DMBLK = 1b, CH4MD = 1b, FBLK[7:0] = 20h	1.7	1.907	2.3	Hz
Blinking pulse width	t_{BLK_MIN}	DMBLK = 1b, CH4MD = 1b, FBLK[7:0] = 20h, DUTYBLK[7:0] = 01h		16.384		ms
LED regulation headroom voltage	V_{HD}			450		mV
Protections						
LED short protection threshold	V_{SLP}	SLP[1:0] = 11b	3.3	3.5	3.7	V
SW current limit	I_{LIMIT}	ILIMIT[1:0] = 10b	0.8	1	1.2	A
LED short protection delay time	t_{SLP}			24		ms
All used channels short protection delay time	t_{SLP_ALL}		90	100	110	ms
LED open protection threshold	V_{LED_UVP}		60	80	100	mV
LED open protection delay time	t_{OLP}			24		ms
OVP threshold	V_{OVP}		5	5.4	5.8	V
FF pull down resister	R_{FF}	I_{LOAD} = 3mA		13		Ω
Over-temperature protection rising threshold	T_{ST}	Rising edge		150		°C
Over-temperature protection hysteresis	T_{ST_HYS}			20		°C

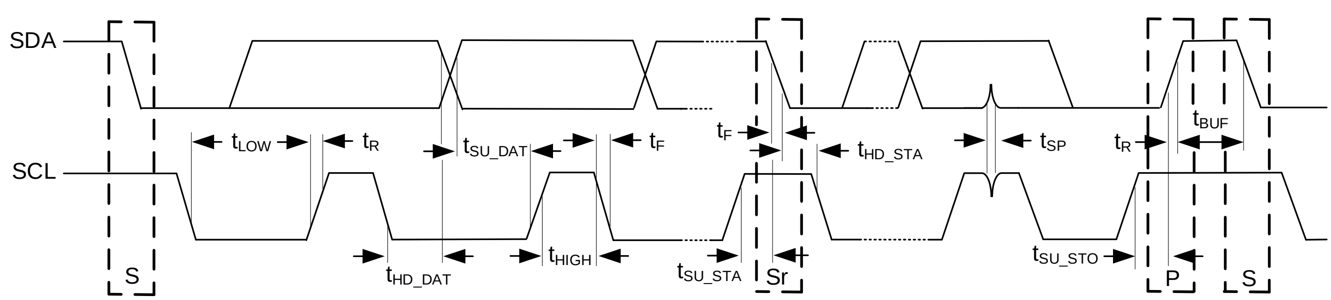
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface						
Input logic low voltage	V_{IL}				0.99	V
Input logic high voltage	V_{IH}		2.31			V
Output logic low voltage (6)	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (6)	f_{SCL}				400	kHz
SCL high time (6)	t_{HIGH}		0.26			μs
SCL low time (6)	t_{LOW}		0.5			μs
Data set-up time (6)	t_{SU_DAT}		50			ns
Data hold time (6)	t_{HD_DAT}		0			μs
Set-up time for a repeated start condition (6)	t_{SU_STA}		0.26			μs
Hold time for start condition (6)	t_{HD_STA}		0.26			μs
Bus free time between a start and a stop condition (6)	t_{BUF}		0.5			μs
Set-up time for a stop condition (6)	t_{SU_STO}		0.26			μs
Rise time of SCL and SDA (6)	t_R				120	ns
Fall time of SCL and SDA (6)	t_F				120	ns
Pulse width of suppressed spike (6)	t_{SP}		0		50	ns
Capacitance bus for each bus line (6)	C_B				400	pF

Notes:

5) Matching is defined as the difference between the maximum current and minimum current, divided by 2 times the average current.
6) Guaranteed by characterization. Not tested in production.



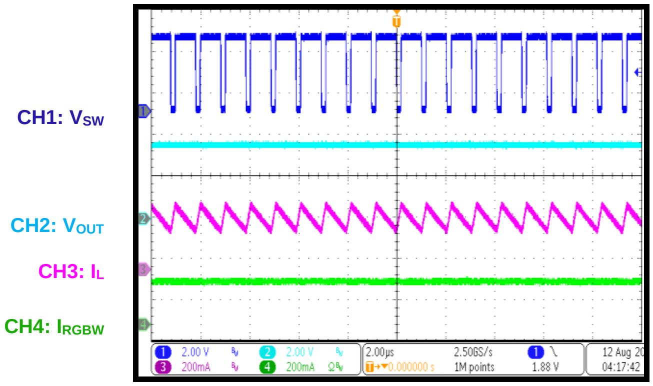
S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

Figure 4: I²C-Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

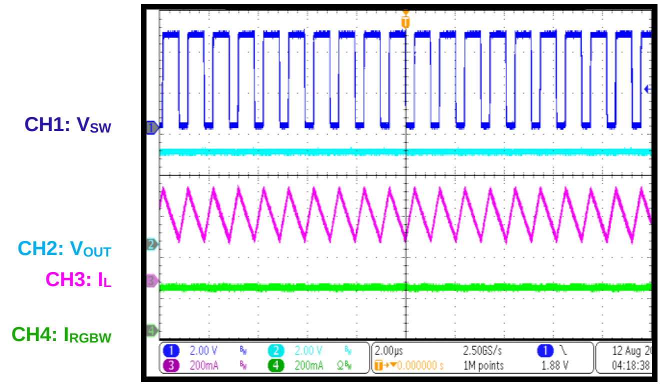
V_{IN} = 3V, RGBW LED load, 50mA/channel, adaptive mode, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

Steady State

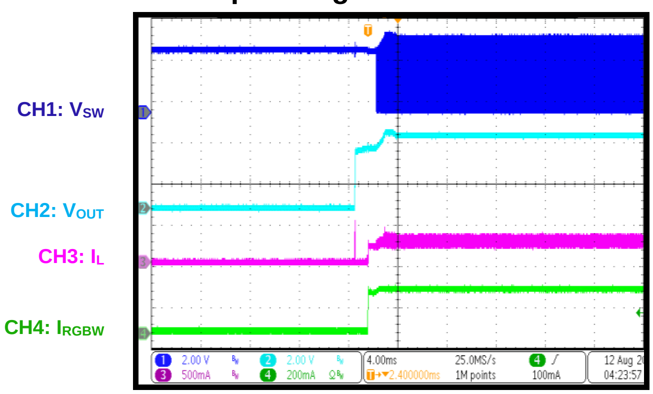


Steady State

CV mode, V_{OUT} = 4.5V

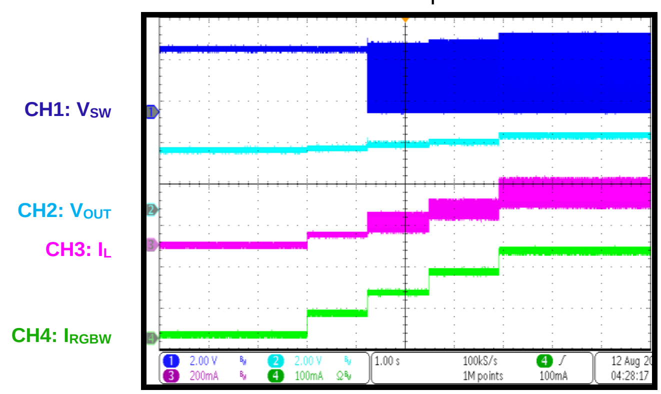


Start-Up through the EN Bit



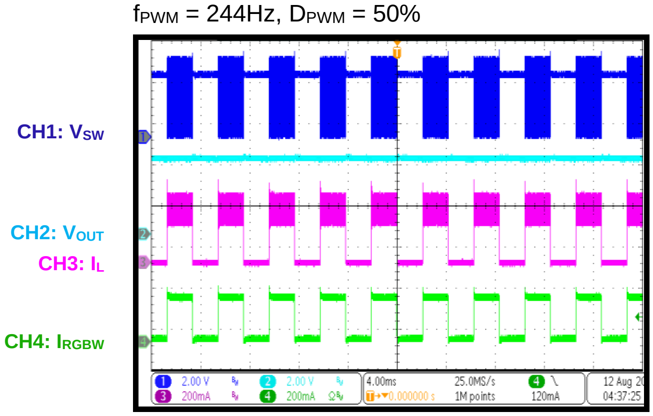
Start-Up through Channels 1~4 EN Bit

Enable channels 1~4 in sequence



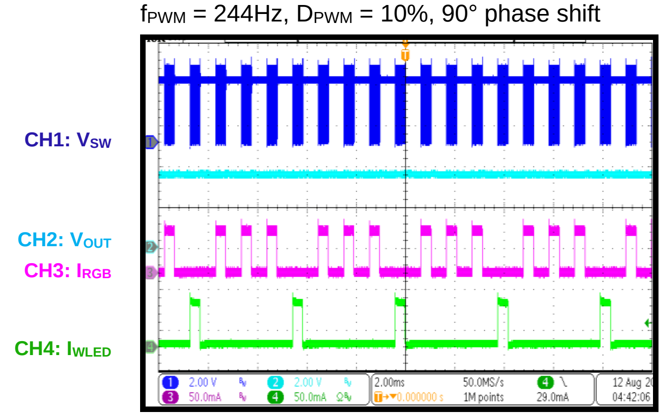
PWM Dimming

f_{PWM} = 244Hz, D_{PWM} = 50%



PWM Dimming with Phase Shift

f_{PWM} = 244Hz, D_{PWM} = 10%, 90° phase shift

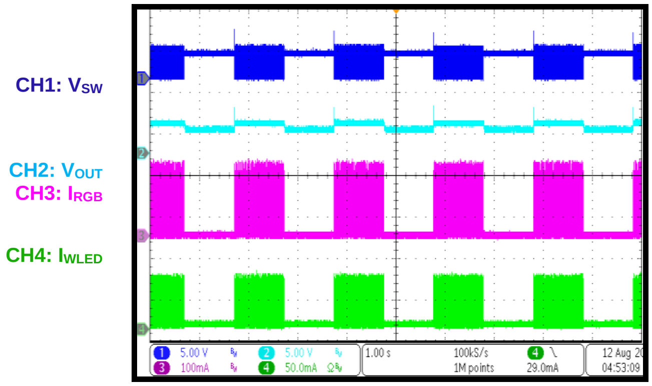


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3V, RGBW LED load, 50mA/channel, adaptive mode, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

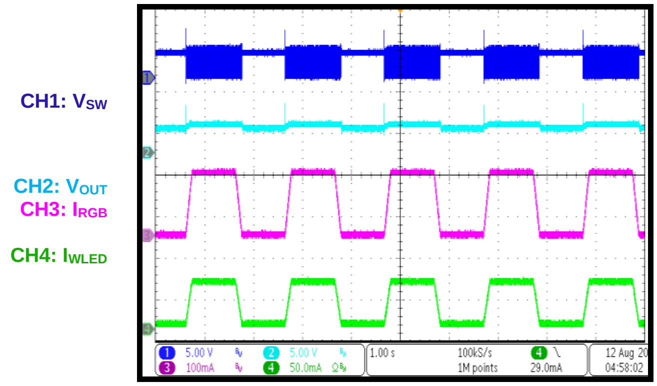
Blinking Mode

f_{PWM} = 1.95kHz, D_{PWM} = 50%, all channels blinking (0.5Hz/50%/infinitely)



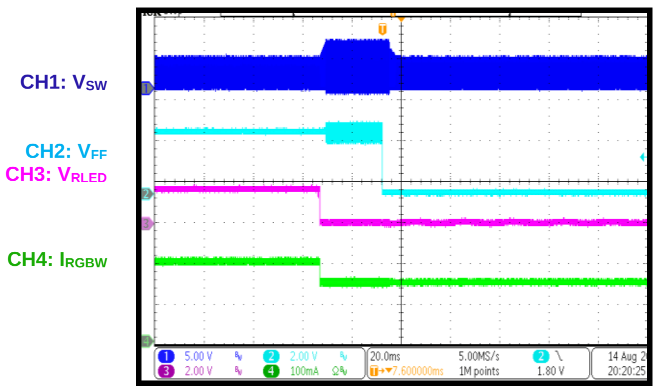
Breathing Light Mode

D_{PWM} = 100%, all channels blinking (0.5Hz/50%/infinitely), t_{STEP_UP} = t_{STEP_DOWN} = 1ms/step



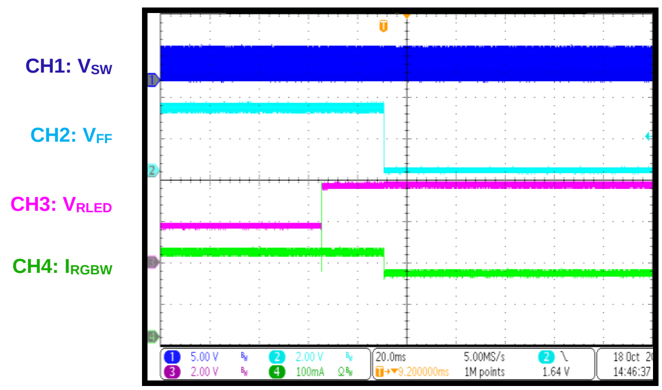
LED Open Protection

OLP_MD[1:0] = 10b, open RLED during normal operation



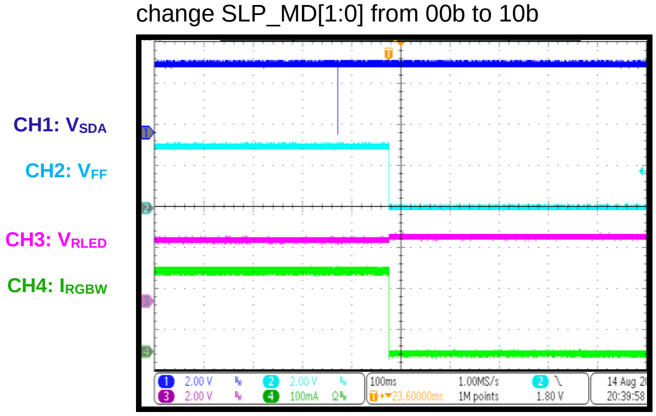
LED Short Protection

SLP_MD[1:0] = 10b, V_{SLP} = 2.5V, short RLED during normal operation

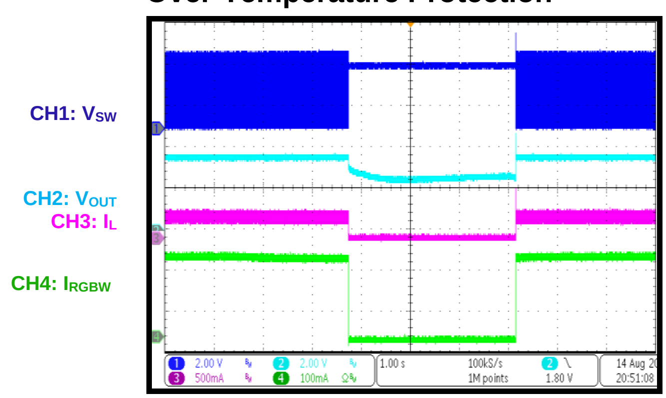


All LED Short Protection

V_{SLP} = 2.5V, short RGBW LED, change SLP_MD[1:0] from 00b to 10b



Over-Temperature Protection



FUNCTIONAL BLOCK DIAGRAM

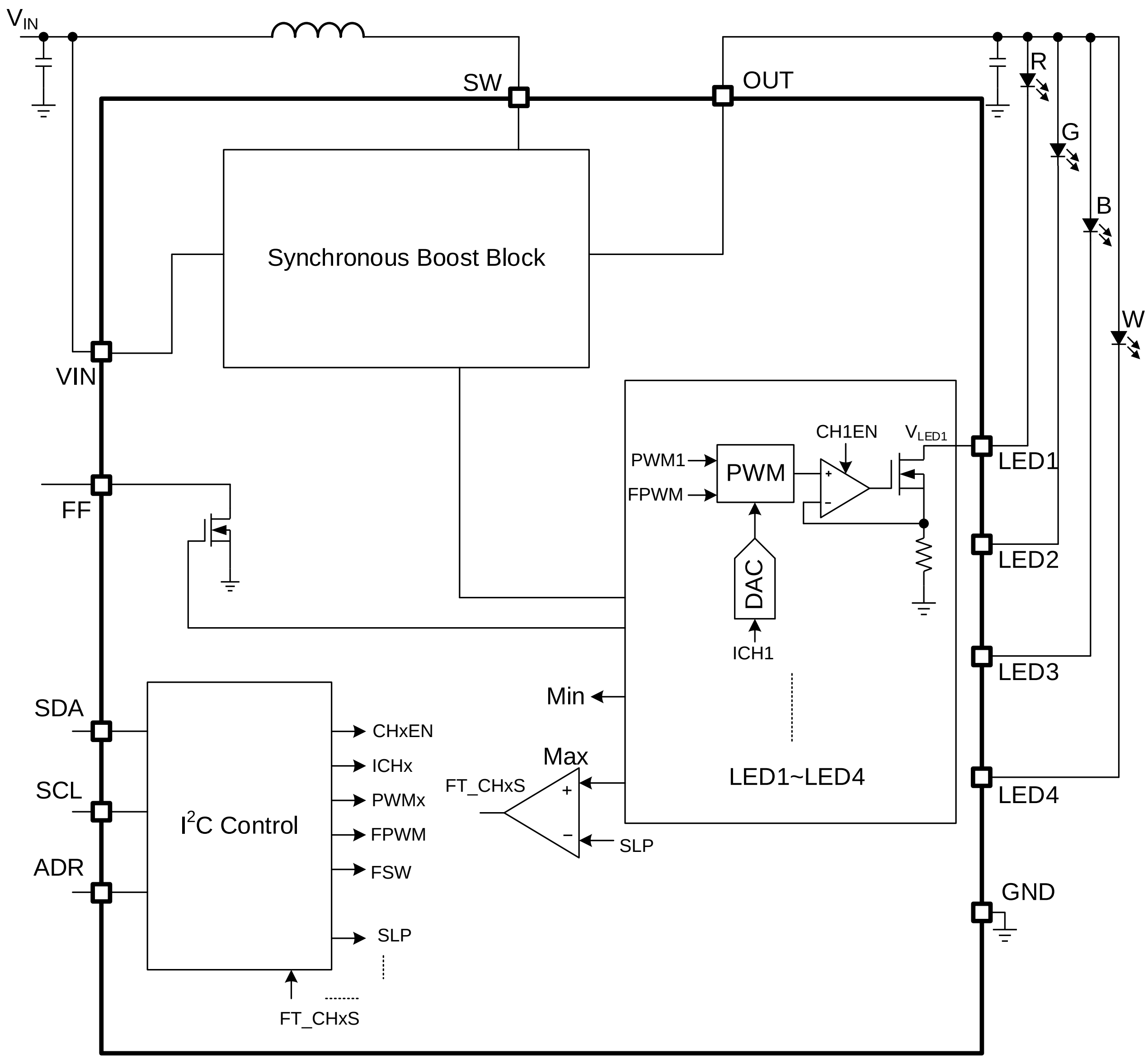


Figure 5: Functional Block Diagram

OPERATION

The MP3320B is an RGBW LED driver that integrates a synchronous boost converter, and is ideal for LED indicators and smart device lighting. The device has up to 4 channels of regulated current sources with 8-bit analog dimming and 10-bit pulse-width modulation (PWM) dimming.

System Start-Up

When the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) rising threshold, the MP3320B enters standby mode and the I^2C is enabled. Set the EN bit high to enable the IC and start up the system.

Channel Selection

The four channels can be enabled by setting the corresponding CHxEN bit (where x = 1, 2, 3, or 4) high; the channels can be disabled by setting the corresponding CHxEN low. If V_{IN} significantly exceeds channel x's LED forward voltage, set the CLEDx bit (where x = 1, 2, 3, or 4) high to directly connect the anode to VIN and select the corresponding channel as a pure current source without requiring loop control.

Step-Up Converter

The MP3320B integrates a synchronous boost block that can be configured to work in different modes when enabled.

Enable and Disable

Set the EN_BST bit high to enable the boost block; set EN_BST low to disable the boost block. Once V_{IN} is sufficiently high to drive the LED load of all the enabled channels and VIN is externally connected to the LED channel anodes, EN_BST can be reset to disable the boost block and the corresponding CLEDx bit (where x = 1, 2, 3, or 4) can be set to use all the enabled channels as pure current sources.

When the boost block is enabled, the MP3320B employs peak current mode control to regulate the output power (P_{OUT}). At the beginning of each switching cycle, the internal clock turns on the internal, N-channel low-side MOSFET (LS-FET). A stabilizing ramp is added to the current-sense amplifier's output to prevent sub-harmonic oscillations at >50% duty cycles. The summed output of the stabilizing ramp and the current-sense amplifier is fed into the PWM comparator. Once the summed voltage reaches the error amplifier's output, the LS-FET turns off.

Adaptive Mode

VOUT[1:0] sets the boost converter mode. If VOUT[1:0] = 00b, the boost converter works in adaptive mode. The converter automatically selects the lowest active LEDx voltage (V_{LEDx_MIN}) as the feedback voltage (V_{FB}) to regulate the output voltage (V_{OUT}). V_{LEDx_MIN} is monitored periodically and regulated to about 450mV.

Constant Voltage (CV) Mode

In constant voltage (CV) mode, V_{OUT} can be set at a fixed voltage, regardless of the LEDx voltage (V_{LEDx}).

- If VOUT [1:0] = 01b, then V_{OUT} = 4V.
- If VOUT [1:0] = 10b, then V_{OUT} = 4.5V.
- If VOUT [1:0] = 11b, then V_{OUT} = 5V.

Dimming and Blinking Control

Dimming Control

The MP3320B supports independent analog and PWM dimming for each channel, where each channel has an 8-bit analog dimming register and 10-bit PWM dimming register.

For analog dimming, channel x's LED current (I_{LEDx}) varies with the I_{LEDx} setting register value. Adjust the code of ICHx[7:0] (where x = 1, 2, 3, or 4) to achieve the corresponding channel's analog dimming. I_{LEDx} can be calculated with Equation (1):

$$I_{LEDx} = 0.4 \times ICHx[7:0]\ (mA) \quad (1)$$

If ICH1[7:0] = 32h, the channel 1's current amplitude is 20mA.

Figure 6 shows analog dimming for the RGBW LED.

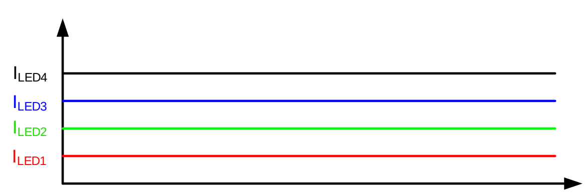


Figure 6: Analog Dimming for RGBW LED

During PWM dimming, the I_{LEDx} amplitude remains unchanged while the I_{LEDx} duty (D_{ILEDx}) varies with the PWM duty setting register, PWMx[10:0] (where x = 1, 2, 3, or 4). The PWMx[10:0] range is from 000h to 400h. D_{ILEDx} can be calculated with Equation (2):

$$D_{ILEDx} = \frac{PWMx[10:0]}{1024} \quad (2)$$

The PWM dimming frequency (f_{PWM}) can be selected by FPWM[7:0]. The default is FPWM[7:0] = 10h with a 1.95kHz corresponding f_{PWM}.

Figure 7 shows the simultaneous application of analog dimming and PWM dimming for the RGBW LED.

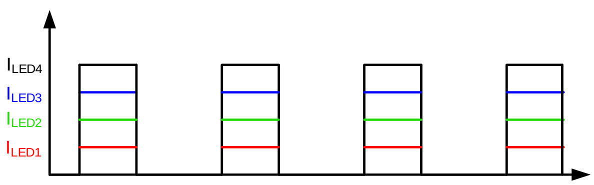


Figure 7: Analog and PWM Dimming for RGBW LED

Blinking Control

The MP3320B supports blinking control. Table 1 shows the blinking mode register configuration.

Table 1: Blinking Mode Register Configuration

CH4MD	Blinking Mode Register Configuration			
	DMBLK = 0b		DMBLK = 1b	
	CH1~3	CH4	CH1~3	CH4
0b	No blinking		Blinking	No blinking
1b	No blinking		Blinking	Blinking

For blinking control, the blinking frequency (f_{BLK}) can be set via FBLK[7:0]. f_{BLK} can be calculated with Equation (3):

$$f_{BLK} = \frac{1}{t_{BLK}} = \frac{1}{16.384ms \times FBLK[7:0]} \quad (3)$$

The blinking on time (t_{BLK_ON}) can be set via DUTYBLK[7:0]. t_{BLK_ON} can be calculated with Equation (4):

$$t_{BLK\_ON} = 16.384 \times DUTYBLK[7:0]\ (ms) \quad (4)$$

Consider when FBLK[7:0] = 20h and DUTYBLK[7:0] = 03h, f_{BLK} is about 1.9Hz and the blinking duty is about 10%. If t_{BLK_ON} exceeds the blinking period (t_{BLK}), the actual blinking duty is 100% and there is no blinking effect.

Figure 8 shows all four channels working in PWM and analog dimming modes while blinking.

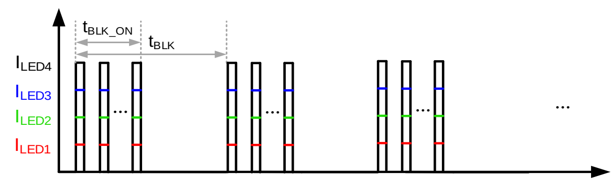


Figure 8: PWM Dimming, Analog Dimming, and Blinking for RGBW LED

Figure 9 shows channel 1, channel 2, and channel 3 working in both dimming and blinking mode, while channel 4 works in dimming mode without blinking.

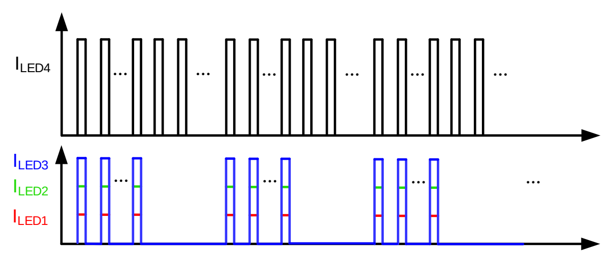


Figure 9: PWM Dimming, Analog Dimming, and Blinking for RGBW LED vs. Dimming Without Blinking for WLED

BLK_TIMES[7:0] sets the blinking cycles. If BLK_TIMES[7:0] = 00h, the MP3320B continues to operate in blinking mode. If BLK_TIMES[7:0] = FFh, the blinking lasts for 255 cycles. Once the blinking ends, the IC remains in dimming mode if BLK_PWM = 1b or enters standby mode if BLK_PWM = 0b.

Breathing Light

To achieve a breathing effect, all four channels must work in blinking mode (DMBLK = 1b, CH4MD = 1b) and the I_{LEDx} duty must reach 100% (PWMx[10:0] = 400h, where x = 1, 2, 3, or 4). Under these conditions, STEP_UP[3:0] and STEP_DOWN[3:0] can be configured to achieve the breathing effect.

In breathing mode, t_{BLK_ON} begins from the first step-up moment to the first step-down moment. If the required total time from the first step-up moment to the I_{LEDx} amplitude exceeds t_{BLK_ON},

I_{LEDx} steps down from the present value once t_{BLK_ON} ends.

If I_{LEDx} does not step down to 0 until the end of one blinking cycle, I_{LEDx} steps up from the present value in the next blinking cycle.

Figure 10 shows I_{LEDx} under the breathing light.

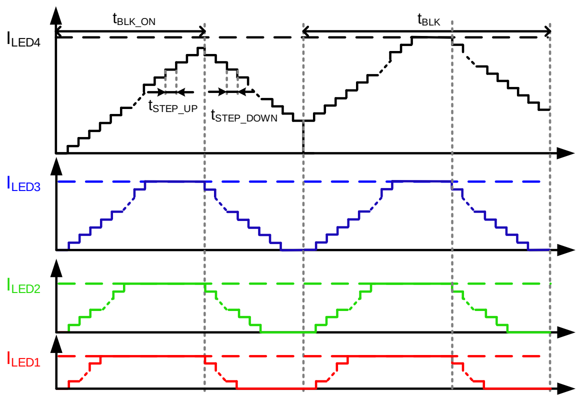


Figure 10: I_{LEDx} under Breathing Light

Phase Shift

The MP3320B integrates phase shift to eliminate audible noise and reduce inrush current in PWM dimming. The phase shift function is enabled by setting PS[1:0]. When the phase shift function is enabled, the rising edge sequence of I_{LED1} to I_{LED4} follows: channel 4, channel 3, channel 2, channel 1. The PS[1:0] setting determines the shifted phase, described below:

- If PS[1:0] = 00b, phase shift is disabled.
- If PS[1:0]= 01b, phase shift is enabled and the shifted phase is 90°.
- If PS[1:0]= 10b, phase shift is enabled and the shifted phase is 120°.
- If PS[1:0] = 11b, phase shift is enabled and the shifted phase is 180°.

Note that the rising edge sequence and shifted phase of I_{LED1} to I_{LED4} remain unchanged even when certain channels are disabled. When PS[1:0] = 01b and channel 2 is disabled, the I_{LED1} rising edge delays 180° after the I_{LED3} rising edge.

Protections

The MP3320B integrates LED open protection, LED short protection, over-voltage protection (OVP), and over-temperature protection. All channels include a corresponding LED open and LED short fault indicator bit.

LED Open Protection

LED open protection is achieved by detecting V_{LEDx} (where x = 1, 2, 3, or 4). V_{LEDx} drops when an LED string is open. If V_{LEDx} drops below the LED open protection threshold and lasts for 24ms, LED open protection is triggered by setting OLP_MD[1:0]. Once an LED open protection is triggered, the IC has different actions depending on the OLP_MD[1:0] setting, described below:

- If OLP_MD[1:0] = 00b, the IC has no action.
- If OLP_MD[1:0] = 01b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4).
- If OLP_MD[1:0] = 10b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4), and turns off the fault channel.
- If OLP_MD[1:0] = 11b, the IC sets the corresponding fault indicator bit, FT_CHxO (where x = 1, 2, 3, or 4), and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.

LED Short Protection

The MP3320B monitors V_{LEDx} to determine whether an LED short has occurred. If one or more LED strings are shorted, the LEDx pins tolerate high voltage stress. If V_{LEDx} exceeds the LED short protection threshold (configured by SLP[1:0]) and lasts for 24ms, LED short protection is triggered. If V_{LEDx} of all the enabled channels exceed the protection threshold, LED short protection is triggered only when this fault condition lasts for 100ms. Once an LED short protection is triggered, the IC has different actions depending on the SLP_MD[1:0] setting, described below:

- If SLP_MD[1:0] = 00b, the IC has no action.
- If SLP_MD[1:0] = 01b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4).
- If SLP_MD[1:0] = 10b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4), and turns off the fault channel.

- If SLP_MD[1:0] = 11b, the IC sets the corresponding fault indicator bit, FT_CHxS (where x = 1, 2, 3, or 4), and resets EN to 0 to enter standby mode. The IC exits standby mode once EN is set to 1.

Over-Temperature Protection

To prevent the IC from operating at an exceedingly high temperature, over-temperature protection is implemented by detecting the silicon die temperature. If the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down. Once the die temperature drops below the lower threshold, the IC resumes normal operation. The hysteresis is typically 20°C.

One-Time Programmable (OTP) Memory

The MP3320B can change the register default values one time via the one-time programmable (OTP) memory. MPS can provide a custom default value with a different -3320B suffix.

I2C INTERFACE

I2C Chip Address

The device address of the 7 most signifcant bits (MSB) is 60h~6Fh, where A3~A0 is configured via an ADR resistor (R_{ADR}). Table 2 shows the recommended R_{ADR} configurations to set the I2C address.

Table 2: I2C ADR Resistor vs Device Address

R_{ADR} (1% Accuracy) (kΩ)	I2C Address (A3A2A1A0)
0	0000
2	0001
4	0010
6	0011
8	0100
10	0101
14	0110
18	0111
22	1000
26	1001
30	1010
34	1011
38	1100
74	1101
86	1110
>150 or floating	1111

Figure 11 shows an I2C-compatible device address, where A0~A3 is configured by the ADR pin. After a start (S) condition, the I2C-compatible master sends a 7-bit address, followed by an eighth data direction bit (where 1 = read and 0 = write).

1	1	0	A3	A2	A1	A0	R/W

Figure 11: I2C-Compatible Device Address

I²C REGISTER MAP (7)

Name	R/W	Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
ADDR_IC	R	00h	00h	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
BLK_MD	R/W	01h	06h	NC	NC	NC	DMBLK	EN	CH4MD	BLK_ PWM	NC
BOOST_MD	R/W	02h	24h	VOUT1	VOUT0	FSW2	FSW1	FSW0	ILIMIT1	ILIMIT0	EN_BST
CHN_SET	R/W	03h	0Fh	CLED4	CLED3	CLED2	CLED1	CH4EN	CH3EN	CH2EN	CH1EN
STEP_UP/DOWN	R/W	04h	11h	STEP_ UP3	STEP_ UP2	STEP_ UP1	STEP_ UP0	STEP_ DOWN3	STEP_ DOWN2	STEP_ DOWN1	STEP_ DOWN0
ILED_FPWM	R/W	05h	10h	FPWM7	FPWM6	FPWM5	FPWM4	FPWM3	FPWM2	FPWM1	FPWM0
ILED_FBLK	R/W	06h	20h	FBLK7	FBLK6	FBLK5	FBLK4	FBLK3	FBLK2	FBLK1	FBLK0
DUTYBLK	R/W	07h	03h	DUTY BLK7	DUTY BLK6	DUTY BLK5	DUTY BLK4	DUTY BLK3	DUTY BLK2	DUTY BLK1	DUTY BLK0
BLK_TIMES	R/W	08h	00h	BLK_ TIMES7	BLK_ TIMES6	BLK_ TIMES5	BLK_ TIMES4	BLK_ TIMES3	BLK_ TIMES2	BLK_ TIMES1	BLK_ TIMES0
PRO_MD	R/W	09h	ACh	SLP_MD1	SLP_MD0	OLP_MD1	OLP_MD0	SLP1	SLP0	PS1	PS0
ILED_CH1	R/W	0Ah	32h	ICH1[7:0]							
ILED_CH2	R/W	0Bh	32h	ICH2[7:0]							
ILED_CH3	R/W	0Ch	32h	ICH3[7:0]							
ILED_CH4	R/W	0Dh	32h	ICH4[7:0]							
DPWM_CH1_1	R/W	0Eh	00h	NC					PWM1[2:0]		
DPWM_CH1_2	R/W	0Fh	80h	PWM1[10:3]							
DPWM_CH2_1	R/W	10h	00h	NC					PWM2[2:0]		
DPWM_CH2_2	R/W	11h	80h	PMW2[10:3]							
DPWM_CH3_1	R/W	12h	00h	NC					PWM3[2:0]		
DPWM_CH3_2	R/W	13h	80h	PWM3[10:3]							
DPWM_CH4_1	R/W	14h	00h	NC					PWM4[2:0]		
DPWM_CH4_2	R/W	15h	80h	PMW4[10:3]							
FAU_STATE	R	16h	00h	FT_CH4S	FT_CH3S	FT_CH2S	FT_CH1S	FT_ CH4O	FT_ CH3O	FT_CH2O	FT_CH1O

Note:

7) All registers have a configurable OTP memory by default.

I2C REGISTER DESCRIPTION

ADDR_IC (00h)

Format: Unsigned binary

The ADDR_IC command enables the device ID.

Bits	Access	Bit Name	Default	Description
7:0	R	ID[7:0]	00h	Enables the device ID.

BLK_MD (01h)

Format: Unsigned binary

The BLK_MD command sets the blinking mode.

Bits	Access	Bit Name	Default	Description
7:5	R/W	RESERVED	3'b000	Reserved. Do not change the default value.
4	R/W	DMBLK	1'b0	Sets the dimming or blinking mode. 1'b0: Dimming mode 1'b1: Blinking mode
3	R/W	EN	1'b0	Enables the IC. 1'b0: Standby mode 1'b1: Enabled
2	R/W	CH4MD	1'b1	Enables channel 4 in blinking mode. 1'b0: Channel 4 does not work in blinking mode, and follows PWM dimming and analog dimming 1'b1: If DMBLK = 1b, channels 1~4 work in blinking mode; if DMBLK = 0b, channel 1~4 do not work in blinking mode.
1	R/W	BLK_PWM	1'b1	Sets the operation mode after blinking completes. 1'b0: The IC enters standby mode after blinking completes 1'b1: The IC follows PWM and analog dimming after blinking completes
0	R/W	RESERVED	1'b0	Reserved. Do not change the default value.

BOOST_MD (02h)

Format: Unsigned binary

The BOOST_MD command sets the boost converter's operation mode.

Bits	Access	Bit Name	Default	Description
7:6	R/W	VOUT[1:0]	2'b00	Sets the boost converter's operation mode. 2'b00: Minimum active V_{LEDx} control 2'b01: V_{OUT} = 4V 2'b10: V_{OUT} = 4.5V 2'b11: V_{OUT} = 5V
5:3	R/W	FSW[2:0]	3'b100	Sets the boost switching frequency (f_{SW}). 3'b000: 200kHz 3'b001: 400kHz 3'b010: 666kHz 3'b011: 800kHz 3'b100: 1MHz 3'b101: 1.33MHz 3'b110~3'b111: Reserved

2:1	R/W	ILIMIT[1:0]	2'b10	Sets the internal LS-FET peak current limit. 2'b00: 0.5A 2'b01: 0.75A 2'b10: 1A 2'b11: 1.5A
0	R/W	EN_BST	1'b0	Enables the boost block. 1'b0: Disabled 1'b1: Enabled When the boost block is disabled, channels 1~4 can only work in pure current source mode.

CHN_SET (03h)

Format: Unsigned binary

The CHN_SET command sets the operation mode and enable bits of channels 1~4.

Bits	Access	Bit Name	Default	Description
7	R/W	CLED4	1'b0	Sets channel 4 to operate white LED in pure current source. 1'b0: Connects to the boost control loop 1'b1: Channel 4 works in pure current source
6	R/W	CLED3	1'b0	Sets channel 3 to operate blue LED in pure current source. 1'b0: Connects to the boost control loop 1'b1: Channel 3 works in pure current source
5	R/W	CLED2	1'b0	Sets channel 2 to operate green LED in pure current source. 1'b0: Connects to the boost control loop 1'b1: Channel 2 works in pure current source
4	R/W	CLED1	1'b0	Sets channel 1 to operate red LED in pure current source. 1'b0: Connects to the boost control loop 1'b1: Channel 1 works in pure current source
3	R/W	CH4EN	1'b1	Enables channel 4. 1'b0: Disables channel 4 1'b1: Enables channel 4
2	R/W	CH3EN	1'b1	Enables channel 3. 1'b0: Disables channel 3 1'b1: Enables channel 3
1	R/W	CH2EN	1'b1	Enables channel 2. 1'b0: Disables channel 2 1'b1: Enables channel 2
0	R/W	CH1EN	1'b1	Enables channel 1. 1'b0: Disables channel 1 1'b1: Enables channel 1

STEP_UP/DOWN (04h)

Format: Unsigned binary

The STEP_UP/DOWN command sets the LED current step-up and step-down time.

Bits	Access	Bit Name	Default	Description
7:4	R/W	STEP_UP[3:0]	4'b0001	Sets the current step-up time (µs/step). 4'b0001: 2µs 4'b0010: 4µs 4'b0011: 8µs 4'b0100: 16µs 4'b0101: 32µs 4'b0110: 64µs 4'b0111: 128µs 4'b1000: 256µs 4'b1001: 512µs 4'b1010: 1ms 4'b1011: 2ms 4'b1100: 4ms 4'b1101: 8ms 4'b1110: 16ms 4'b1111: 32ms
3:0	R/W	STEP_DOWN [3:0]	4'b0001	Sets the current step-down time (µs/step). 4'b0001: 2µs 4'b0010: 4µs 4'b0011: 8µs 4'b0100: 16µs 4'b0101: 32µs 4'b0110: 64µs 4'b0111: 128µs 4'b1000: 256µs 4'b1001: 512µs 4'b1010: 1ms 4'b1011: 2ms 4'b1100: 4ms 4'b1101: 8ms 4'b1110: 16ms 4'b1111: 32ms

ILED_FPWM (05h)

Format: Unsigned binary

The ILED_FPWM command sets f_{PWM}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FPWM[7:0]	10h	Sets f_{PWM}. In dimming mode (DMBLK = 0b), f_{PWM} can be set according to the following register values: 01h: 31.25kHz 02h: 15.625kHz 03h: 10.42kHz 04h: 7.81kHz 05h: 6.25kHz 06h: 5.2kHz 07h: 4.46kHz 08h: 3.906kHz 10h: 1.95kHz 18h: 1.30kHz 20h: 976Hz 28h: 781Hz 30h: 651Hz 38h: 558Hz 40h: 488Hz 48h: 434Hz 50h: 390Hz 58h: 355Hz 60h: 325Hz 68h: 300Hz 70h: 279Hz 78h: 260Hz 80h: 244Hz If f_{PWM} exceeds 3.906kHz (FPWM[7:0] < 08h) and the clock frequency is 4MHz, the PWM dimming duty resolution is below 10 bits.

ILED_FBLK (06h)

Format: Unsigned binary

The ILED_FBLK command sets f_{BLK}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FBLK[7:0]	20h	In blinking mode (DMBLK = 1b), f_{BLK} can be calculated with the following equation: $f_{BLK} = 1/(16.384ms \times FBLK[7:0])$ f_{BLK} can be set according to the following register values: 01h: 61Hz 02h: 30.5Hz 03h: 20.3Hz … 20h: 1.907Hz … 3Dh: 1Hz … 7Ah: 0.5Hz … FFh: 0.239Hz

DUTYBLK (07h)

Format: Unsigned binary

The DUTYBLK command sets the blinking duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	DUTYBLK[7:0]	03h	In blinking mode, the blinking on time (t_{BLK_ON}) can be calculated with the following equation: $t_{BLK\_ON} = 16.384 \times DUTYBLK[7:0]$ (ms) If DUTYBLK[7:0] = 03h and FBLK[7:0] = 20h, the blinking duty is about 10%.

BLK_TIMES (08h)

Format: Unsigned binary

The BLK_TIMES command sets the blinking cycles.

Bits	Access	Bit Name	Default	Description
7:0	R/W	BLK_TIMES[7:0]	00h	Sets the blinking cycles. 00h: Infinitely runs in blinking mode 01h: 1 cycle 02h: 2 cycles 03h: 3 cycles … FFh: 255 cycles

PRO_MD (09h)

Format: Unsigned binary

The PRO_MD command sets the protection mode and the phase shift.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SLP_MD[1:0]	2'b10	Sets the IC action after LED short protection is triggered. 2'b00: No action 2'b01: Sets the corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4) 2'b10: Sets the corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4), and turns off the fault channel 2'b11: Sets the corresponding fault bit, FT_CHxS (where x = 1, 2, 3, or 4), and resets EN to 0b to enter standby mode. The IC exits standby mode once EN is set to 1b
5:4	R/W	OLP_MD[1:0]	2'b10	Sets the IC action after LED open protection is triggered. 2'b00: No action 2'b01: Sets the corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4) 2'b10: Sets the corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4), and turns off the fault channel 2'b11: Sets the corresponding fault bit, FT_CHxO (where x = 1, 2, 3, or 4), and resets EN to 0b to enter standby mode. The IC exits standby mode once EN is set to 1b
3:2	R/W	SLP[1:0]	2'b11	Sets the LED short protection threshold. 2'b00: 2V 2'b01: 2.5V 2'b10: 3V 2'b11: 3.5V

1:0	R/W	PS[1:0]	2'b00	Sets the phase shift. 2'b00: No phase shift 2'b01: 90° phase shift 2'b10: 120° phase shift 2'b11: 180° phase shift

ILED_CH1 (0Ah)

Format: Unsigned binary

The ILED_CH1 command sets the channel 1 I_{LED} amplitude.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ICH1[7:0]	32h	Sets the channel 1 I_{LED} amplitude, where I_{LED1} can be calculated with the following equation: $I_{LED1} = 0.4 \times ICH1[7:0]$ (mA) Where if the ICH1[7:0] value increases by one step, I_{LED1} increases by 0.4mA. The default value is 20mA.

ILED_CH2 (0Bh)

Format: Unsigned binary

The ILED_CH2 command sets the channel 2 I_{LED} amplitude.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ICH2[7:0]	32h	Sets the channel 2 I_{LED} amplitude, where I_{LED2} can be calculated with the following equation: $I_{LED2} = 0.4 \times ICH2[7:0]$ (mA) Where if the ICH2[7:0] value increases by one step, then I_{LED2} increases by 0.4mA. The default value is 20mA.

ILED_CH3 (0Ch)

Format: Unsigned binary

The ILED_CH3 command sets the channel 3 I_{LED} amplitude.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ICH3[7:0]	32h	Sets the channel 3 I_{LED} amplitude, where I_{LED3} can be calcuated with the following equation: $I_{LED3} = 0.4 \times ICH3[7:0]$ (mA) Where if the ICH3[7:0] value increases by one step, then I_{LED3} increases by 0.4mA. The default value is 20mA.

ILED_CH4 (0Dh)

Format: Unsigned binary

The ILED_CH4 command sets the channel 4 I_{LED} amplitude.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ICH4[7:0]	32h	Sets the channel 4 I_{LED} amplitude, where I_{LED4} can be calculated with the following equation: $I_{LED4} = 0.4 \times ICH4[7:0]$ (mA) Where if the ICH4[7:0] value increases by one step, then I_{LED4} increases by 0.4mA. The default value is 20mA.

DPWM_CH1_1 (0Eh)

Format: Unsigned binary

The DPWM_CH1_1 command sets the 3LSB for the channel 1 I_{LED} PWM dimming duty (D_{ILED1}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	5'b 0000 0	Reserved. Do not change the default value.
2:0	R/W	PWM1[2:0]	3'b000	Sets the 3LSB for the channel 1 I_{LED} PWM dimming duty (D_{ILED1}). PWM1[2:0] is valid after PWM1[10:3] is written.

DPWM_CH1_2 (0Fh)

Format: Unsigned binary

The DPWM_CH1_2 command sets the 8MSB for D_{ILED1}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM1[10:3]	80h	Sets the 8MSB for D_{ILED1}. PWM1[2:0] is valid after PWM1[10:3] is written.

DPWM_CH2_1 (10h)

Format: Unsigned binary

The DPWM_CH2_1 command sets the 3LSB for the channel 2 I_{LED} PWM dimming duty (D_{ILED2}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	5'b 0000 0	Reserved. Do not change the default value.
2:0	R/W	PWM2[2:0]	3'b000	Sets the 3LSB for D_{ILED2}. PWM2[2:0] is valid after PWM2[10:3] is written.

DPWM_CH2_2 (11h)

Format: Unsigned binary

The DPWM_CH2_2 command sets the 8MSB for D_{ILED2}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM2[10:3]	80h	Sets the 8MSB for D_{ILED2}. PWM2[2:0] is valid after PWM2[10:3] is written.

DPWM_CH3_1 (12h)

Format: Unsigned binary

The DPWM_CH3_1 command sets the 3LSB for the channel 3 I_{LED} PWM dimming duty (D_{ILED3}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	5'b 0000 0	Reserved. Do not change the default value.
2:0	R/W	PWM3[2:0]	3'b000	Sets the 3LSB for D_{ILED3}. PWM3[2:0] is valid after PWM3[10:3] is written.

DPWM_CH3_2 (13h)

Format: Unsigned binary

The DPWM_CH3_2 command sets the 8MSB for D_{ILED3}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM3[10:3]	80h	Sets the 8MSB for D_{ILED3}. PWM3[2:0] is valid after PWM3[10:3] is written.

DPWM_CH4_1 (14h)

Format: Unsigned binary

The DPWM_CH4_1 command sets the 3LSB for the channel 4 I_{LED} PWM dimming duty (D_{ILED4}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	5'b 0000 0	Reserved. Do not change the default value.
2:0	R/W	PWM4[2:0]	3'b000	Sets the 3LSB for D_{ILED4}. PWM4[2:0] is valid after PWM4[10:3] is written.

DPWM_CH4_2 (15h)

Format: Unsigned binary

The DPWM_CH4_2 command sets the 8MSB for D_{ILED4}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM4[10:3]	80h	Sets the 8MSB for D_{ILED4}. PWM4[2:0] is valid after PWM4[10:3] is written.

FAU_STATE (16h)

Format: Unsigned binary

The FAU_STATE command reads the LED short or open fault state of channels 1~4.

Bits	Access	Bit Name	Default	Description
7	R	FT_CH4S	1'b0	Sets channel 4's LED short protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No short fault 1'b1: Channel 4 is shorted
6	R	FT_CH3S	1'b0	Sets channel 3's LED short protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No short fault 1'b1: Channel 3 is shorted
5	R	FT_CH2S	1'b0	Sets channel 2's LED short protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No short fault 1'b1: Channel 2 is shorted
4	R	FT_CH1S	1'b0	Sets channel 1's LED short protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No short fault 1'b1: Channel 1 is shorted
3	R	FT_CH4O	1'b0	Sets channel 4's LED open protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No open fault 1'b1: Channel 4 is open
2	R	FT_CH3O	1'b0	Sets channel 3's LED open protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No open fault 1'b1: Channel 3 is open
1	R	FT_CH2O	1'b0	Sets channel 2's LED open protection fault indicator, which resets to 0 after a readback or power reset. 1'b0: No open fault 1'b1: Channel 2 is open

0	R	FT_CH1O	1’b0	Sets channel 1’s LED open protection fault indicator, which resets to 0 after a readback or power reset. 1’b0: No open fault 1’b1: Channel 1 is open

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. C_{IN} impedance at the switching frequency (f_{SW}) should be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 4.7µF ceramic capacitor is sufficient.

Selecting the Inductor

The MP3320B requires an inductor to supply a high V_{OUT} while being driven by V_{IN}. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the internal N-channel MOSFET; however, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Choose a minimum inductance to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and reduced EMI.

The required inductance (L) can be calculated with Equation (5):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (5)$$

Where I_{LOAD} is the LED load current, η is the efficiency, and D is the duty.

The duty (D) can be estimated with Equation (6):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (6)$$

For most applications, the inductor DC current rating should be at least 40% higher than the maximum input peak inductor current. The inductor's DC resistance should be as small as possible to achieve high efficiency.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the V_{OUT} ripple small and ensures feedback loop stability. C_{OUT} impedance should be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7µF ceramic capacitor is sufficient.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation (especially the high-frequency switching path to reduce noise and EMI). For the best results, refer to Figure 12 and follow the guidelines below:

1. A high-frequency pulse current flows through the loop between SW, OUT, C_{OUT}, and GND. Keep this loop as short as possible to reduce noise and EMI.
2. Connect the power ground to the signal ground externally.
3. Route the power ground away from the logic signals.
4. Place the ceramic capacitor (C1) as close to VIN as possible.

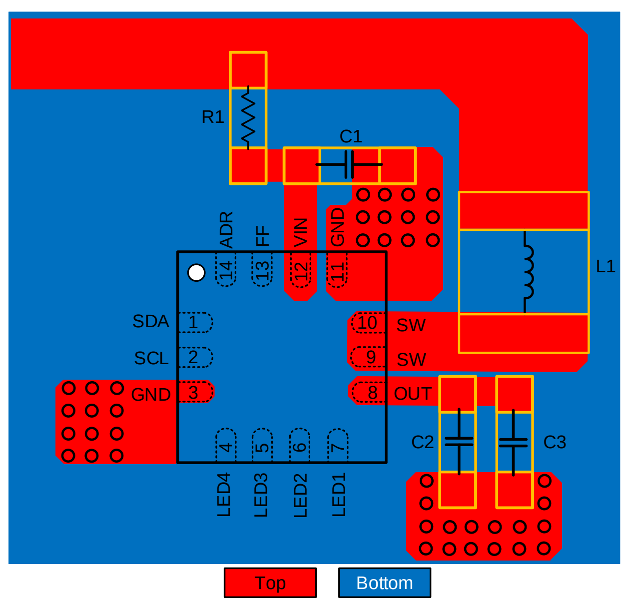


Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

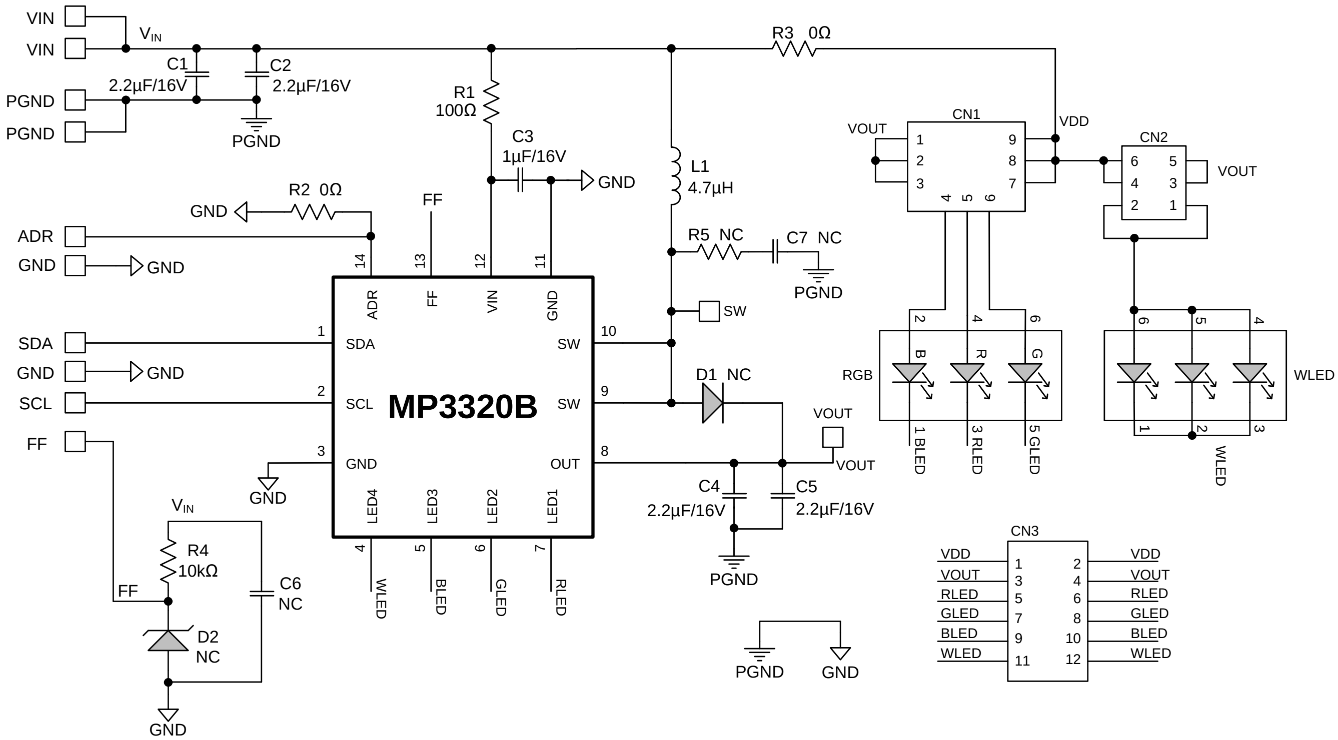
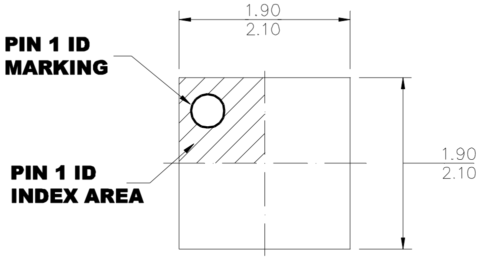


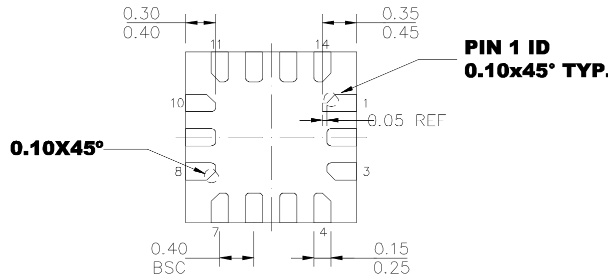
Figure 13: Typical Application Circuit

PACKAGE INFORMATION

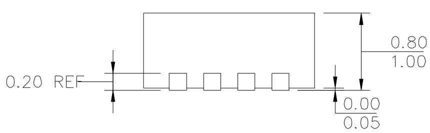
QFN-14 (2mmx2mm)



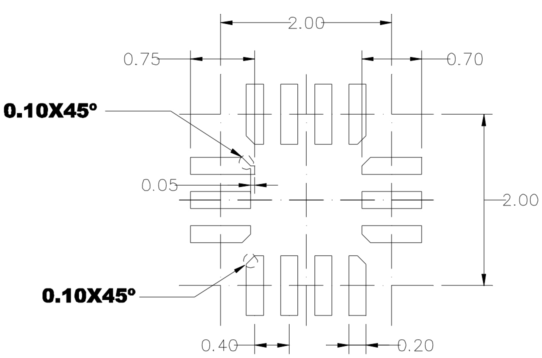
TOP VIEW



BOTTOM VIEW



SIDE VIEW

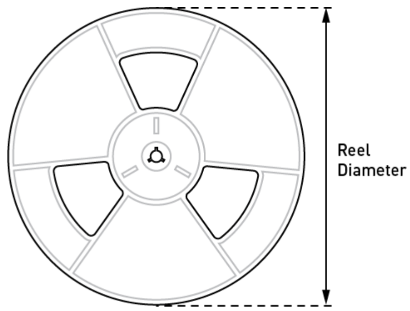


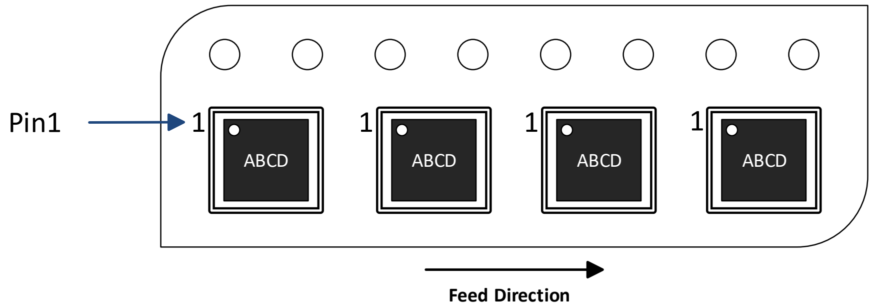
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3320BGG-Z	QFN-14 (2mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/13/2023	Initial Release	-