MP5025C

16V, 15A, 3mΩ R_{DS_ON}, Hot-Swap Protection Device with Current Monitoring

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MP5022C

DESCRIPTION

The MP5025C is a hot-swap protection device designed to protect circuitry on its output from transients on its input. The MP5025C also protects its input from unwanted shorts and transients coming from its output.

During start-up, inrush current is limited by the slew rate at the output. The slew rate is controlled by an external capacitor at SS.

The maximum load at the output is current-limited through sense FET topology. The magnitude of the current limit is controlled by a low-power resistor from ISET to ground.

An internal charge pump drives the gate of the power device, allowing a power FET with a very low on resistance of 3mΩ to turn on.

The MP5025C includes an IMON option that produces a voltage proportional to the current through the power device set by a resistor from IMON to ground.

Full protection features includes current limit, thermal shutdown, damaged MOSFET detection, over-voltage protection (OVP), and under-voltage protection (UVP).

The MP5025C is available in a QFN-22 (3mmx5mm) package.

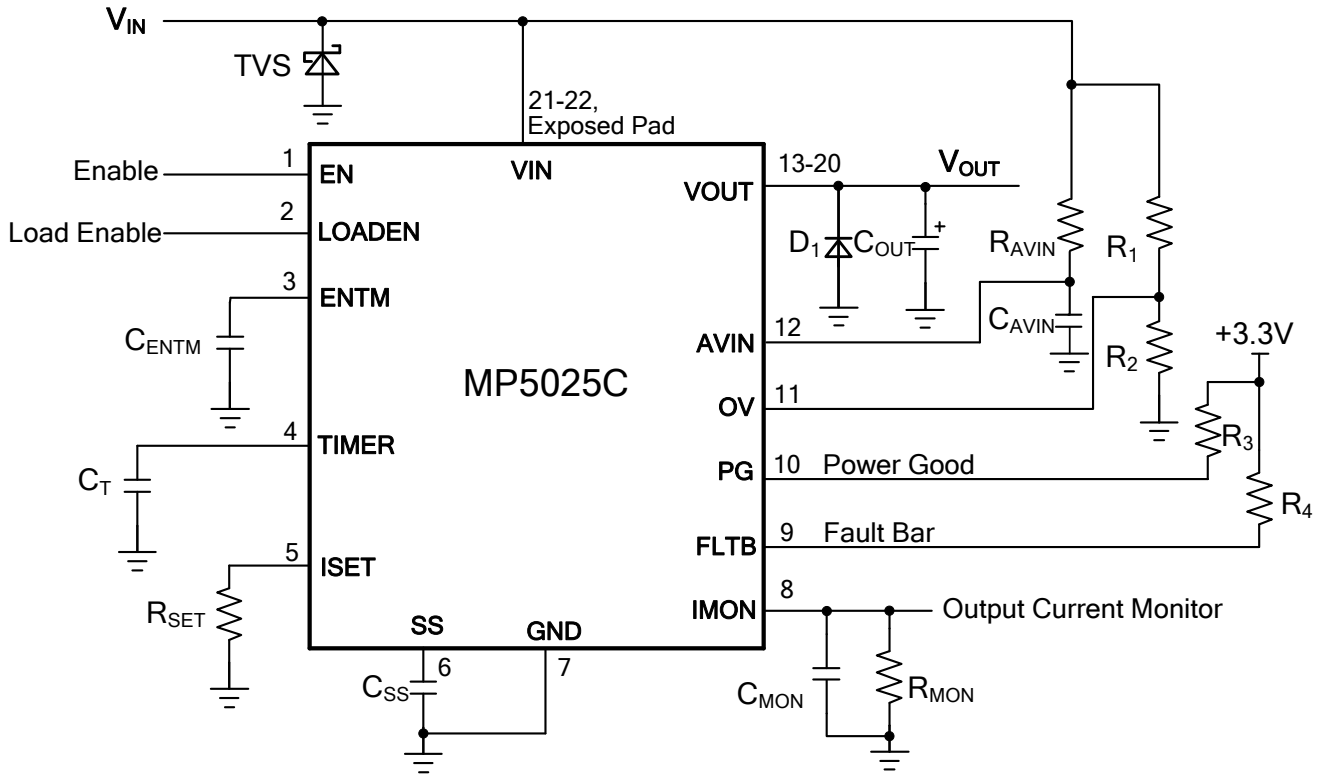
FEATURES

- 4.5V to 16V Operating Input Range
- Integrated 3mΩ Power FET
- Adjustable Current Limit
- Output Current Measurement
- ±3% Current Monitor Accuracy (6A < Io < 15A)
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at VIN = 0
- Input-to-Output Short-Circuit Detection
- External Soft Start
- Programmable LOADEN Blanking Time
- Configurable Over-Voltage Lockouts with Hysteresis
- Under-Voltage Lockout (UVLO)
- Thermal Protection
- Available in a Small QFN-22 (3mmx5mm) Package

APPLICATIONS

- Hot Swap
- PC Cards
- Disk Drives
- Servers
- Networking
- Laptops

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5025CGQV	QFN-22 (3mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP5025CGQV–Z)

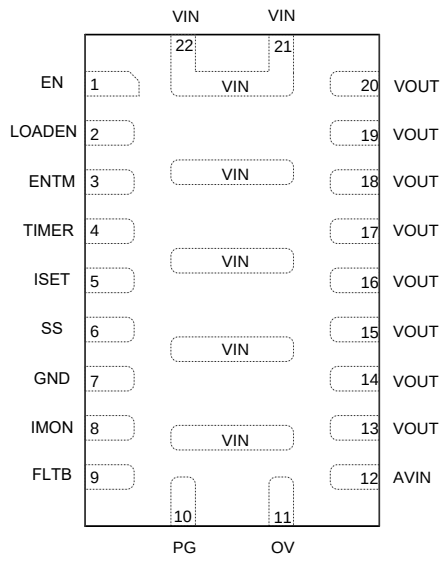
TOP MARKING

MPYW
5025
CLLL

MP: MPS prefix
Y: Year code
W: Week code
5025C: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-22 (3mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** EN used in conjunction with LOADEN can turn on or off the main power device in the MP5025C. EN is pulled high internally.
2	LOADEN	**Load enable input.** LOADEN used in conjunction with EN can turn on or off the main power device in the MP5025C (see Table 1). LOADEN is also used to shut down the power switch after the LOADEN blanking time, but cannot turn it back on by recycling LOADEN only.
3	ENTM	**LOADEN blanking time set.** Connect an external capacitor to set the LOADEN blanking time. Once EN is active, the timer starts and the LOADEN de-assertion is blanked. The switch shuts down in the presence of a fault or EN low condition, but LOADEN low during the blanking time has no effect.
4	TIMER	**Timer set.** An external capacitor sets the hot-plug insertion time delay and fault time-out period.
5	ISET	**Current limit set.** Place a resistor from ISET to ground to set the value of the over-current limit.
6	SS	**Soft start.** An external capacitor connected to SS sets the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage at start-up. Float SS to set the soft-start time at its minimum (1ms).
7	GND	**Ground.**
8	IMON	**Output current monitor.** IMON provides a voltage proportional to the current flowing through the power device. Placing a 10kΩ resistor (R_{MON}) to ground creates a 0V to 1.5V voltage when the current is between 0A and 15A. Place a capacitor greater than 10nF in parallel with R_{MON} during application.
9	FLTB	**Fault bar.** FLTB is an open-drain output that drives to ground when an over-current or a thermal shutdown occurs. Pull FLTB up to an external power supply through a 10-100kΩ resistor.
10	PG	**Power good.** PG is an open-drain output. Pull PG up to an external power supply through a 10-100kΩ resistor. PG high means power good.
11	OV	**Over-voltage enable input.** Pull OV high to turn off the internal MOSFET. Connect OV to an external resistive divider to set the over-voltage disable threshold.
12	AVIN	**Internal power supply for VCC sub regulator.** Connect a 49.9Ω, 0603 package resistor from VIN to AVIN and a 2.2μF bypass capacitor to GND to guarantee full operation in the event that VIN collapses during a strong short from VOUT to GND.
13-20	VOUT	**Output.** VOUT is the voltage controlled by the IC. A Schottky diode should be placed between VOUT and GND to absorb the negative voltage spike.
21, 22, Exposed Pads	VIN	**Input power supply for main power.**

ABSOLUTE MAXIMUM RATINGS (1)

VIN, AVIN ..... -0.3V to 24V
VOUT ..... -0.3V to 20V
Other pins ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
..... 2.7W
Junction temperature ..... +150°C
Storage temperature ..... -65°C to +155°C

Recommended Operating Conditions (3)

Input voltage operating range ..... .4.5V to 16V
Operating junction temp. (T_J). .....
..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-22 (3mmx5mm)	46	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{SET} = 10.2k, C_{OUT} = 470µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	EN = high, no load		1.3	2.0	mA
		Fault latch off		1.3		mA
		EN = 0, V_{IN} = 16V			700	µA
Power FET						
On resistance	$R_{DS(ON)}$	T_J = 25°C		3	4	mΩ
		T_J = 85°C(5)		3.8	4.8	
Off-state leakage current	I_{OFF}	V_{IN} = 24V, EN = 0V			1	µA
Maximum continuous current(5)	I_{OUT_MAX}		15			A
Thermal Shutdown						
Shutdown temperature(5)	t_{STD}			145		°C
VIN Under-Voltage Protection (UVLO)						
VIN UVLO threshold	$V_{IN\ UVLO}$	VIN UVLO rising threshold		4.15V	4.4	V
VIN UVLO hysteresis	$V_{IN\ UVLOHYS}$			0.25		V
LOADEN						
Low-level input voltage	V_L				0.9	V
High-level input voltage	V_H		2.3			V
Soft Start (SS)						
SS pull-up current	I_{SS}	V_{SS} = 0V	10	12.5	15	µA
Current Limit						
Current limit at normal operation	I_{Limit_NO}	R_{SET} = 10.2k	11.34	12.6	13.86	A
Current limit response time(5)	t_{CL}			20		µs
Secondary current limit(5)	I_{LimitH}	Regardless of R_{SET}		36		A
Short-circuit protection response time(5)	t_{SC}			200		ns
Output Current Monitor						
Gain of current sense amplifier	A_{IMON}	6A < I_{OUT} < 15A	9.7	10	10.3	µA/A
		3A < I_{OUT} < 6A	9.5	10	10.5	µA/A
Max IMON voltage	V_{IMON}				3	V
Timer						
Upper threshold voltage	V_{TMRH}		1.2	1.24	1.28	V
Insertion delay charge current	I_{INSERT}		34.5	43	51.5	µA
Fault detection charge current	I_{FLTD}		175	215	255	µA
Discharge $R_{DS(ON)}$	R_{FLTE}	I_{OUT} < I_{Limit}		35	70	Ω
LOADEN Blanking Time (ENTM)						
Upper threshold voltage	V_{ENTMRH}		1.2	1.24	1.28	V
Charge current	I_{ENTMCC}		0.8	1.1	1.4	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{SET} = 10.2k, C_{OUT} = 470µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable						
Rising threshold	V_{ENRS}		1.258	1.325	1.391	V
Hysteresis	V_{ENHYS}			170		mV
Over-Voltage (OV)						
OV threshold	V_{OV_TH}	V_{OV} rising	1.2	1.24	1.28	V
OV threshold hysteresis	V_{OV_HYS}	V_{OV} falling		90		mV
Fault Bar (FLTB)/Power Good (PG)						
Low-level output voltage	V_{OL}	Sink current 1mA			0.2	V
Fault bar off-state leakage current	I_{FLT_LKG}	V_{FLTB} = 3.3V			1	µA
Fault bar propagation delay	t_{PDE}	ISET stepped to 1V to FLTB pull-down		8	16	µs
Power good rising threshold(5)	PG_{Vth_Hi}			90%		V_{IN}
Power good falling threshold	PG_{Vth_Lo}			75%	80%	V_{IN}
Power good off-state leakage current	I_{PG_LKG}	V_{PG} = 3.3V			2.5	µA
PG low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull up to 3.3V through 100kΩ resistor		600	720	mV
	V_{OL_10}	V_{IN} = 0V, pull up to 3.3V through 10kΩ resistor		720	870	mV

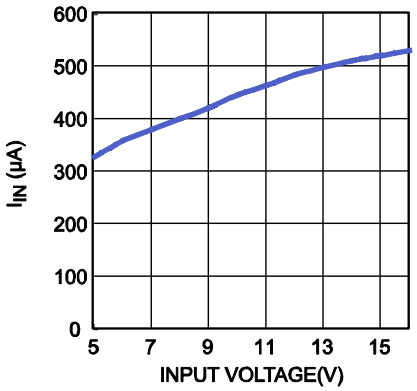
NOTE:
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 6.8kΩ, T_A = +25°C, unless otherwise noted.

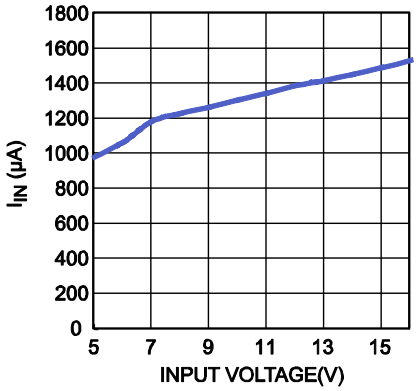
Disable Supply Current vs. Input Voltage

EN=0



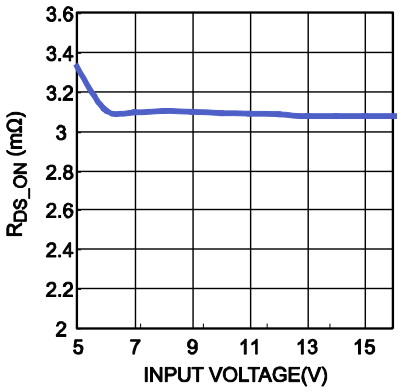
Enable Supply Current vs. Input Voltage

EN=NC, Loaden=3V, No Load



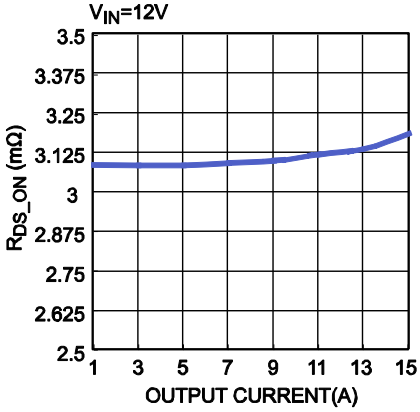
R_{DS_ON} vs. Input Voltage

I_{OUT}=1A

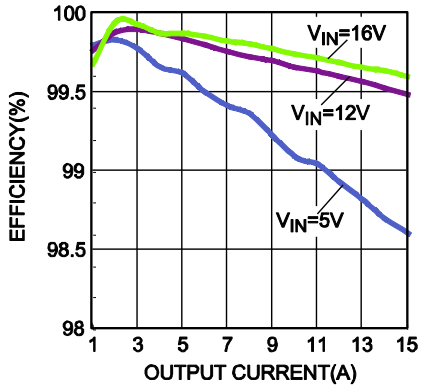


R_{DS_ON} vs. Load Current

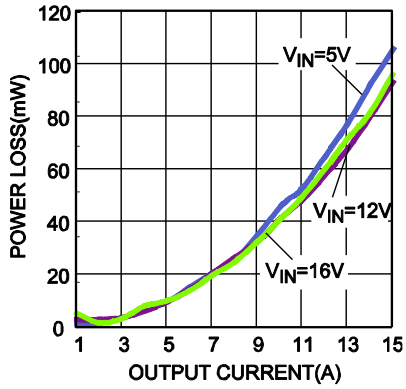
V_{IN}=12V



Efficiency vs. Load Current

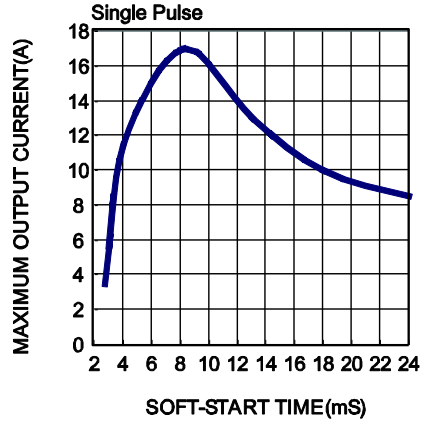


Power Loss vs. Load Current



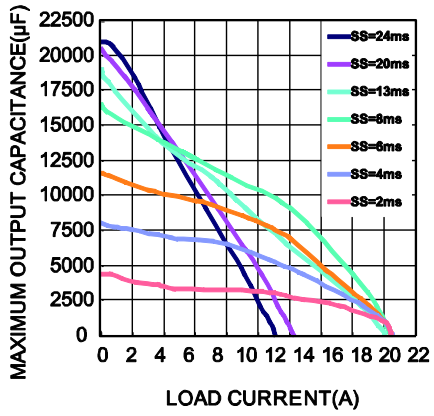
Maximum Output Current vs. Soft Start Time

V_{IN}=12V, C_{OUT}=4700µF, En On, Single Pulse

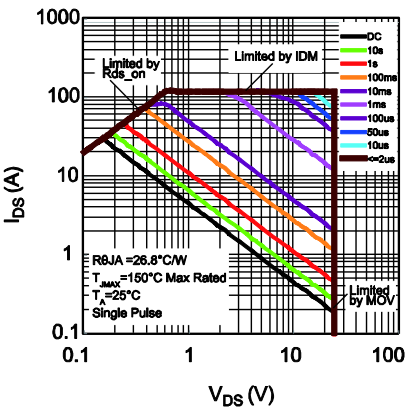


Maximum Output Cap. vs. Load Current

V_{IN}=12V, En On, Single Pulse



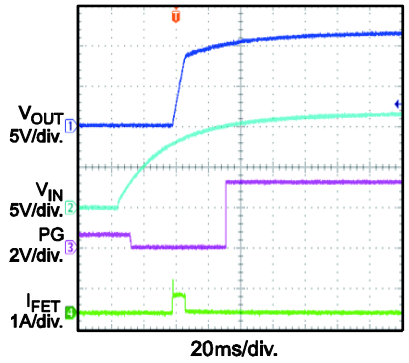
Safe Operation Area



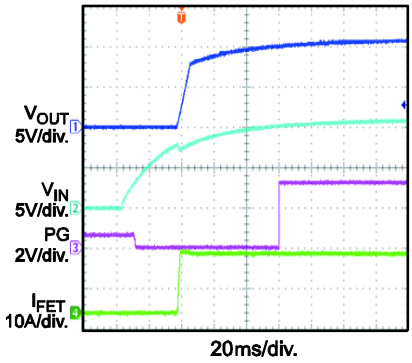
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 6.8kΩ, T_A = +25°C, unless otherwise noted.

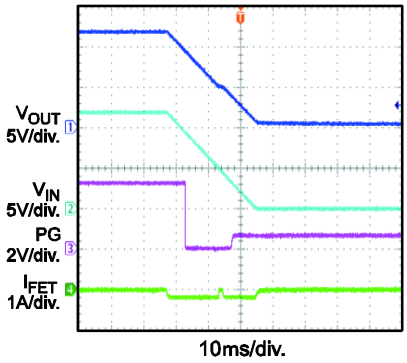
Start Up through V_{IN}
I_{OUT}=0A



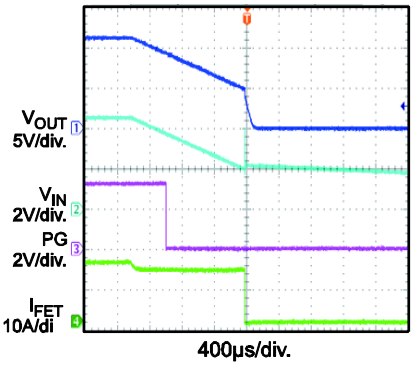
Start Up through V_{IN}
I_{OUT}=15A



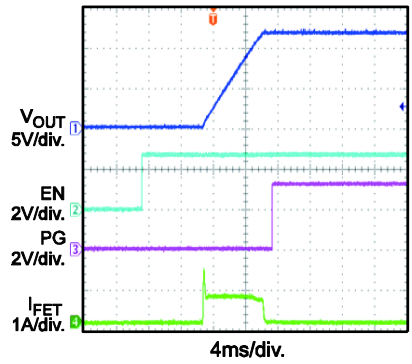
Shut Down through V_{IN}
I_{OUT}=0A



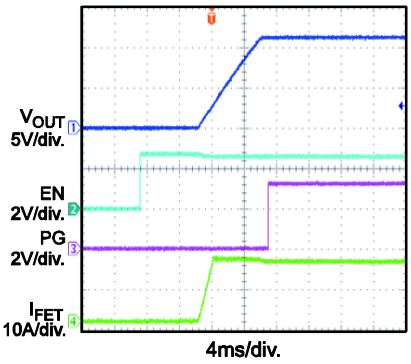
Shut Down through V_{IN}
I_{OUT}=15A



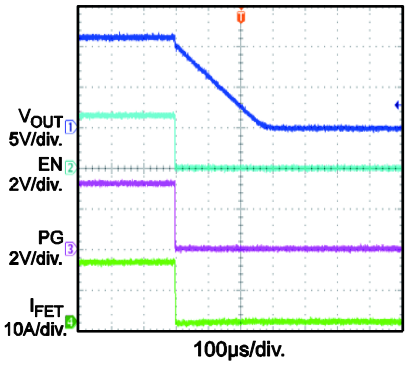
Start Up through EN
I_{OUT}=0A



Start Up through EN
I_{OUT}=15A



Shut Down through EN
I_{OUT}=15A

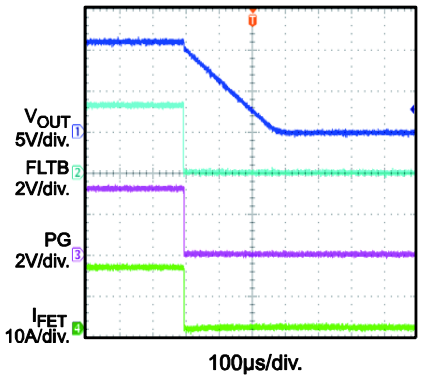


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 6.8kΩ, T_A = +25°C, unless otherwise noted.

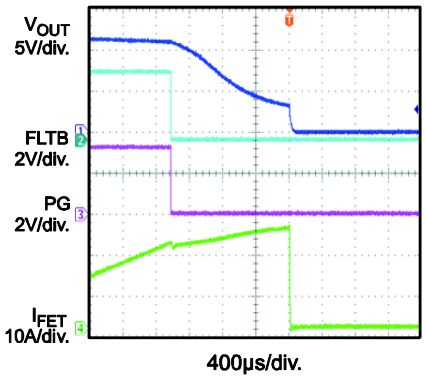
Thermal Shutdown

I_{OUT}=15A



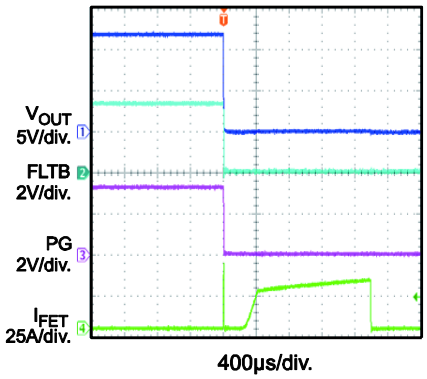
OCP

I_{LIMIT}=19A



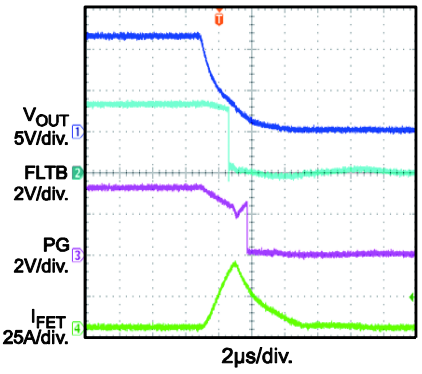
SCP Entry

I_{LIMIT}=19A



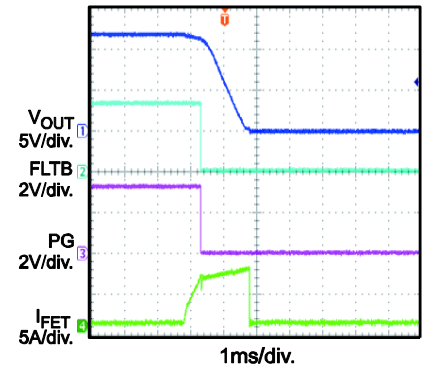
SCP Entry Detail

I_{LIMIT}=19A



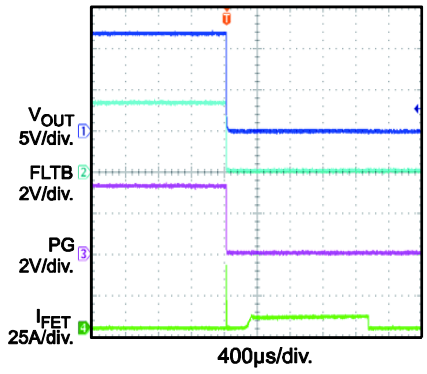
OCP

I_{LIMIT}=5A



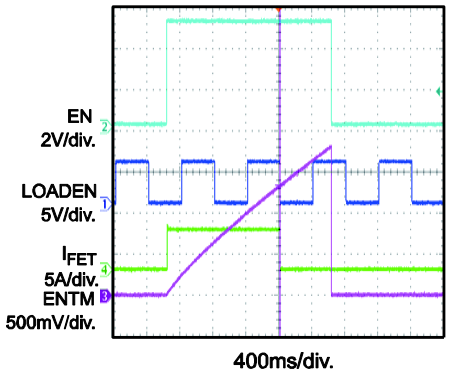
SCP Entry

I_{LIMIT}=5A



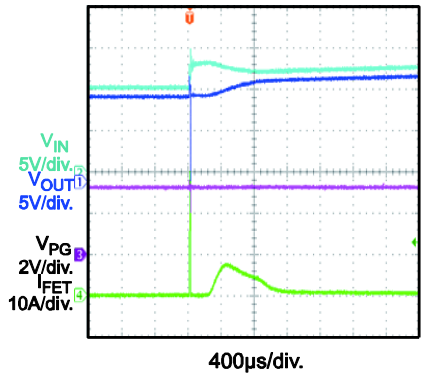
EN and LOADEN Logic

I_{OUT}=5A, EN and LOADEN signals are generated by function generator



LINE SPIKE

I_{LIMIT}=19A



BLOCK DIAGRAM

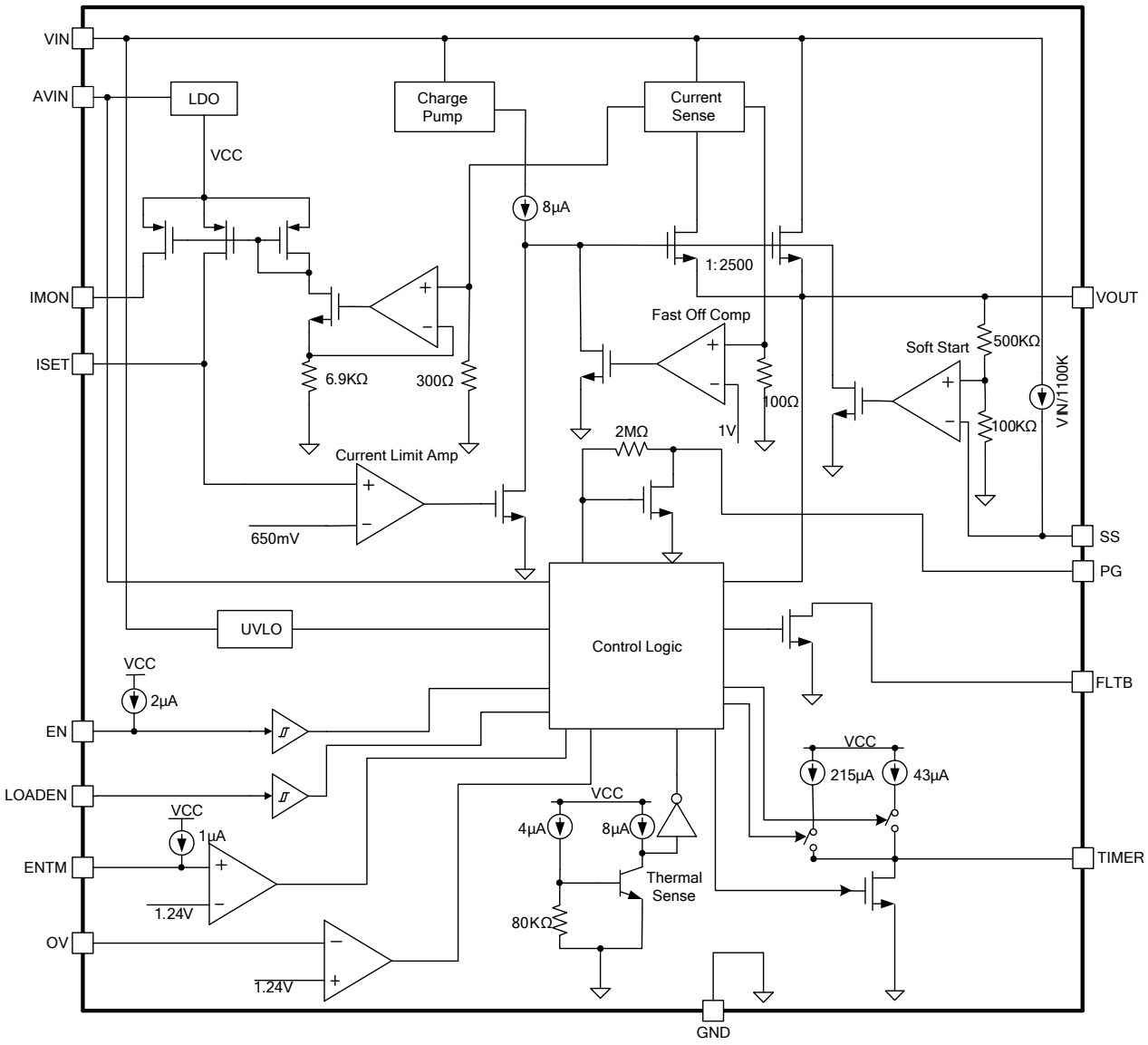


Figure 1: Functional Block Diagram

OPERATION

The MP5025C is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, limiting the backplane's voltage drop and the dV/dt of the voltage to the load. The MP5025C provides an integrated solution for monitoring the input voltage, output voltage, output current, and die temperature to eliminate the need for an external current sense power resistor, power MOSFET, and thermal sense device.

Current Limit

The MP5025C provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. To limit the current, the gate-to-source voltage must be regulated from 4V to around 1V. The typical response time is about 20µs. The output current may have a small overshoot during this time period.

When the current limit is triggered, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5025C resumes normal operation. Otherwise, if the current-limit duration exceeds the fault timeout period, the power FET is latched off.

When the device reaches either its current limit or over-temperature threshold, FLTB is driven low with an 8µs propagation delay to indicate a fault. The desired current limit at normal operation is a function of the external current-limit resistor.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current-limit threshold before the control loop can respond. If the current reaches a 36A secondary current-limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current (see Figure 2). This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns.

When short-circuit protection is triggered, the chip restarts to determine whether the overload condition exists or not. If the short-circuit has been induced by the input line transient, the part works normally. If a real short circuit occurs, the part latches off completely (see Figure 2 and Figure 3).

FLTB switches low once it reaches a 36A current limit and asserts low until the short circuit is removed.

Fault Timer and Restart

When the current reaches its limit threshold, a 215µA fault timer current source charges the external capacitor (C_T) at TIMER. If the current limit state ceases before TIMER reaches 1.24V, the MP5025C resumes normal operation mode and releases TIMER immediately when the current limit is removed. If the current limit state lasts after the TIMER voltage reaches 1.24V, the power FET switches off. The capacitance of C_T can be determined with Equation (1):

$$C_T = \frac{215 \times t_{fault}}{1.24} \quad (1)$$

Where C_T is the fault timer capacitance (nF), and t_{fault} is the fault timer (ms). For example, a 100nF capacitor yields a fault timer of 0.58ms.

This fault timer capacitor also determines the insertion delay timer during start-up.

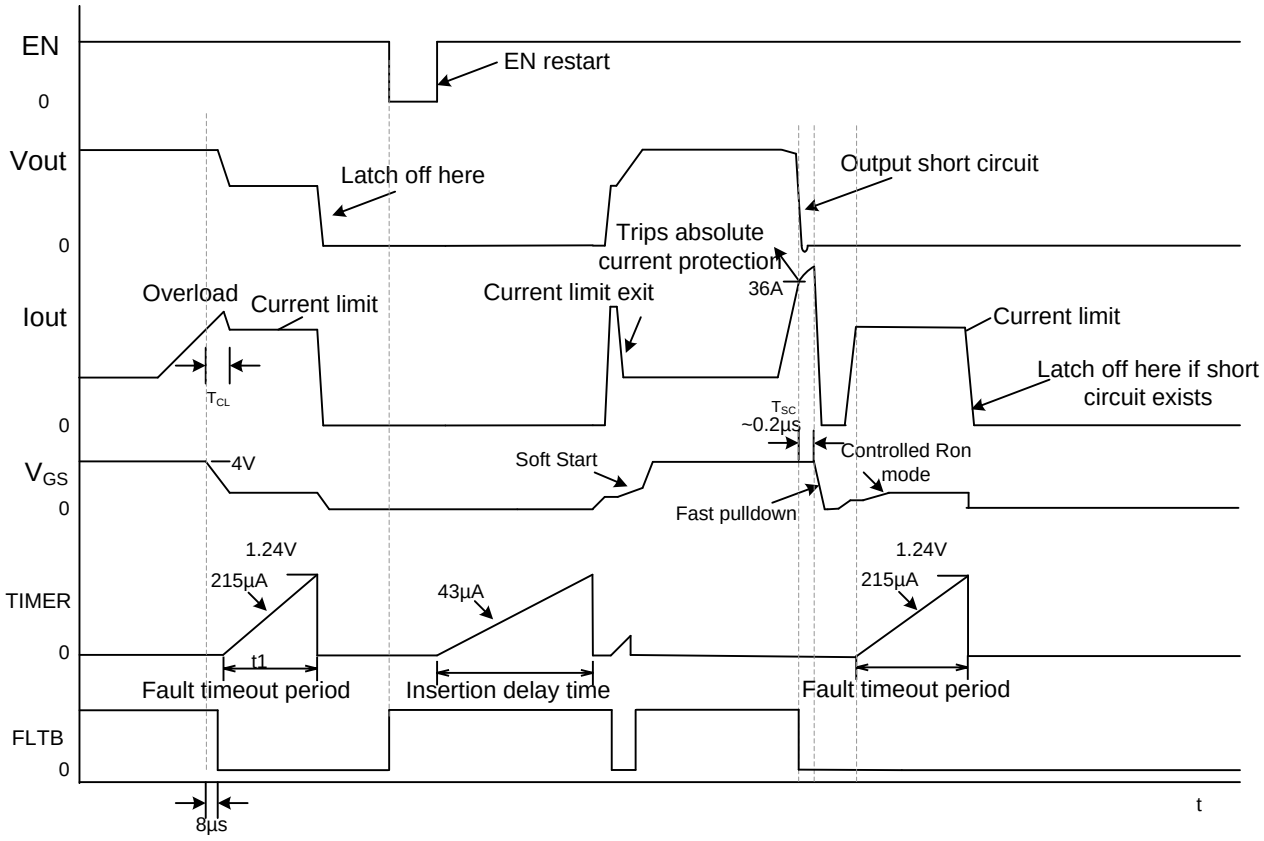


Figure 2: Over-Current Protection

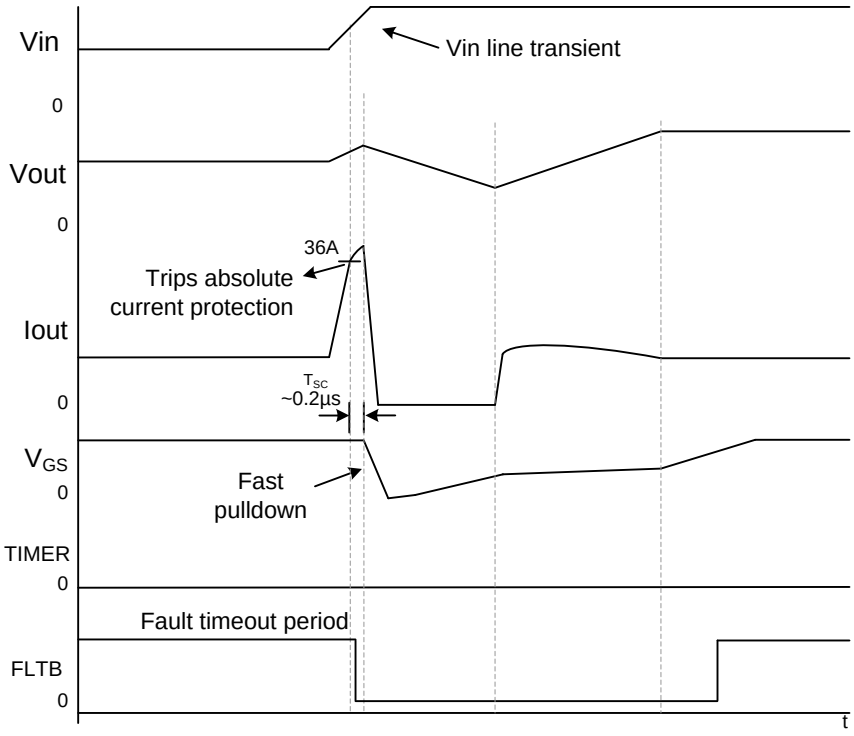


Figure 3: V_{IN} Line Transient Response

Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range relative to the input voltage. PG is also the open drain of the FET. Pull PG up to the external power supply through a 10-100kΩ resistor. During start-up, the power good output is driven low. This instructs the system to remain off and minimize the load on VOUT to reduce inrush current and power dissipation at start-up.

The power-good signal is pulled high when the device meets the following conditions:

- V_{OUT} > 90% * V_{IN}
- V_{GS} > 3V
- V_{OUT} > V_{IN} - 0.8V

Once these conditions are met, the system can then draw full power.

When V_{OUT} < 75% * V_{IN}, PG is switched low. The PG output is pulled low when EN is below its threshold. With no input, PG stays at a logic low level in the presence of a pull-up supply.

Fault Bar (FLTB)

Fault bar (FLTB) is an open-drain output used to indicate that a fault has occurred. Pull FLTB up to an external power supply through a 10-100kΩ resistor.

When the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold or the MOSFET is shorted before power-up, the fault output is driven low with an 8µs propagation delay. If a short circuit occurs and the 36A secondary current limit is reached, the FLTB is switched low immediately.

FLTB goes high when the MP5025C resumes normal operation. This means that the output voltage is higher than the setting voltage of the PG rising threshold, and the power FET is fully on (V_{GS} > 3V).

External Pull-Up Voltage for PG and FLTB

PG and FLTB require an external power supply. The open-drain output of PG can work from the external pull-up voltage, even when V_{IN} = 0 and EN is disabled. Use a 10-100kΩ pull-up resistor for PG and FLTB.

Power-Up Sequence

For hot-swap applications, the input of the MP5025C can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. To help stabilize the input voltage, an insertion delay is implemented before the main FET is turned on. TIMER charges the external capacitor (C_T) through a 43µA constant current source when the input voltage reaches the UVLO threshold (see Figure 4). The insertion delay finishes when the TIMER voltage reaches 1.24V. The capacitance of C_T can be determined with Equation (2):

$$C_T = \frac{43 \times t_{delay}}{1.24} \quad (2)$$

Where C_T is the insertion delay timer capacitance (nF), and t_{delay} is the insertion delay (ms). For example, a 100nF capacitor yields an insertion delay timer of 2.9ms.

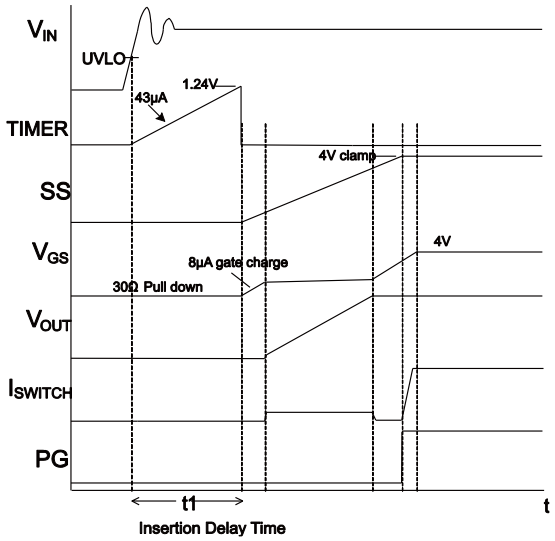


Figure 4: Start-Up Sequence

This insertion delay timer capacitor also determines the fault timer, as specified in the Fault Timer and Restart section on page 12.

After TIMER reaches 1.24V, an 8µA current source pulls up the power FET's gate-source voltage. Meanwhile, the TIMER voltage is discharged to zero. Once the gate voltage reaches its threshold (V_{GSTH}), the output voltage begins to rise. The rise time is determined by the soft-start capacitor.

Soft Start (SS)

A capacitor connected to SS determines the soft-start time. When the insertion delay time ends, a constant-current source proportional to the input voltage charges up the SS voltage. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value can be calculated with Equation (3):

$$C_{SS} = \frac{6 \times t_{SS}}{R_{SS}} \quad (3)$$

Where t_{SS} is the soft-start time, and R_{SS} is 1.1MΩ. For example, a 47nF capacitor gives a soft-start time of 8.6ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time exceeds the current limit. In this case, the rise time is controlled by the load capacitor and the current limit.

Float SS to generate a fast ramp-up voltage. An 8μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time. The approximate soft-start time (1ms) is the minimum soft-start time.

Enable and LOADEN

EN and LOADEN are used to control the on/off status of the MP5025C (see Table 1).

During the LOADEN blanking time, EN = 1 alone is sufficient to turn on the switch. After the LOADEN blanking time expires, both EN = 1 and LOADEN = 1 are required to turn on the switch. At all times, EN = 0 turns off the switch. Recycle EN or VIN to restart the chip once it is latched off.

Table 1: EN/LOADEN Blanking Time

LOADEN blanking time over?	EN	LOADEN	Status
N	0	0	Off
N	0	1	Off
N	1	0	On
N	1	1	On
Y	0	0	Off
Y	0	1	Off
Y	1	0	Off
Y	1	1	On

Please note that LOADEN is used to shut down the power switch after the LOADEN blanking time, but LOADEN cannot turn on the power switch by recycling LOADEN only (see Figure 5).

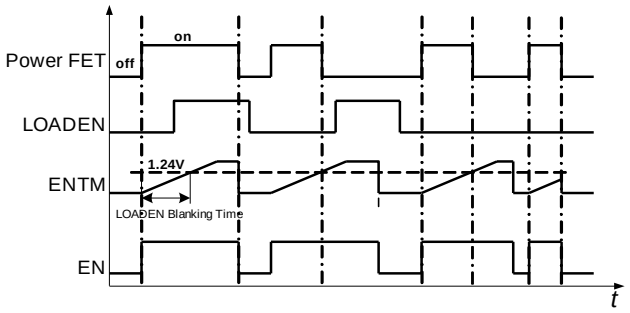


Figure 5: EN/LOADEN Timing Diagram

EN is pulled high internally with a 2μA internal pull-up current source.

Once the part is enabled, the insertion delay timer starts. When the insertion delay time ends, the internal 8μA current source charges the power FET's gate. Charging takes about 1ms for V_{GS} to reach its threshold. Then the output voltage rises following the SS controlled slew rate.

LOADEN Blanking Time

Supposing EN is high, LOADEN has a programmable blanking time that prevents LOADEN from de-asserting during the blanking time (see Figure 6). All fault functionality is operative during start-up, so the power switch shuts down if a fault is detected. However, LOADEN going low during this blanking time will not turn off the switch. At the end of the blanking time, LOADEN operates normally.

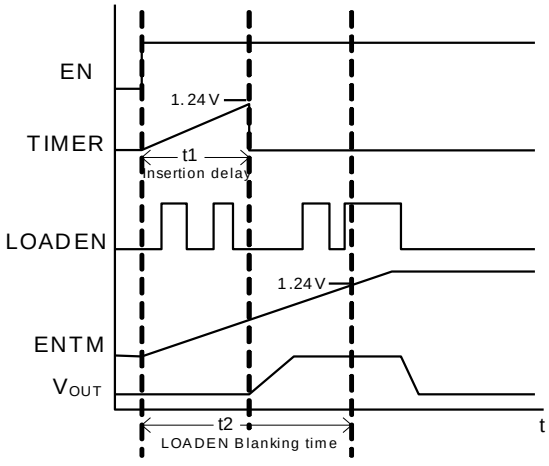


Figure 6: LOADEN Blanking Time

The blanking time can be set by a capacitor connected to ENTM. The blanking timer capacitor is calculated with Equation (4):

$$C_{ENTM} = \frac{t_{LDNB} \times 10^{-6}}{1.24} \quad (4)$$

Where t_{LDNB} is the LOADEN blanking time, and C_{ENTM} is the LOADEN blanking time capacitor on ENTM. For example, a 1μF capacitor gives a blanking time of 1.24s.

Connect ENTM to GND if not used LOADEN.

Input-to-Output Short-Circuit Detection

The MP5025C can detect a main pass FET during power up by treating an output voltage exceeding V_{IN} - 0.8V during start-up as a short on the MOSFET. FLTB goes low to indicate a fault condition and the power switch is held off. Once $V_{OUT} \leq V_{IN}$ - 0.8, the part starts up normally.

Internal VCC SUB Regulator

The MP5025C has an internal 4V linear sub-regulator that steps down the input voltage to generate a 4V bias supply that powers low-voltage circuitry. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high.

AVIN

AVIN is the power supply for the internal VCC sub-regulator. Connect a 49.9Ω resistor from VIN to AVIN and a 2.2μF bypass capacitor to GND to guarantee full operation in the event VIN collapses during a strong short from VOUT to GND. VIN has UVLO protection, but AVIN does not provide UVLO protection. Do not use AVIN alone to power off the MP5025C. The AVIN supply current is 500μA, typically.

Over-Voltage Lockout (OVLO)

The MP5025C monitors the supply voltage through OV pin for input over-voltage conditions. An external resistive divider from VIN to OV provides flexibility for setting the over-voltage lockout threshold.

When the voltage on OV pin exceeds 1.24V, the internal MOSFET is shut down, and the output is disabled. When the voltage on OV pin falls below 1.24V-V_{OV_HYS}, internal MOSFET is turned on again and the output ramps up with a soft-start.

Under-Voltage Lockout (UVLO)

If the supply (input) falls below the under-voltage lockout (UVLO) threshold, the output is disabled and PG goes low.

When the supply exceeds the UVLO threshold without exceeding the OV threshold, the output is enabled.

Monitoring the Output Current

IMON provides a current proportional to the output current (the current through the power device). The gain of the current sense amplifier with 10μA/A, which means that for every amp the main FET conducts, IMON provides 10μA of current. Placing a 10kΩ resistor to ground creates a voltage between 0V and 2V when the MOSFET current ranges from 0A to 20A. The voltage compliance for IMON is from 0V to 3V. Place a capacitor more than 10nF in parallel with R_{MON} during application.

APPLICATION INFORMATION

Current Limit Set (R_{SET})

The MP5025C current limit value should be higher than the normal maximum load current, allowing for tolerances in the current sense value. The current limit can be set using Equation (5):

$$I_{LIMIT} = \frac{1.3(V)}{R_{SET}} \times 10^5 (A) \quad (5)$$

When the current limit is set lower than 7A, place an R-C circuit in parallel with the ISET resistor (see Figure 7). Generally, choose R = 20kΩ and C = 560pF.

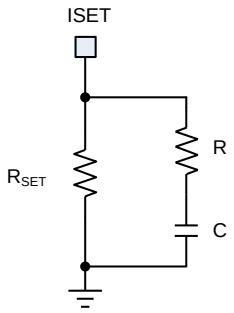


Figure 7: R-C Filter Circuit for ISET

Figure 8 shows a quick graphical view of the R_{SET} resistor value vs. the desired current when the desired current limit is greater than 7A. Table 2 provides the bench results for the evaluation board.

Table 2: Current Limit vs. Current Limit Resistor

Current limit resistor (kΩ)	6.8	16.2	32.4
Current limit (A)	19	8	4.06

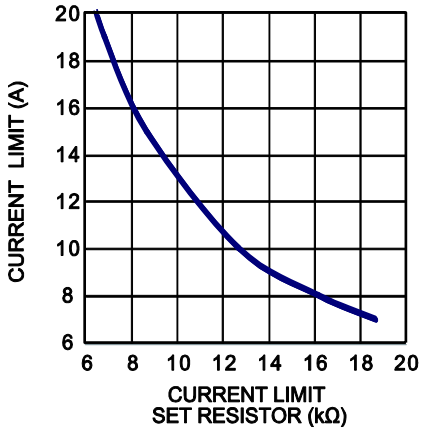


Figure 8: Current Limit vs. R_{SET} Value (Current Limit ≥7A)

Figure 9 shows a graphical view of the RSET resistor vs. the current limit for currents 7A and below.

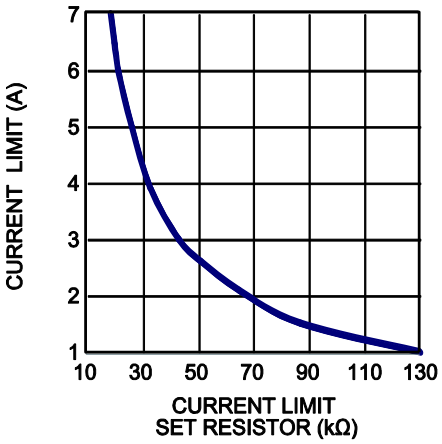


Figure 9: Current Limit vs. R_{SET} Value (Current Limit <7A)

Current Monitor Set

The MP5025C can monitor the power MOSFET current. Place a resistor (R_{MON}) to ground to set the gain of the output. The theory equation is shown with Equation (6):

$$I_{MON} = \frac{I_{POWER\_FET}}{10^5} (A) \quad (6)$$

Where I_{POWER_FET} is the current flowing from the power MOSFET. Placing a 10kΩ resistor from IMON to GND can achieve 100mV/A. Place a capacitor more than 10nF from IMON to GND to smooth the indicator voltage.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 10 and follow the guidelines below.

1. Place the high current path from the board's input to output and the current return path in parallel with a minimized loop to reduce the loop inductance.
2. Place a transient voltage suppressor diode (TVS) at VIN.
3. Place TVS as close as possible to VIN.

   TVS is used to absorb the input voltage spike from the system input line spike or when the load current of the MP5025C decreases sharply, which generates a voltage spike at VIN.
4. Connect the MP5025C's GND to a small GND island, in which all the signal GNDs of the part are referenced.

   This signal GND island can be connected to the main PWR GND of the system via a single point grounding method.
5. Ensure that the input decoupling capacitors on VIN have a minimal trace length to VIN and to GND.
6. Place the Schottky diode close to VOUT and GND to absorb negative voltage spikes when the power FET is shut off.
7. Place output capacitors as close to the MP5025C as possible to minimize the effect of PCB parasitic inductance.
8. Keep the IN and GND pads connected with large coppers.
9. Place vias on the thermal pad to achieve better thermal performance.
10. Ensure that all VIN and VOUT pins are connected to achieve equal current distribution of each lead or pin.

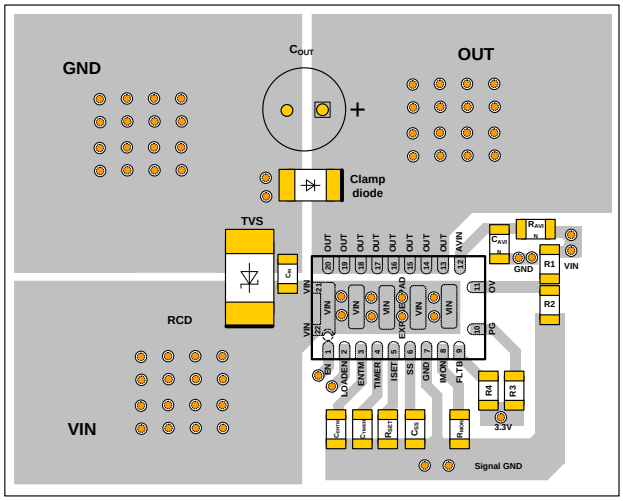


Figure 10: Recommended Layout

Design Example

The detailed application schematic is shown in Figure 11, Figure 12 and Figure 13. Figure 11 shows the application circuit for applications over the current limit ≥7A. Figure 12 is the application circuit for applications over the current limit <7A. Figure 13 is the application circuit with LOADEN unused. The typical performance and waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

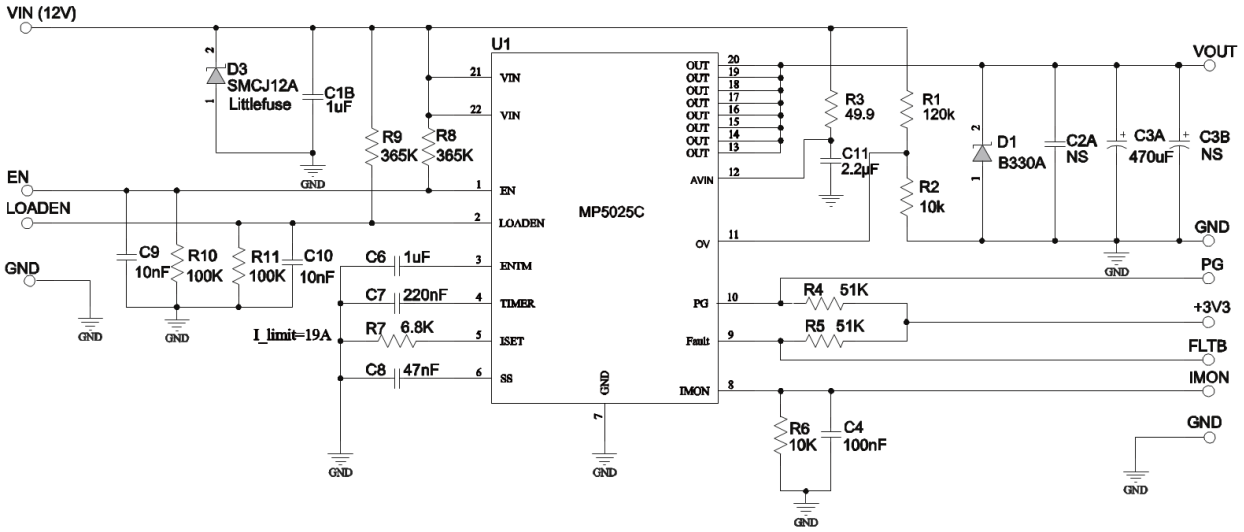


Figure 11: Over-Current Limit ≥7A Applications

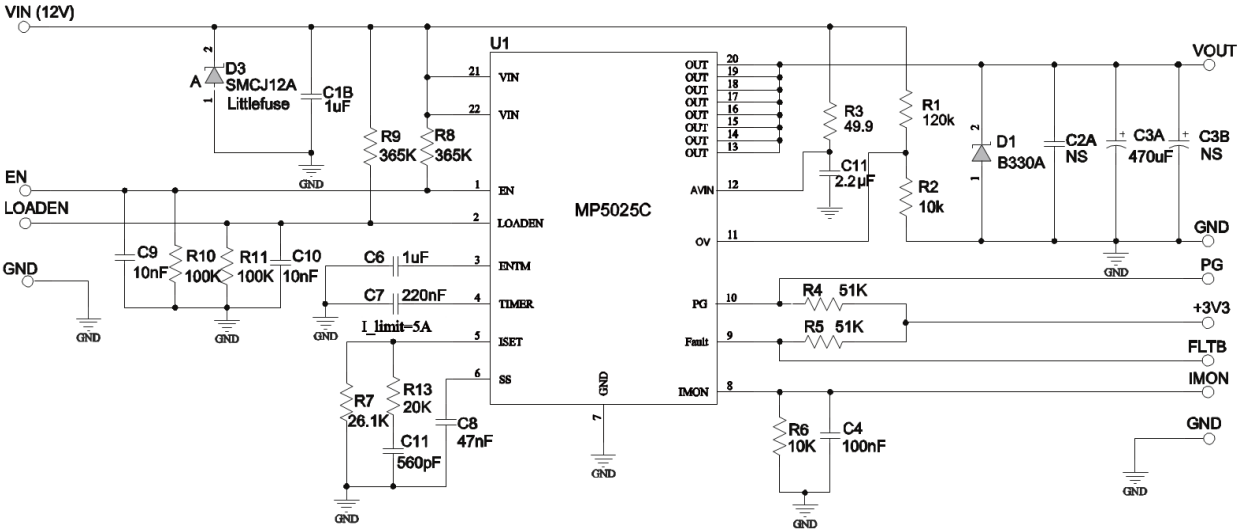


Figure 12: Over-Current Limit <7A Applications

TYPICAL APPLICATION CIRCUITS *(continued)*

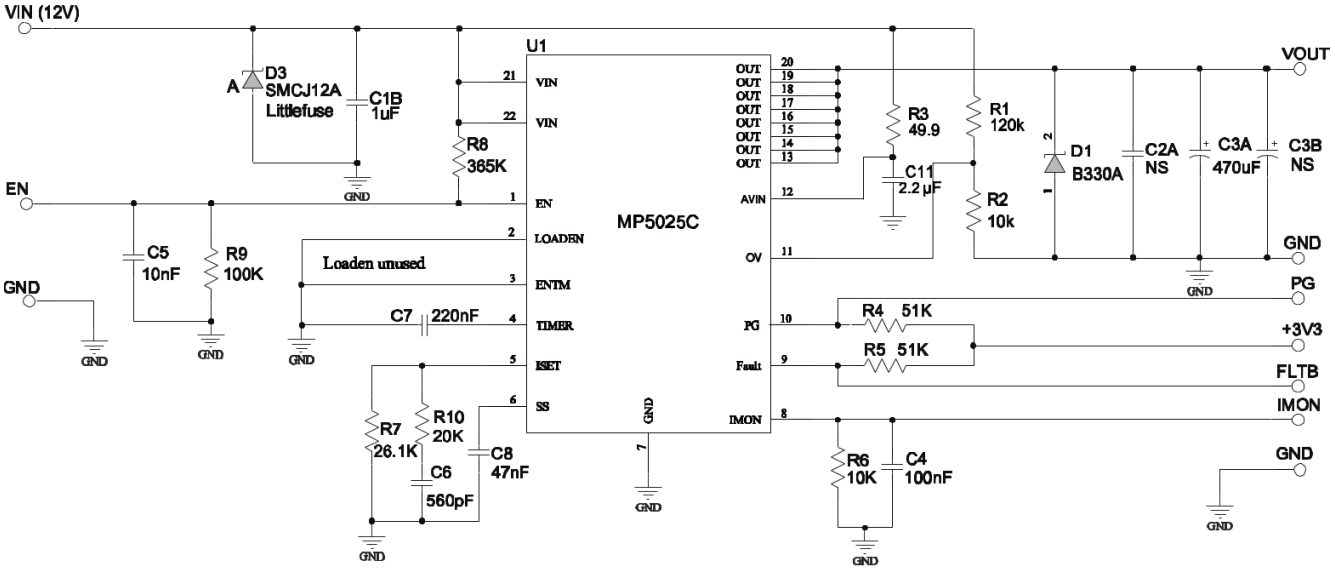
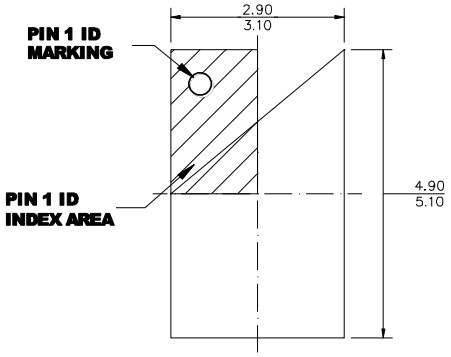


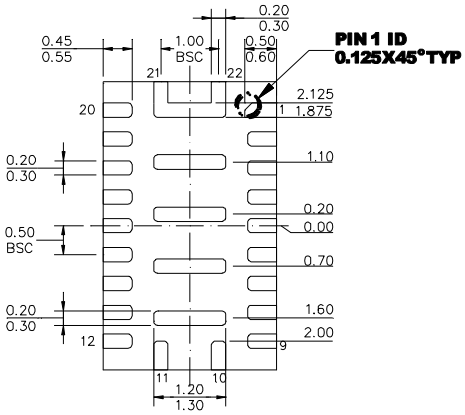
Figure 13: LOADEN Not Used

PACKAGE INFORMATION

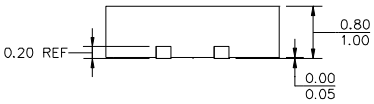
QFN-22 (3mmx5mm)



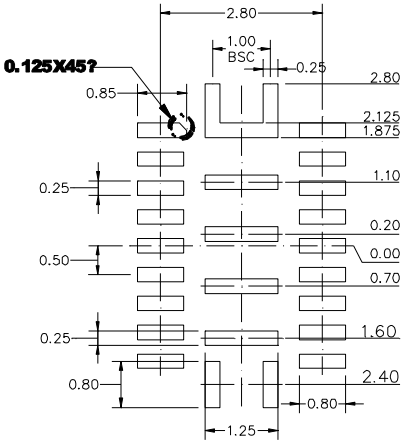
TOP VIEW



BOTTOM VIEW



SIDE VIEW

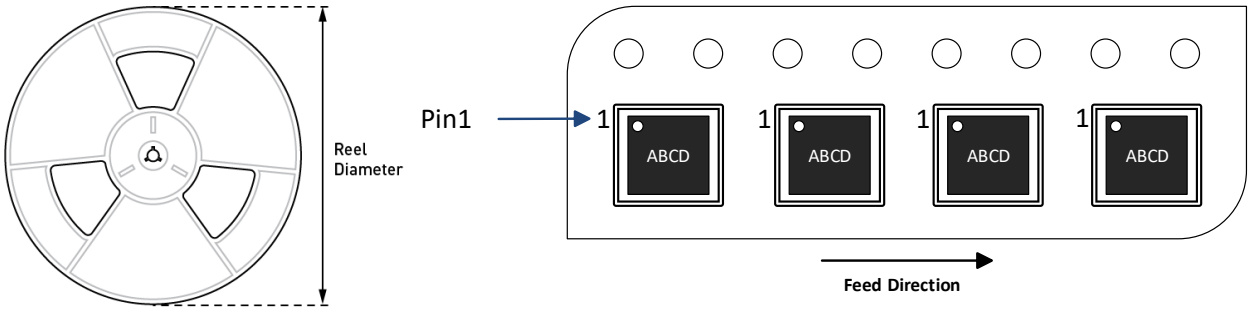


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5025CGQV-Z	QFN-22 (3mmx5mm)	5000	N/A	N/A	13 in.	12 mm	8 mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	11/06/2020	Initial Release	-