MP5505A

7V, 4A, High-Efficiency Energy Storage and Management Unit

The Future of Analog IC Technology

DESCRIPTION

The MP5505A is a lossless energy storage and management unit targeted at solid-state and hard-disk drive applications. Its highly integrated input current limit and energy storage and release management makes the system solution very compact.

The internal input-current-limit block with dv/dt control prevents inrush current during system start-up; the bus voltage start-up slew rate is programmable. Also, it includes a power-on-reset function for hot-swapping. MPS' patented energy storage and release management control circuit minimizes the storage capacitor requirement. It pumps the input voltage to a higher storage voltage and releases the energy over a hold-up time to the system in the case of an input outage. The storage voltage and the release voltage are both programmable for different system applications.

The MP5505A requires a minimal number of readily available, standard, external components and is available in a QFN-20 (3mm x 4mm) package.

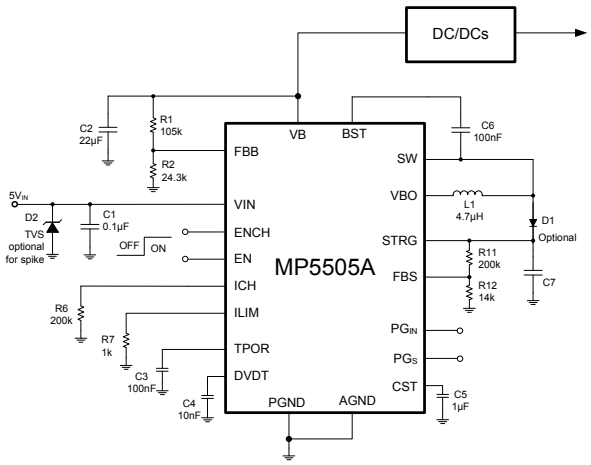
FEATURES

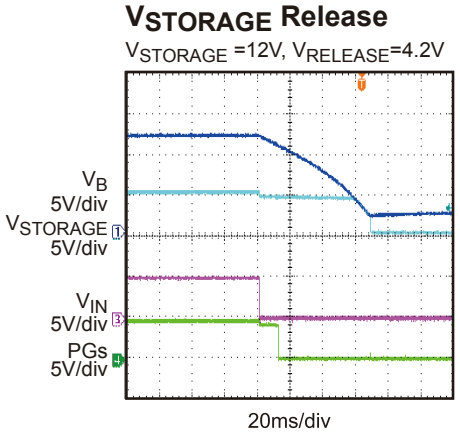
- Wide 2.7V to 7V Operating Input Range
- Input Current Limiter with Integrated 50mΩ MOSFET
- Up to 4.5A Input Current Limit
- Reverse-Current Protection
- 6V Bus Clamping Voltage
- Power-On-Reset
- Adjustable dv/dt Slew Rate for Bus Voltage Start-Up
- Internal 30mΩ Disconnect Switch
- Internal 70mΩ and 60mΩ Power Switches for Energy Storage and Release Management Circuits
- Thermal Protection
- EN and Power Good Indicators
- Available in a QFN-20 (3mm x 4mm) Package

APPLICATIONS

- Solid-State Drives
- Hard-Disk Drives
- Power Back-Up/Battery Hold-Up Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5505AGL	QFN-20 (3mmx4mm)	*See Below*

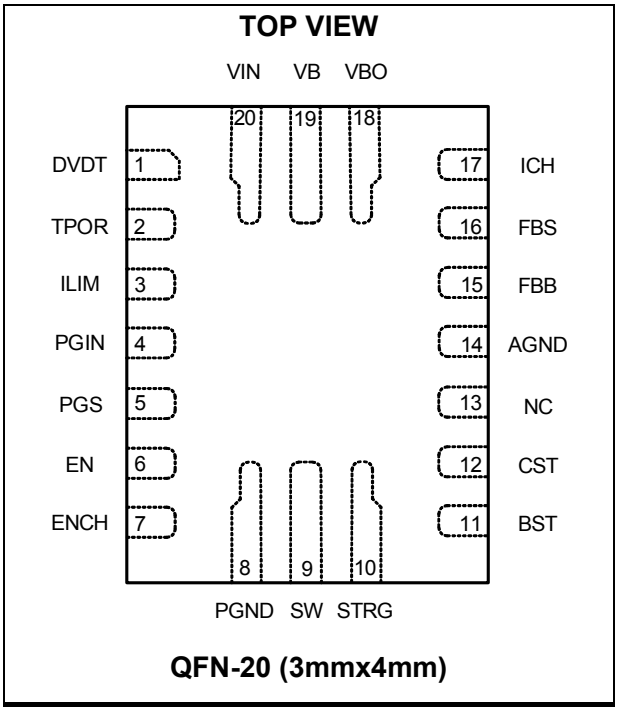
* For Tape & Reel, add suffix –Z (e.g. MP5505AGL–Z);

TOP MARKING

MPYW
5505
ALLL

MP: MPS prefix;
Y: year code;
W: week code:
5505A: first five digits of the part number;
LLL: lot number;

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 8.0V
V_{STRG} ..... -0.3V to 35V
V_{SW} ..... -0.3V to V_{STRG}+0.3V
V_{BST} ..... -0.3V to V_{STRG}+6.5V
V_{CST} ..... -0.3V to 40V
All Other Pins ..... –0.3V to 6.5 V
Continuous Power Dissipation (T_A = +25°C) (2) 2.6W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Operating Temperature ..... –40°C to +85°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 7V
Bus Voltage V_B ..... 2.7V to 6V
Storage Voltage V_{STRG} ..... V_{IN} to 30V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm)	48	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input-Supply Voltage Range	V_{IN}		2.7		7	V
Supply Current (Shutdown)	I_S	V_{EN}=0V			2	μA
Supply Current (Quiescent)	I_Q	$V_{EN/ENCH}$=2V, $V_{FBB/FBS}$=1V			2	mA
Thermal Shutdown (6)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (6)	T_{HYS}			30		°C
VIN Under-Voltage Lockout Threshold Rising	$INUV_R$			2.5	2.7	V
VIN Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$		0.3	0.4	0.5	V
EN/ENCH UVLO Threshold Rising	EN_R				1.2	V
EN/ENCH UVLO Threshold Falling	EN_F		0.4			V
Current-Limit FET ON Resistance	R_{DSON} (7)	V_{IN}=5V, I_B=0.5A		50	65	mΩ
		V_{IN}=3.3V, I_B=0.5A		68	83	
Continuous Current Limit	I_{LIM}	R_{ILIM}=1.07kΩ		4.6		A
		R_{ILIM}=1.2kΩ		4.1		
		R_{ILIM}=1.4kΩ	-10%	3.7	10%	
Off-State Leakage Current	I_{LEAK}	V_{IN}=6V, V_B=0V or V_B=6V, V_{IN}=0V			2	μA
Clamping Voltage	V_{CLAMP}	V_{IN}=7V	+10%	6	+10%	V
Rise Time (dv/dt)	τ_R	DVDT Pin Floating	0.5	0.9	1.5	ms
		$C_{dv/dt}$=10nF		10		
		$C_{dv/dt}$=100nF		100		
Internal RESET Delay Time	τ_D	TPOR Pin Floating		0.4		ms
		C_{TPOR}=100nF		100		
		C_{TPOR}=500nF		500		
Pre-Charge Current	I_{CH_PRE}			130		mA
Charge Peak Current @ Boost Mode	I_{CH}	ICH Pin Floating		500		mA
		R_{ICH}=100kΩ		400		
		R_{ICH}=200kΩ		200		
Boost Disconnect Switch R_{on}	R_{dison}			30	35	mΩ
Energy Management HS R_{on}	R_{Hon}			70		mΩ
Energy Management LS R_{on}	R_{Lon}			60		mΩ
Feedback Voltage	V_{FBB}, V_{FBS}		0.77	0.79	0.81	V
Feedback Current	I_{FBB}	V_{FBB}=V_{FBS}=0.79V			50	nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG_S High Threshold	PG_{H_S}			0.95		V_{FBS}
PG_S Low Threshold	PG_{L_S}			0.9		V_{FBS}
PG_S Delay	PG_{D_S}			20		µs
PG_S Sink-Current Capability	V_{PG_S}	Sink 4mA			0.3	V
PG_S Leakage Current	I_{PGS_L}	V_{PGS}=3.3V			120	nA
PG_{IN} High Threshold	PG_{H_IN}			1.03		V_{FBB}
PG_{IN} Low Threshold	PG_{L_IN}			1		V_{FBB}
PG_{IN} Delay	PG_{D_IN}			4		µs
PG_{IN} Sink-Current Capability	V_{PG_IN}	Sink 4mA			0.3	V
PG_{IN} Leakage Current	I_{PGIN_L}	V_{PGIN}=3.3V			120	nA
Buck-Mode Dumping-Current Limit	I_{DUMP}			5		A
Release-Buck Switching Frequency	f_{s_RLS}			500		kHz
VB Under-Voltage Lockout Threshold, Rising(5)	$INUVB_R$		1.8	2.2	2.5	V
VB Under-Voltage Lockout Threshold, Hysteresis(5)	$INUVB_{HYS}$		0.15	0.25	0.35	V

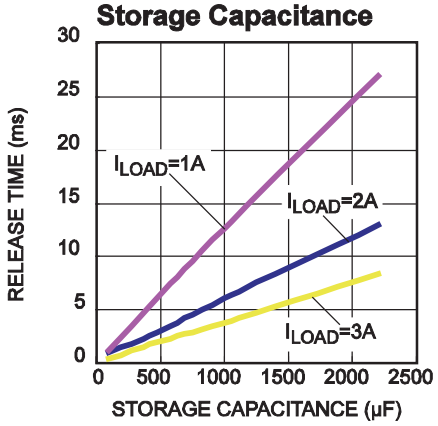
Notes:

5) VB UVLO is applied to energy storage and release circuitry.
6) Guaranteed by design.
7) Refer to TPC curve for Current-Limit FET On Resistance value under different temperature and load condition.

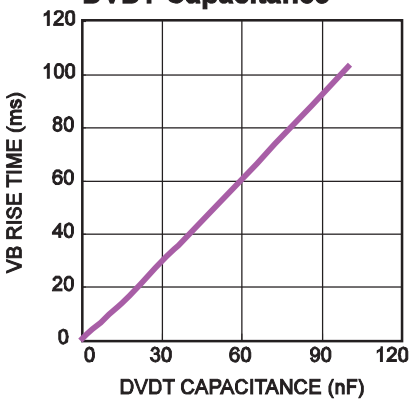
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$=4.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

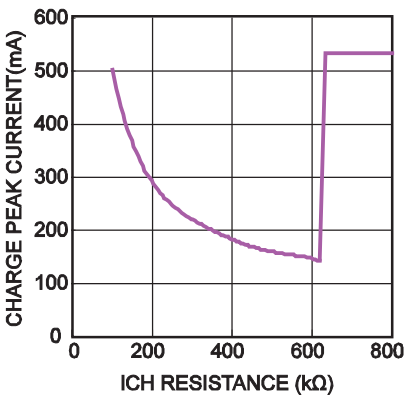
Release Time vs. Storage Capacitance



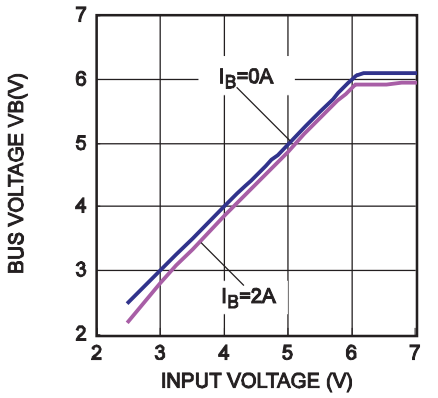
VB Rising Rate vs. DVDT Capacitance



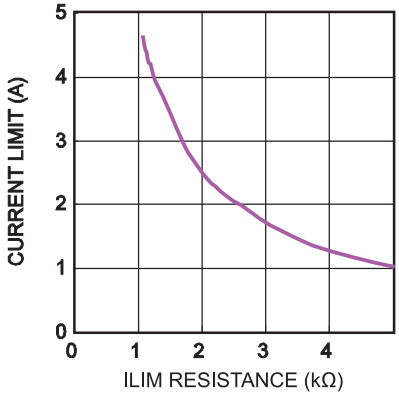
Boost Charge Peak Current vs. ICH Resistor



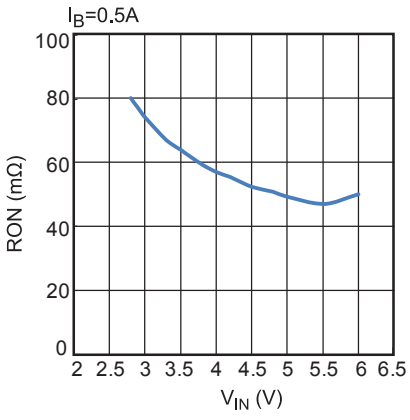
VB Bus Clamping Voltage



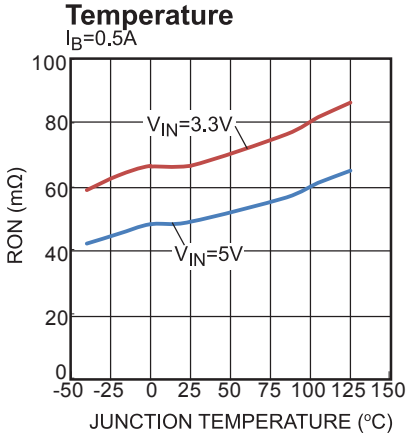
VIN to VB Current Limit



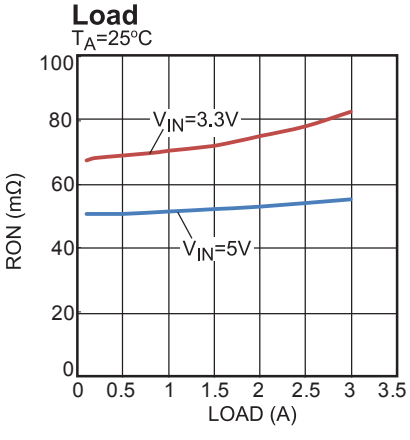
Input MOSFET RON vs.VIN



Input MOSFET RON vs. Temperature



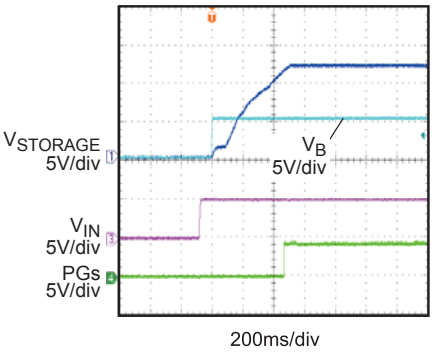
Input MOSFET RON vs. Load



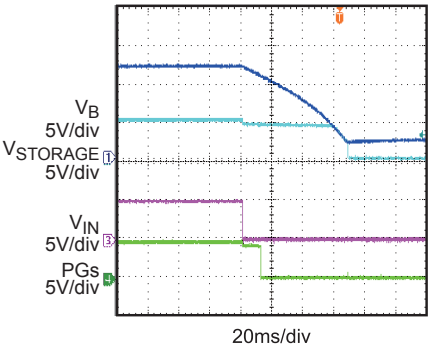
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$=4.2V, L = 4.7μH, T_A = 25°C, unless otherwise noted.

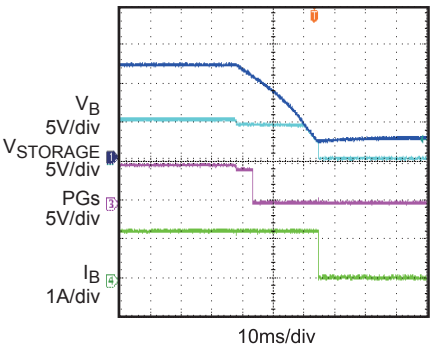
$V_{STORAGE}$ Charge



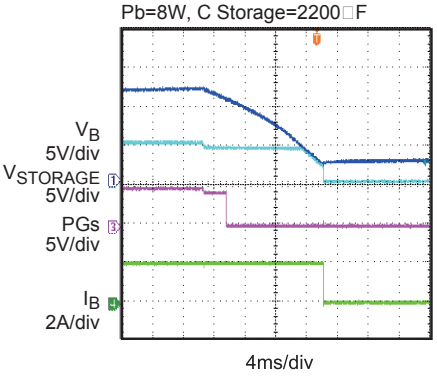
$V_{STORAGE}$ Release



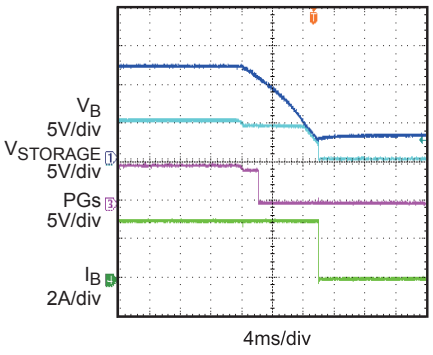
Release Time
Pb=5W, C Storage=2200□F



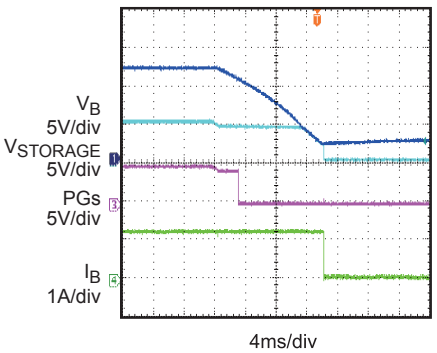
Release Time
Pb=8W, C Storage=2200□F



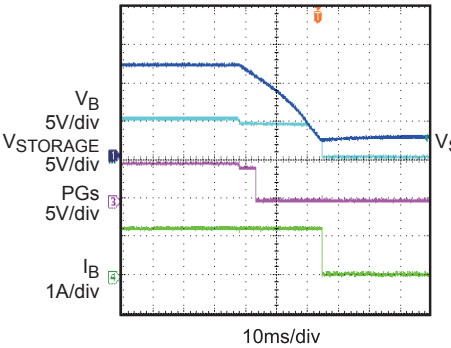
Release Time
Pb=12W, C Storage=2200□F



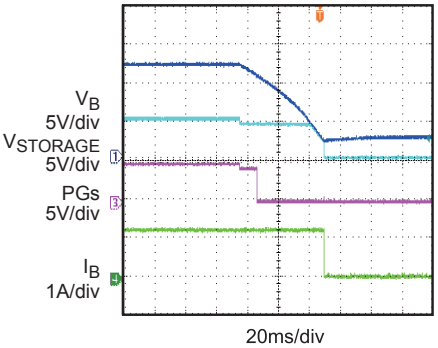
Release Time
Pb=5W, C Storage=1000□F



Release Time
Pb=5W, C Storage=2200□F



Release Time
Pb=5W, C Storage=4400□F



PIN FUNCTIONS

QFN-20 (3mm×4mm) Pin #	Name	Description
1	DVDT	Slew-Rate Control Pin for VB Voltage during Start-Up. Connect a capacitor from DVDT to GND to program a different VB charge-up slew rate. Leave DVDT open for the default soft-start time (around 0.9ms from 0V to VIN).
2	TPOR	Power-On-Reset Delay Time for VB Start-Up. When VIN and EN are ready (after the programmable delay time), VB starts to charge-up. Connect a capacitor between TPOR and GND to select a different delay time. Leave TPOR open for the default power-on-reset delay time (0.4ms).
3	ILIM	Input-Current-Limit Setting. Connect a resistor between ILIM and GND to adjust the current limit of the input-current limiter. ILIM CANNOT be left open.
4	PG_{IN}	VB Power Good Indicator. PG_{IN} is an open-drain output. PG_{IN} goes high if the FBB voltage exceeds $1.03\times V_{FBB}$ (0.813V, typically). PG_{IN} goes low if the FBB voltage drops below $1.0\times V_{FBB}$ (0.79V).
5	PG_S	Storage Voltage Power Good Indicator. PG_S is an open-drain output. PG_S goes high if the FBS voltage exceeds $0.95\times V_{FBS}$ (0.75V). PG_S goes low if the FBS voltage drops below $0.9\times V_{FBS}$ (0.71V).
6	EN	ON/OFF Control pin for MP5505A. When EN is pulled low, all functions of MP5505A are disabled (for both the input-current limiter and the charge/release circuitry). Make sure EN voltage is high during release.
7	ENCH	ON/OFF Control Pin for the Charge/Release Circuitry. When ENCH is pulled down, the release circuitry is disabled. *Note that ENCH needs to be kept high to achieve energy release.
8	PGND	Power Ground.
9	SW	Switch Output for the Charge/Release Circuitry. Connect a small inductor between SW and VBO.
10	STRG	Storage Voltage. Connect the appropriate storage capacitors for energy storage and release operation.
11	BST	Bootstrap Pin for the Charge/Release Circuitry. The internal bi-directional switcher requires a bootstrap capacitor (100nF) from BST to SW to supply the high-side switch driver voltage during release.
12	CST	High-Side Switch Driving Voltage Storage. MP5505A supports energy even when storage voltage is close to the VB regulated voltage.
13	NC	No Connection.
14	AGND	IC Signal Ground.
15	FBB	Bus-Voltage Feedback Sense. FBB sets the bus-release voltage.
16	FBS	Storage-Voltage Feedback Sense. FBS sets the storage voltage.
17	ICH	Boost-Mode Current Limit Adjustment. ICH CANNOT be pulled to VCC or pulled to an external voltage source.
18	VBO	Internal Boost. The input voltage after passing through the input isolation FET.
19	VB	Internal-Bus Voltage. Requires a 22µF to 47µF ceramic capacitor as close to VB as possible.
20	VIN	Input-Supply Voltage. The MP5505A operates from an unregulated 2.7V to 7V input. Place a 0.1µF (or larger) ceramic capacitor as close to VIN as possible. A TVS diode at input is necessary if the VIN voltage spike is high. Refer to the “Selecting Input Capacitor and TVS” section for additional details.

FUNCTIONAL BLOCK DIAGRAM

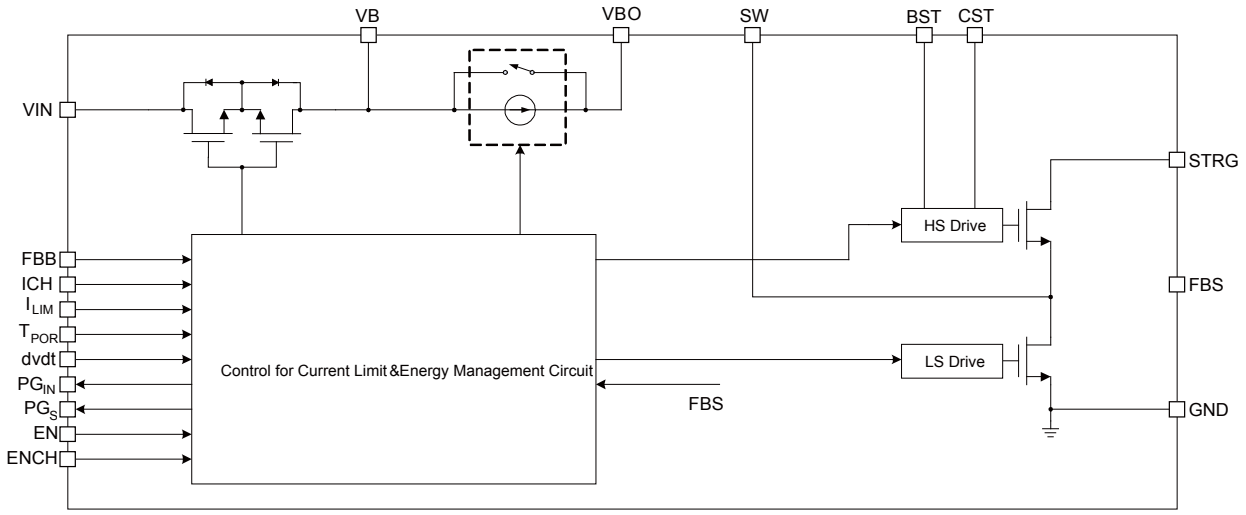


Figure 1. Functional Block Diagram

OPERATION

The MP5505A is an energy storage and management unit in a QFN-20 (3mm×4mm) package. It provides a very compact and efficient energy management solution for typical solid-state drive or hard-disk drive applications. MPS patented lossless energy storage and release management circuits use a bi-directional buck/boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter raises the energy-storage voltage level. The storage feedback resistor divider sets the storage voltage. If the input shuts down suddenly, the internal buck converter transfers the energy from the storage capacitor to the bus and holds the bus voltage when the system consumes the energy from the storage capacitor. The buck converter can work in 100% duty cycle operation to deplete fully the stored energy.

Start-Up

When VIN starts-up, the VB bus voltage is charged from 0 to VIN (nearly). The VB rising slew rate is controlled by DVDT capacitance. This function avoids the input-inrush current and provides protection to the whole system.

EHCH is used to enable the storage charge and release circuitry. If ENCH is already high before VB finishes the DVDT process, the storage charge circuitry works automatically when VIN is higher than the UVLO (2.5V, typically).

The storage charge circuitry operates in two modes: pre-charge mode (where the STRG voltage is charged to the VB voltage using a current source) and boost mode (where the STRG voltage is charged to set the voltage). The pre-charge mode charges the STRG voltage up to the VB voltage using an almost constant current source (around 130mA). When STRG voltage is close to VB and VB voltage is higher than a certain threshold (where the corresponding FBB is higher than 0.813V), boost mode is initiated.

Boost mode charges the STRG voltage to the target voltage. Figure 2 shows the charging build-up process when ENCH is high before VB starts up.

It is recommended strongly to enable ENCH after VB has settled (see Figure 3). Because release mode is triggered when FBB voltage is lower than 0.79V (although there is a 23mV hysteresis between boost mode and release mode, in some high-current charges boost mode can be programmed by ICH), VB voltage may be pulled back low and accidently enter release mode. In order to avoid this, enable ENCH after VB settles. Figure 3 shows the charging build-up process when ENCH is enabled after VB settles.

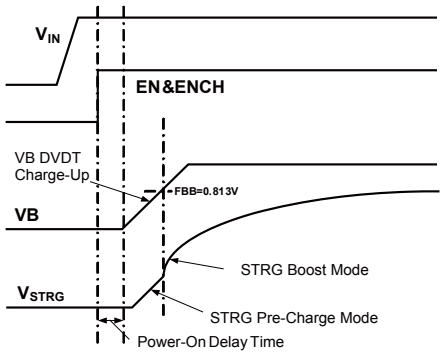


Figure 2. Charging Process

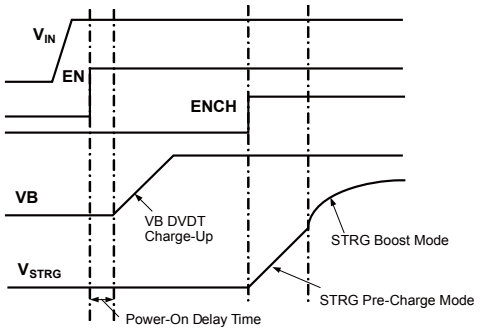


Figure 3. Charging Process when EN and ENCH Are Separated

Storage Voltage

After the start-up period, the internal boost converter regulates automatically the storage voltage to a set value. The MP5505A uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode initiates and charges

the storage capacitor. During the burst period, the current limit and the low-side MOSFET (LS-FET) control the switch. When the LS-FET turns on, the inductor current increases until it reaches its current limit. The boost-current limit can be programmed by an ICH resistor. By floating ICH, the boost-current limit is around 500mA. After hitting the current limit, the LS-FET turns off for the set minimum off-time. At the end of this minimum off-time, if the feedback voltage remains below the 0.79V internal reference, the LS-FET turns on again; otherwise the MP5505A waits until the voltage drops below the threshold before turning on the LS-FET.

Release

The MP5505A monitors continuously the input and bus voltages. Once the bus voltage drops below the selected release voltage (such as when losing input power), the internal boost converter stops charging and works in buck-release mode. In buck mode, the part transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. Determine the release voltage by selecting resistor values for the bus resistor divider.

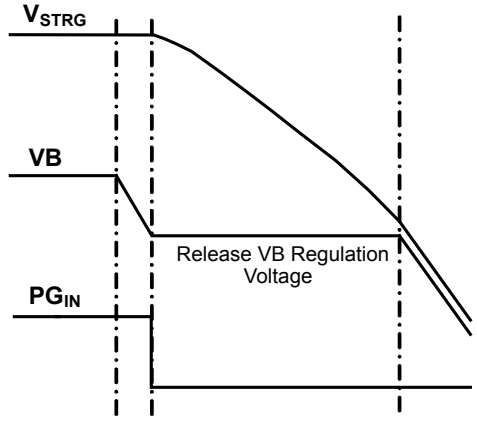


Figure 4. Release Times

The released buck applies the fixed-frequency constant-on-time (COT) control and enables the fast transition between the charge and release modes. The buck converter works at 100% duty cycle until the storage-capacitor voltage approaches the bus voltage. Then the storage and bus voltages drop until they reach the DC-DC converter's UVLO (see Figure 4).

Input-Current Limit

The input-current limiter controls carefully the input-inrush current of the internal hot-swap MOSFET to prevent an inrush current from the input to the bus. A capacitor connected to dv/dt sets the soft-start time. Despite the soft-start process, ILIM can limit the steady-state current. Connect a resistor between ILIM and GND to set the current limit.

Reverse-Current Protection

The hot-swapping circuit uses reverse-current protection to prevent the storage energy from transferring back to the input when energy is released from the storage capacitors to bus. The hot-swap MOSFET turns on when the input voltage exceeds the VIN UVLO threshold during start-up (or when input voltage is about 0.2V higher than VB voltage). The hot-swap MOSFET turns off when input voltage falls below the bus voltage during release (or input falls below the PG_{IN} threshold).

Start-Up Sequencing

Connect a capacitor across DVDT to program the soft-start time; during soft-start, the energy storage capacitors will charge. Very short dv/dt times can trigger the current-limit threshold. Select the DVDT capacitor based on the storage capacity.

Storage Power-Good Indicator (PG_S)

When the voltage on FBS (storage feedback) drops below $0.9\times V_{FBS}$, the MP5505A pulls PG_S low internally. When the FBS voltage is above $0.95\times V_{FBS}$, PG_S goes high.

Bus Power-Good Indicator (PG_{IN})

When the voltage on FBB (bus feedback) falls below $1.0\times V_{FBB}$, the MP5505A pulls PG_{IN} low to indicate the releasing status. When MP5505A works in boost mode, PG_{IN} is pulled high to indicate the charging status.

APPLICATION INFORMATION

Selecting Input Capacitor and TVS

Capacitors at VIN are recommended to absorb possible voltage spikes during input-power turn on, input-switch hard off (during power off), or other special conditions. The application determines the capacitor. For example, if the input-power trace is too long (with higher parasitic inductance) during the input-switch hard-off period, more energy pumps into the input. This means more input capacitors are needed to ensure the input voltage spike stays in a safe range. Use a 0.1uF (or larger) capacitor based on the spike condition.

Keep inrush-current requirements in mind when selecting an input capacitor. Typically, more input capacitors result in a higher input-inrush current during hot-plugging. A smaller input capacitor is needed for a smaller inrush current. MP5505A works normally with a very small input capacitor. However, this leads to a possible high-voltage spike. An efficient solution is to add a TVS diode at the input to absorb the possible input-voltage spike. At the same time, keep the inrush current small during hot-plugging. A typical TVS diode, like SMA6J5.0A, is recommended.

Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors R11 and R12 shown in Figure 5.

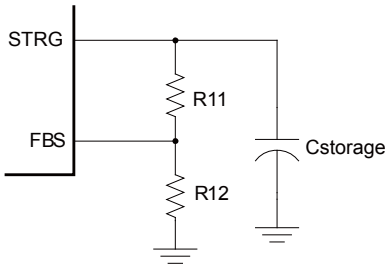


Figure 5. Storage Feedback Circuit

The storage voltage is determined by:

$$V_{STORAGE} = (1+\frac{R11}{R12}) \times V_{FBS}$$

Where V_{FBS} is 0.79V, typically. R11 and R12 are not critical for normal operation. Select R11 and R12 higher than 10kΩ to account for the bleed current. For example, if R12 is 14kΩ, R11 is then:

$$R11 = \frac{14k\Omega \times (V_{STORAGE} - V_{FBS})}{V_{FBS}}$$

For a 12V storage voltage, R11 is 200kΩ.

Table 1 lists the recommended resistors for different storage voltages.

Table 1. Resistor Pairs for $V_{STORAGE}$

$V_{STORAGE}$(V)	R11 (kΩ)	R12 (kΩ)
8	127	14
12	200	14
20	340	14

Select Release Voltage and VBus Capacitors

Select the release voltage by choosing the external feedback resistors R1 and R2 (see Figure 6).

Similarly, the release voltage is:

$$V_{RELEASE} = (1+\frac{R1}{R2}) \times V_{FBB}$$

V_{FBB} is 0.79V, typically. However, R1 and R2 not only determine the release voltage, but also affect stability. Since the release-buck mode works in COT mode, avoid small resistor values to ensure a sufficient voltage ramp. Generally, choose R1//R2≥20kΩ for stable performance with C_B=22μF. Table 2 lists the recommended resistor values for different release voltages.

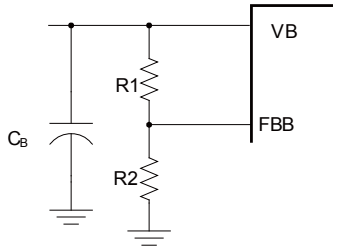


Figure 6. Release Feedback Circuit

Table 2. Resistor Pairs for $V_{RELEASE}$

$V_{RELEASE}$ (V)	R1 (kΩ)	R2 (kΩ)
4.2	105	24.3
2.9	107	40.2

Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases this energy to VB

when VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POS capacitor for most applications. One 4.7uF ceramic capacitor is recommended if the electrolytic capacitor ESR is high.

Select a storage capacitor with a voltage rating that exceeds the targeted storage voltage. Consider the capacitance reduction with the DC voltage offset when choosing the capacitors. Different capacitors have a different capacitance de-rating performance. Choose a capacitor with enough voltage rating to guarantee enough capacitance.

The required capacitance depends on the length of the "dying gasp" for a typical application. Assume the release current is $I_{RELEASE}$ when VB voltage is regulated at $V_{RELEASE}$ for the DC-DC converter, the storage is $V_{STORAGE}$, and the required dying gasp time is τ_{DASP}. The required storage capacitance is then:

$$C_S = \frac{2 \times V_{RELEASE} \times I_{RELEASE} \times \tau_{DASP}}{V_{STORAGE}^2 - V_{RELEASE}^2}$$

Consider the power loss during release; the buck converter can run up to 90% efficiency in most applications. Select storage capacitance at 1.1xCs to ensure enough releasing time. If $I_{RELEASE}$=1A, τ_{DASP}=20ms, $V_{STORAGE}$=12V, and $V_{RELEASE}$=4.2V, then the required storage capacitance is 1500μF.

For typical applications using a 5V input supply, set the storage voltage above 10V to utilize fully the high-voltage energy and minimize the storage capacitance requirements. Generally, use the 16V POS capacitor or 25V electrolytic capacitors.

Selecting the External Diode

An external diode parallel with the high-side power MOSFET (HS-FET) is optional for normal charge mode operation. This diode improves the boost efficiency if the boost peak current is high. The voltage rating should be higher than the storage voltage, and the current rating should be higher than the current programmed by ICH.

Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to GND to set the current-limit value. For example, a 1.2kΩ resistor sets the current limit to about 4.1A. Table 3 lists the recommended resistors for different current limit values.

Table 3. I_{LIM} vs. R_{LIM}

I_{LIM}(A)	R_{LIM} (kΩ)
4.6	1.07
4.1	1.2
3.7	1.4
1.6	3.2

Input Hot-swap Voltage Drop

MP5505A integrates one back-to-back MOSFET between VIN and VB for current limit and reverse current blocking. The voltage drop on this FET may affect application when VIN voltage is low. One load switch such as MP5090 is suggested to place in parallel with MP5005A input hot-swap MOSFET, as Figure 7 block diagram. In this application, OUT1 and OUT2 of MP5090 must be connected together without capacitor to GND. PGB of MP5505A will enable MP5090 and provide much lower resistance between VIN and VB power, while providing reverse current block at the same time.

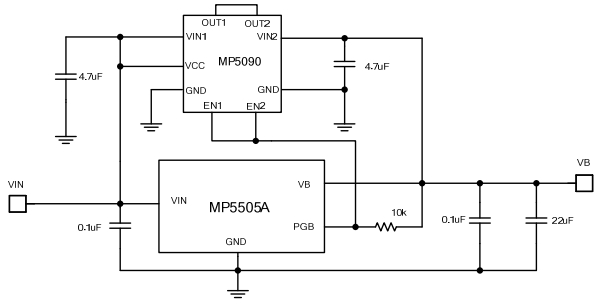


Figure 7. MP5505A parallel with MP5090

Selecting the Inductor

The inductor is necessary to supply constant current to the load. Since boost mode and buck mode share the same inductor, and generally the buck mode current is higher, an inductor that at least supports the buck mode releasing current is recommended.

Select the inductor based on the buck-release mode. If the storage voltage is V_S, then the release voltage is V_R and the buck running is fixed at a 500kHz frequency. The inductance value can be calculated by:

$$L = \frac{V_R}{\Delta I_L \times F_{SW}} \times (1 - \frac{V_R}{V_S})$$

Where ΔI_L is the peak-to-peak inductor-ripple current (which can be set in the range of 30% to 40% of the full releasing current).

The inductor should not saturate under the maximum inductor peak current.

Setting the Power-On Reset Delay Time

Connect a capacitor to TPOR to set the power-on-reset delay time. Leave TPOR floating for the default delay time (around 0.4ms). Table 4 lists the recommended capacitors for different delay times. In order to eliminate the power-on-reset delay, connect TPOR directly to VIN.

Table 4. Reset Delay vs. Capacitor Value

T_D (mS)	C_{TPOR} (nF)
100	100
500	500

Setting the Bus Voltage Rise Time

Connect a capacitor to the DVDT to set the bus voltage start-up slew rate and soft-start time. Leave DVDT floating for the default soft-start time (around 0.9ms from 0V to 5V). Table 5 lists the recommended capacitors for different soft-start times at a 5V input condition.

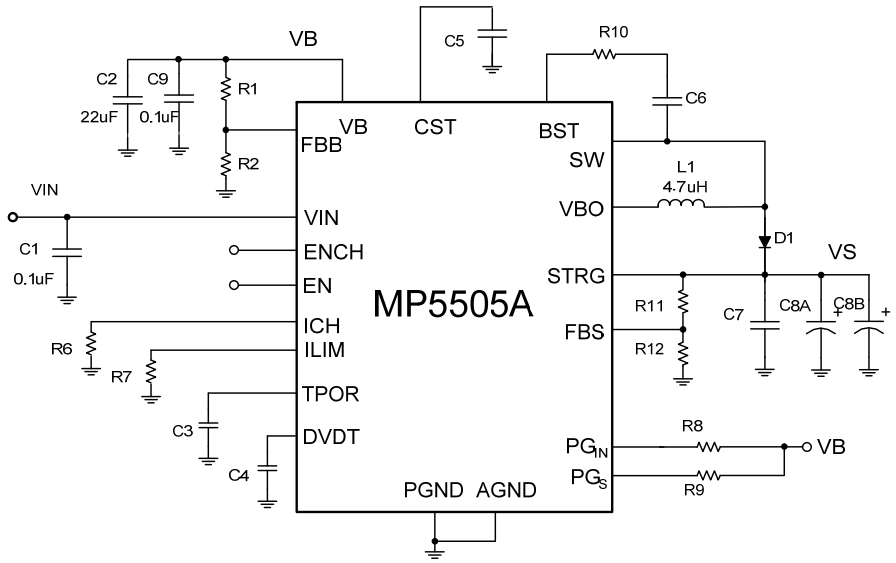
Table 5. Soft-Start vs. Capacitor Value

T_R (mS)	$C_{dv/dt}$ (nF)
10	10
100	100

PCB Layout

1) Use short, wide, and direct traces in the high-current paths (VIN, VB, VBO, SW, STRG, and GND).
2) Place the decoupling capacitor across VB and GND as close as possible.
3) Place the decoupling capacitor across STRG and GND as close as possible.
4) Keep the switching node SW short and away from the feedback network.
5) Place the external feedback resistors next to the FB pins.
6) Keep the BST voltage path (BST, C6, R10, and SW) as short as possible.

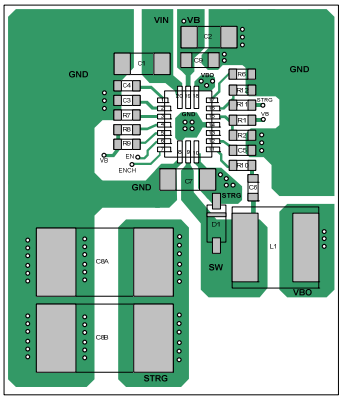
A 4-layered layout is recommended to achieve better thermal performance and simplify layout.



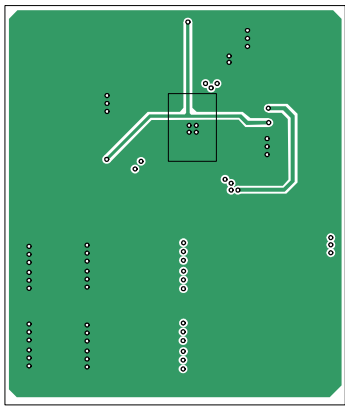
Schematic for Layout

Please use the following figures as a sample layout (with four layers).

Top Layer:



Inner Layer 2:



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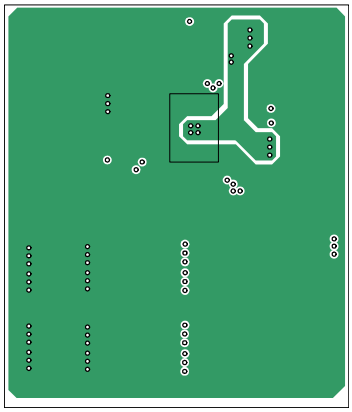


Bottom Layer:

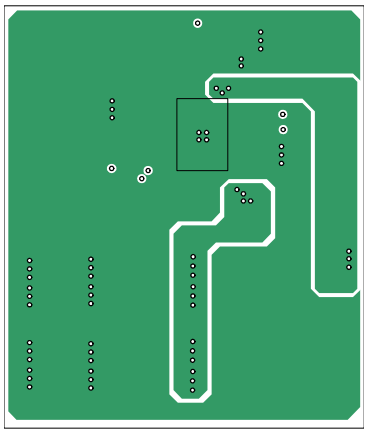


Figure 8. Layout Recommendation

Design Example

Table 6 below is a design example following the application guidelines for the specifications:

Table 6. Design Example

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	5	V
Charge Voltage	V_{STRG}	12	V
Regulated-Bus Voltage at Pfail	V_{RLS}	4.2	V
Boost Mode Max Charge Current	I_{CHARGE}	0.5	A
Buck Mode Max Output Current at Pfail	$I_{RELEASE}$	3	A

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section on page 6. For more device applications, please refer to the related evaluation board datasheets.

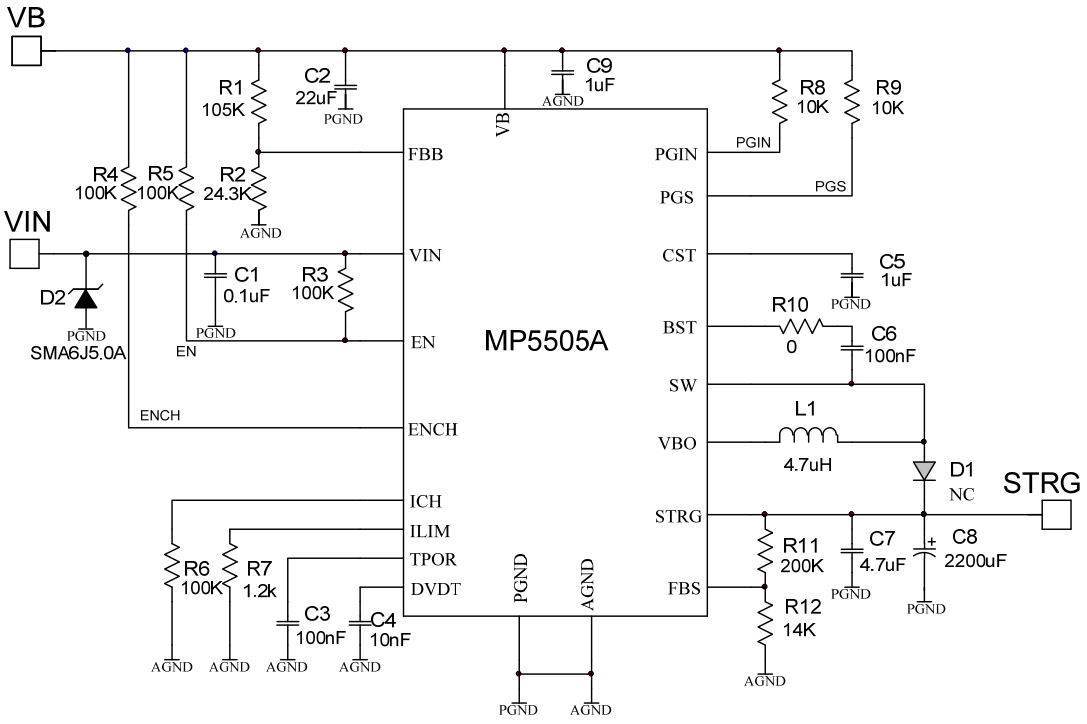
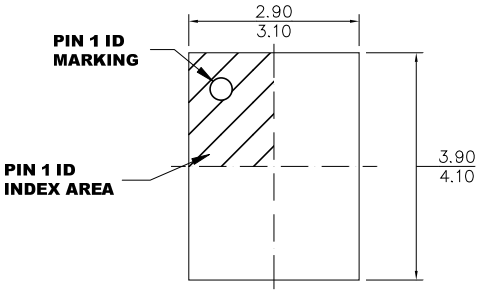


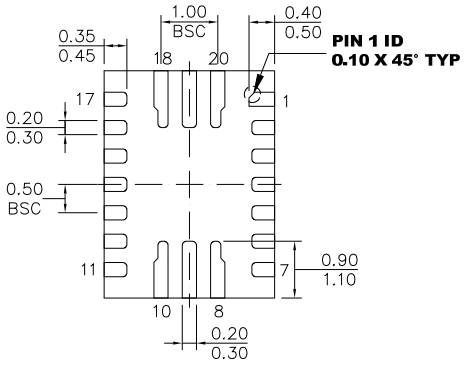
Figure 9. Detailed Application Schematic

PACKAGE INFORMATION

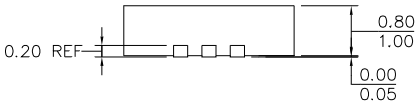
QFN-20 (3mmx4mm)



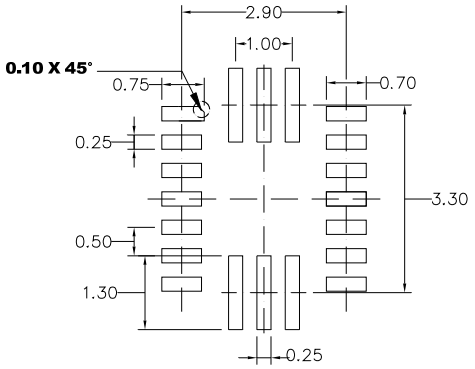
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.11	05/15/2020	The units of 'PGIN high threshold' and 'PGIN low threshold' in EC table on page 5 are changed from V_{FBS} to V_{FBB}.	