MP5514

Wide 2.7V to 18V V_{IN}, 5A, High-Efficiency Bidirectional Power Backup Manager with Hot-Swap, I^2C, ADC, and Capacitor Health Test

DESCRIPTION

The MP5514 is an input power conditioning power management IC (PMIC) designed for enterprise solid-state drives (SSDs), non-volatile dual-inline memory modules (NVDIMMs), and other backup system applications. The device features input current limiting and reverse current blocking. It also integrates an MPS-patented, high-efficiency, bidirectional, buck-boost converter with a single inductor for energy storage and system power backup during an input power failure. The MP5514 also provides an I^2C interface and analog-to-digital converter (ADC). Users can set the input current limit (I_{IN_LIMIT}) and slew rate, and can perform capacitor health tests via the I^2C. The MP5514 monitors system statuses, such as the input voltage (V_{IN}), input current (I_{IN}), storage voltage (V_{STRG}), and temperature. It also provides interrupt options for these features.

Internal input current blocking prevents inrush current during start-up, and reverse current blocking prevents backup energy from flowing to the failing VIN port. MPS's patented energy storage and release management control circuit minimizes the storage capacitor (C_{STRG}) requirement. The circuit increases V_{IN} to provide a higher V_{STRG} to store energy. If an input outage occurs, this energy is released to the system during a hold time (t_{HOLD}).

The MP5514 requires a minimal number of standard external components, and is available in a QFN-30 (5mmx5mm) package.

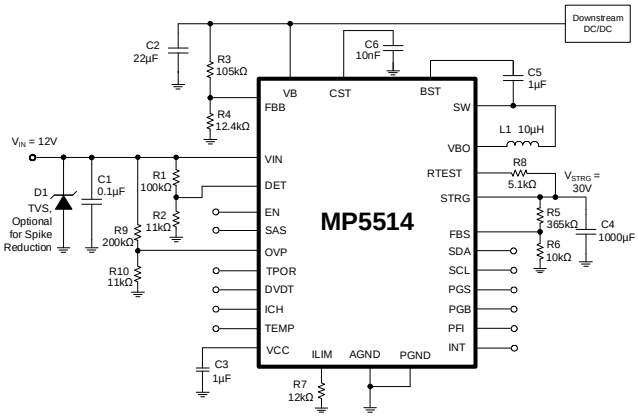
FEATURES

- MPS-Patented Bidirectional Buck-Boost Converter
- Wide 2.7V to 18V Operating Input Voltage (V_{IN}) Range
- Up to 32V Configurable Storage Voltage (V_{STRG})
- Up to 6A Configurable Input Current Limit (I_{IN_LIMIT})
- Up to 5A Buck Load Capability
- Adjustable Bus Voltage (V_{BUS}) Slew Rate
- Input Current Limiting with Integrated 14mΩ MOSFET
- Input Over-Voltage Protection (OVP)
- Reverse-Current Protection (RCP)
- Input Power Failure Indication
- Storage Capacitor (C_{STRG}) Health Test
- Comprehensive Voltage-, Current-, and Temperature-Sensing Analog-to-Digital Converter (ADC)
- Thermal Shutdown
- Available in a QFN-30 (5mmx5mm) Package

APPLICATIONS

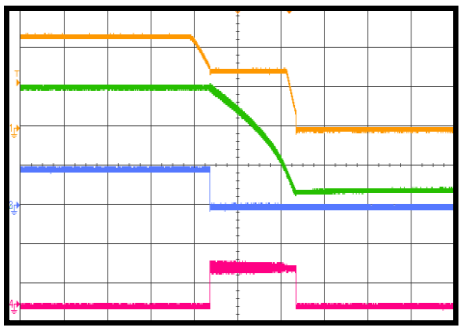
- Solid-State Drives (SSDs)
- Non-Volatile Dual-Inline Memory Modules (NVDIMMs)
- Hard-Disk Drives (HDDs)
- Power Backup Systems

TYPICAL APPLICATION



V_{STRG} Release

V_{IN} = 12V, V_{BUS} = 7.5V, I_{BUS_LOAD} = 5A



5ms/div.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5514GU-xxxx	QFN-30 (5mmx5mm)	*See Below*	1
EVKT-5514	Evaluation Kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP5514GU-Z).

TOP MARKING

MPSYYWW

MP5514

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5514: Part number
LLLLLLL: Lot number

EVALUATION KIT (EVKT-MP5514)

EVKT-5514 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV5514-U-00A	MP5514 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Includes datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

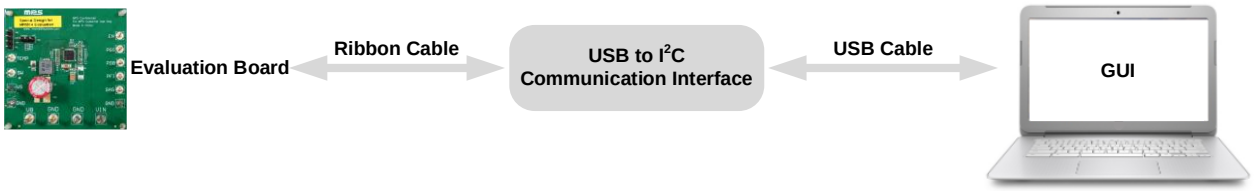
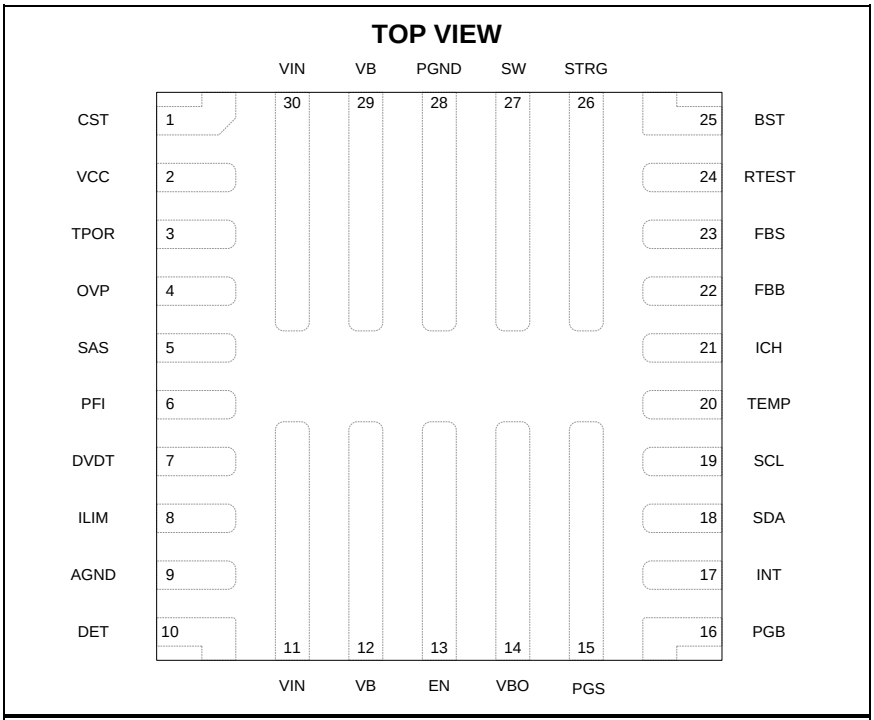


Figure 1: EVKT-5514 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-30 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	CST	**Internal charge pump storage capacitance.** Connect a 10nF to 47nF capacitor between the CST and AGND pins to enable the input current limit (I_{IN_LIMIT}) MOSFET and the disconnect MOSFET.
2	VCC	**Internal LDO output.** The VCC pin provides power to the internal circuitry. Decouple VCC using a ≥1μF ceramic decoupling capacitor, placed as close to VCC as possible. Do not add an external load to VCC.
3	TPOR	**Start-up reset delay.** Connect a ≥1nF capacitor between the TPOR and AGND pins to set the start-up reset delay time (t_{TPOR}). Float TPOR for the default t_{TPOR} (1.5ms).
4	OVP	**Over-voltage protection.** A resistor divider connected between the VIN and OVP pins configures the input over-voltage protection (OVP) threshold (V_{IN_OVP}). If V_{IN_OVP} exceeds 0.81V, then the MP5514 enters buck release mode. If V_{IN_OVP} drops below 0.765V, and the VB pin triggers the bus voltage (V_{BUS}) under-voltage lockout (UVLO) protection, then the part recovers as the first start-up in default with a new t_{TPOR}. Connect the OVP to AGND pins if the OVP function is not used.
5	SAS	**Configured SAS function.** Pull the SAS pin high to turn off the I_{IN_LIMIT} MOSFET and have the part operate in backup mode. If V_{BUS} drops below its UVLO threshold (V_{BUS_UVLO}), then the part exits buck release mode. The internal LDO continues operating. SAS is pulled down internally via a 4MΩ resistor.
6	PFI	**Power failure indication.** The PFI pin is an open-drain output. Pull PFI up to a power source via a resistor to enable the power failure indication function. If the DET voltage (V_{DET}) exceeds 1.02 x the V_{DET} reference voltage (V_{DET_REF}), then PFI is pulled high. If V_{DET} drops below 0.99 x V_{DET_REF}, then PFI is pulled low. Once PFI is pulled low, it remains low for a blanking time (200μs). If SAS, OTP, or EN is off, then PFI is pulled low. If EN is low, then PFI is pulled low, regardless of whether PFI is pulled up to an external DC source. If both VIN and VCC are not available, then PFI is pulled to about 0.85V.
7	DVDT	**Bus voltage start-up slew rate control.** Connect a capacitor ≥1nF between the DVDT and AGND pins to configure the V_{BUS} start-up slew rate. Float DVDT to control the DVDT time (t_{DVDT}) via the I^2C.
8	ILIM	**DC input current limit.** Connect a resistor between the ILIM and AGND pins to adjust the DC current limit (I_{LIMIT}) between the VIN and VB pins. Apply >1.5V to ILIM to trigger over-current protection (OCP) and to disable the isolation MOSFET between VIN and VB.
9	AGND	**IC signal ground.**
10	DET	**Input voltage detection.** The DET pin sets the buck release voltage (V_{BUCK_RLS}) once the input voltage (V_{IN}) drops until V_{DET} below 0.99 x V_{DET_REF}.
11, 30	VIN	**Input supply voltage.** Place a 0.1μF ceramic capacitor as close to the VIN pin as possible. If the VIN power line is long and the system has a high V_{IN} spike, then place a TVS diode at the input. See the Selecting the Input Capacitor and TVS Diode section on page 43 for more details.
12, 29	VB	**Bus voltage.** Place a 22μF to 47μF ceramic capacitor as close to the VB pin as possible.
13	EN	**Enable.** The EN pin enables and disables the internal circuitry. Pull EN low to have the part operate in buck release mode until the storage voltage (V_{STRG}) is discharged. The IC shuts down once V_{BUS} drops and EN is pulled down internally via a 4MΩ resistor. EN has a higher sink current if >2V are applied to it.
14	VBO	**Internal disconnect MOSFET source.** Connect an inductor between the SW and VBO pins for backup boost charge mode and buck release mode.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
15	PGS	**Storage voltage power good indication.** The PGS threshold bits (register 06h, bits[3:0]) are set to 1111 by default. If the FBS voltage (V_{FBS}) exceeds 0.97 x the V_{FBS} reference voltage (V_{FBS_REF}), the then PGS pin is pulled high. If V_{FBS} drops below 0.95 x V_{FBS_REF}, then PGS is pulled low. PGS can be configured via register 06h. PGS is driven by an internal circuit, and does not require an external pull-up resistor. PGS is low, regardless of whether the IC is enabled or disabled. If power from both VIN and VCC are not available, then PGS is pulled down to about 1.3V.
16	PGB	**Bus voltage power good indication.** If the FBB voltage (V_{FBB}) exceeds 0.95 x the V_{FBB} reference voltage (V_{FBB_REF}), then PGB is pulled high. If V_{FBB} drops below 0.9 x V_{FBB_REF}, then PGB is pulled low. PGB is driven by an internal circuit, and does not require an external pull-up resistor. PGB is low, regardless of whether the IC is enabled or disabled. If power from both VIN and VCC are not available, then PGB is pulled down to about 1.3V.
17	INT	**Interrupt output.** The INT is an open-drain output. Even if INT is pulled up to external DC source, INT is pulled low when If EN is low and the IC is not in buck release mode, then INT is pulled low, regardless of whether the part is enabled or disabled. If both VIN and VCC are not available, INT is pulled down to about 0.85V.
18	SDA	**I^2C serial data.**
19	SCL	**I^2C serial clock.**
20	TEMP	**Temperature sense input from thermistor to ADC.**
21	ICH	**Boost charge mode configurable peak switching current.** Float the ICH pin to set the boost charge mode peak switching current to 2A.
22	FBB	**Bus voltage feedback sense.** The FBB pin regulates V_{BUS} in buck release mode.
23	FBS	**Storage voltage feedback sense.** The FBS pin sets the V_{STRG} in boost charge mode.
24	RTEST	**Resistor connection for the capacitor health test.** During a storage capacitor (C_{STRG}) health test, the RTEST pin is pulled to PGND internally. A resistor connected between the STRG and RTEST pins discharges C_{STRG}. The RTEST discharge current (I_{RTEST}) should be below 500mA.
25	BST	**Bootstrap.** Connect a bootstrap capacitor (C_{BST}) between the BST and SW pins to supply the high-side MOSFET (HS-FET) driver.
26	STRG	**Backup energy storage.** Connect C_{STRG} to the STRG pin for the energy storage and release functions.
27	SW	**Switch output.** The SW pin is used for the energy storage and release circuitry. Connect an inductor between the SW and VBO pins.
28	PGND	**Power ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) 21V
V_B, V_{BO} ..... -0.3V to +21V
V_{STRG}, V_{RTEST} ..... -0.3V to +36V
V_{SW} ..... -0.3V (-6V for <10ns) to V_{STRG} + 0.3V
V_{BST} ..... -0.3V to V_{STRG} + 6V
V_{CST} ..... -0.3V to +28V
All other pins ..... -0.3V to +6V
EN current (I_{EN}) 1mA (2)
I_{PFI}, I_{PGB}, I_{PGS}, I_{INT} 5mA (3)
I_{RTEST} 500mA (3)
Continuous power dissipation (T_A = 25°C) (4) 3.57W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM) 750V

Recommended Operating Conditions (5)

Input voltage (V_{IN}) ..... 2.7V (6) to 18V
Bus voltage (V_{BUS}) ..... 2.6V to 16V
Storage voltage (V_{STRG}) ..... V_{IN_MAX} + 3V to 32V
Max input current (I_{IN_MAX}) 6A
Max buck release mode current (I_{BUCK_RLS}) 5A
EN current (I_{EN}) 0.5mA (2)
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-30 (5mmx5mm)			
EV5514-U-00A (7)	35	6.5	°C/W
JESD51-7 (8)	36	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For more details, see the Enable (EN) Control section on page 24.
3) If these pins are pulled up to a power source, then the current should be below the maximum value.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Guaranteed for temperatures conditions ≥25°C. If the temperature drops below 25°C, then it is recommended to connect a Schottky diode between the VIN and VCC pins for start-up from a 2.7V input.
7) Measured on EV5514-U-00A (63mmx63mm), 2-layer PCB.
8) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Shutdown current	I_{SD}	V_{EN} = 0V, then VIN starts up, T_J = 25°C		2.5	5	μA
Quiescent current	I_Q	V_{SAS} = 2V, V_{EN} = 2V, V_{FBB} = V_{FBS} = V_{DET} = 1.1V		1.5		mA
		V_{SAS} = 0V, V_{EN} = 2V, V_{FBB} = V_{FBS} = V_{DET} = 1.1V		2.5	3	mA
VCC regulator voltage	V_{CC}	V_{IN} or V_{BUS} = 6V, I_{VCC} = 1mA	4.75	5	5.25	V
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold (10)	$V_{IN\_UVLO\_RISING}$	EFUSE_UVLO = 00		2.5		V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	EFUSE_UVLO = 00		2.3		V
VIN to VB current-limit MOSFET on resistance	$R_{DS(ON)\_CLM}$			14		mΩ
VIN to VB continuous current limit (I_{LIMIT}) warning	I_{LIMIT_WRN}	R_{ILIM} = 36.5kΩ, T_J = 25°C	1.9	2	2.1	A
		R_{ILIM} = 36.5kΩ, T_J = -40°C to 125°C (9)	1.84	2	2.16	A
Shutdown leakage current	I_{SD_LKG}	V_{IN} = 12V and V_{BUS} = 0V, or V_{BUS} = 12V and V_{IN} = 0V; T_J = 25°C		2	3	μA
VB clamping voltage	V_{CLAMP}	V_{IN} = 18V	15.2	16	16.8	V
Bus voltage (V_{BUS}) rise time (DVDT) (11)	t_{DVDT}	DVDT is floating, V_{IN} = 12V, DVDT bits = 00, t_{DVDT} test		1.6		ms
DVDT current	I_{DVDT}	Connect a capacitor to DVDT, I_{DVDT} test		3		μA
Internal reset delay time	t_{DELAY}	TPOR is floating, t_{DELAY} test		1.5		ms
TPOR current	I_{TPOR}	Connect a capacitor to TPOR, I_{TPOR} test		1		μA
Energy Storage and Release						
Storage pre-charge current	$I_{PRE-CHARGE}$		250	350	450	mA
Boost disconnect MOSFET on resistance	$R_{DS(ON)\_DIS}$			30		mΩ
Boost charge mode peak switching current	I_{CH}	ICH is floating, L = 10μH		2		A
		R_{ICH} = 200kΩ, L = 10μH		0.65		A
Energy management high-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			80		mΩ
Energy management low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			40		mΩ
FBB feedback voltage	V_{FBB_REF}	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to 125°C	0.786	0.8	0.812	V
FBS feedback voltage	V_{FBS_REF}	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to 125°C	0.786	0.8	0.812	V
DET feedback voltage	V_{DET_REF}	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to 125°C	0.786	0.8	0.812	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C [9], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FBB feedback current	I_{FBB}	V_{FBB} = V_{FBS} = V_{DET} = 0.85V		10	50	nA
FBS feedback current	I_{FBS}	V_{FBB} = V_{FBS} = V_{DET} = 0.85V		10	50	nA
DET feedback current	I_{DET}	V_{FBB} = V_{FBS} = V_{DET} = 0.85V		10	50	nA
V_{IN} over-voltage protection (OVP) threshold	V_{IN_OVP}	OVP pin voltage (V_{OVP}) rising		0.81		V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$	V_{IN_OVP} hysteresis		45		mV
V_{STRG} OVP threshold	V_{STRG_OVP}			1.1		% of V_{FBS_REF}
VIN to VB isolation MOSFET start-up voltage		V_{BUS} = 5V, then V_{IN} starts up		0.2		V
VIN to VB isolation MOSFET shutdown current	$I_{IN\_VB\_SD}$	PFI is low		-250	0	mA
PFI high voltage threshold	V_{PFI_HIGH}			1.02		% of $V_{DET-REF}$
PFI low voltage threshold	V_{PFI_LOW}			0.99		
PFI falling delay	$t_{PFI\_FALLING}$			0.5		µs
PFI rising delay	t_{PFI_RISING}			200		µs
PFI sink current capability	V_{PFI_SINK}	4mA sink			0.3	V
PGB high voltage threshold	V_{PGB_HIGH}			0.95		% of V_{FBB_REF}
PGB low voltage threshold	V_{PGB_LOW}			0.9		
PGB delay	t_{PGB}	Rising and falling edge		5		µs
PGB sink current capability	V_{PGB_SINK}	4mA sink			0.3	V
PGS high voltage threshold	V_{PGS_HIGH}	PGS threshold bits = 1111		0.97		% of V_{FBS_REF}
PGS low voltage threshold	V_{PGS_LOW}	PGS threshold bits = 1111		0.95		
PGS delay	t_{PGS}	Rising and falling edge		25		µs
PGS sink current capability	V_{PGS_SINK}	4mA sink			0.3	V
Buck mode valley I_{LIMIT}	I_{LIMIT_VALLEY}		5	6.5		A
Buck release mode switching frequency	f_{SW_RLS}	V_{STRG} = 32V to 10V, BUCK_FSW = 100	380	480	580	kHz
V_{BUS} UVLO rising threshold [10]	$V_{BUS\_UVLO\_RISING}$		2.2	2.35	2.5	V
V_{BUS} UVLO hysteresis [10]	$V_{BUS\_UVLO\_HYS}$			0.1		V
Analog-to-Digital Converter (ADC)						
ADC voltage range			0		1.28	V
ADC resolution [12]				10		bits
ADC conversion time [12]		ADC conversion for one data bit		45		µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Interface (SDA, SCL, INT, SAS, EN)						
High-level input voltage	V_{IN_HIGH}	SDA, SCL, SAS, EN	1.2			V
Low-level input voltage	V_{IN_LOW}	SDA, SCL, SAS, EN			0.4	V
Low-level output voltage	V_{OUT_LOW}	4mA sink, SDA, INT			0.3	V
Input leakage current	I_{IN_LKG}	Connected to 6V, SCL		10		nA
High level output leakage		Open drain, connected to 6V, SDA		10		nA
Protection						
Thermal shutdown (12)	T_{SD}	Forced backup		150		°C
Thermal shutdown hysteresis (12)	T_{HYS}	Forced backup		25		°C
Thermal warning (12)	T_{WRN}			120		°C

Notes:

9) Derived from over-temperature (OT) correlation. Not tested in production.
10) V_{IN} UVLO determines the IC's start-up voltage threshold. V_{BUS} UVLO controls the energy storage and release circuitry. The internal regulator (VCC) is powered by both V_{IN} and V_{BUS}. If either V_{IN} or V_{BUS} exceeds its respective UVLO threshold, the IC does not shut down.
11) See the Start-Up Reset Delay and Bus Voltage Start-Up Slew Rate Control section on page 21 for more details.
12) Guaranteed by characterization. Not tested in production.

I²C PORT SIGNAL CHARACTERISTICS

Parameter	Symbol	Condition	Min (13)	Max (13)	Min (14)	Max (14)	Units
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	t_{SU_START}		160		600		ns
Hold time for a repeated start condition	t_{HD_START}		160		600		ns
SCL clock low period	t_{LOW}		160		1300		ns
SCL clock high period	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DATA}		10		100		ns
Data hold time	t_{HD_DATA}		0	70	0		ns
SCLH signal rise time	t_{RISE_SCLH}		10	40	20 x $0.1C_{BUS\_LOAD}$	300	ns
SCLH signal rise time after a repeated start condition and an acknowledge (ACK) bit	$t_{RISE\_SCLH\_RE}$		10	80	20 x $0.1C_{BUS\_LOAD}$	300	ns
SCLH signal fall time	t_{FALL_SCLH}		10	40	20 x $0.1C_{BUS\_LOAD}$	300	ns
SDAH signal rise time	t_{RISE_SDAH}		10	80	20 x $0.1C_{BUS\_LOAD}$	300	ns
SDAH signal fall time	t_{FALL_SDAH}		10	80	20 x $0.1C_{BUS\_LOAD}$	300	ns
Set-up time for a stop condition	$t_{SU;STOP}$		160		600		ns
Bus free time between a stop and start condition	t_{BUS_FREE}		160		1300		ns
Data valid time	t_{VD_DATA}			16		90	ns
Data valid acknowledge time	$t_{VD;ACK}$			160		900	ns
Voltage spike pulse width	t_{SPIKE}	Should be suppressed by the input filter	0	10	0	50	ns
Capacitive load for each bus line	C_{BUS_LOAD}	SDAH line, SCLH line		100		400	pF
		SDAH line + SDA line, SCLH line + SCL line		400		400	pF

Notes:

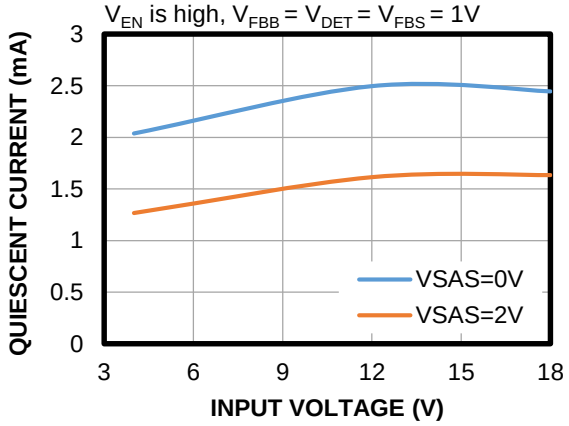
13) C_{BUS_LOAD} = 100pF
14) C_{BUS_LOAD} = 400pF

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{BUS_RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

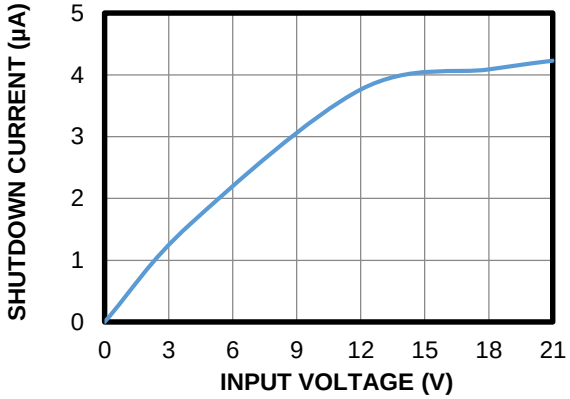
Quiescent Current vs. Input Voltage

V_{EN} is high, V_{FBB} = V_{DET} = V_{FBS} = 1V

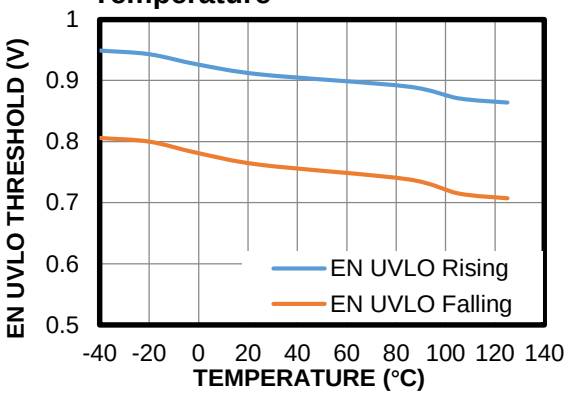


Shutdown Current vs. Input Voltage

V_{EN} = 0V

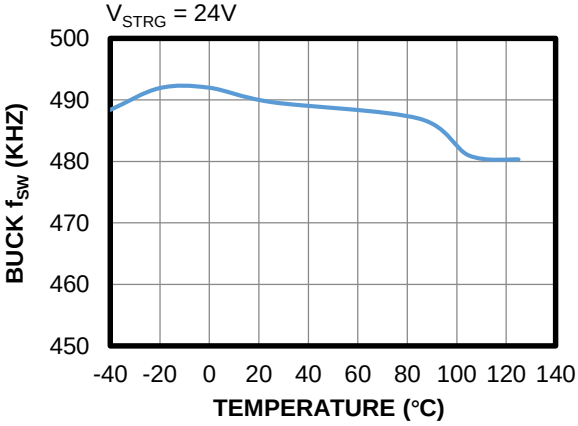


EN UVLO Threshold vs. Temperature

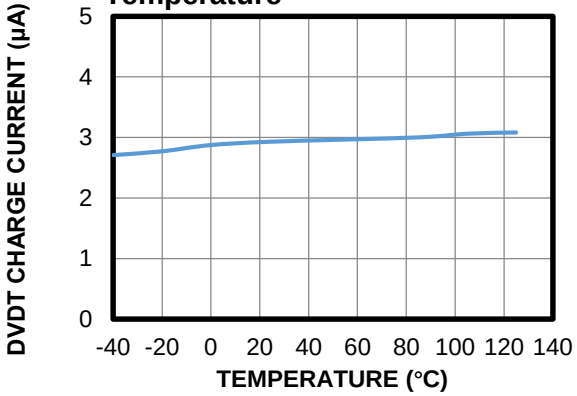


Buck Switching Frequency vs. Temperature

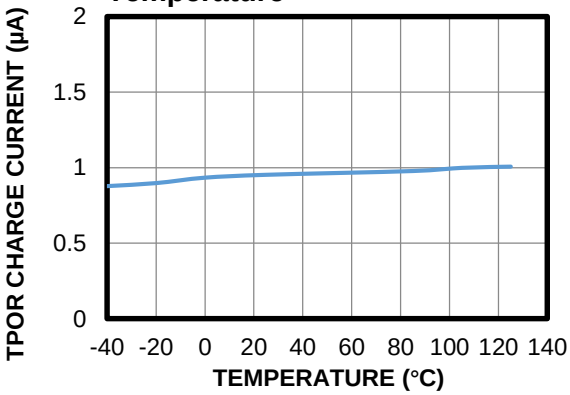
V_{STRG} = 24V



DVDT Charge Current vs. Temperature



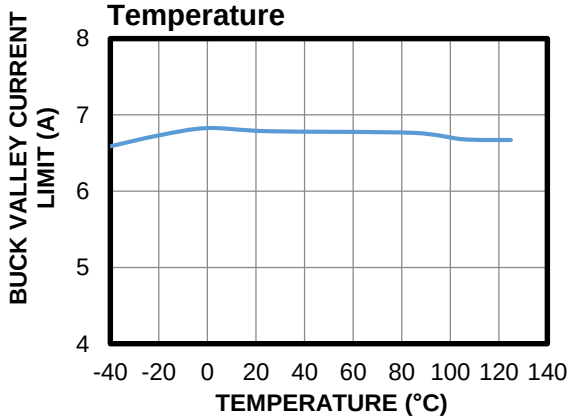
TPOR Charge Current vs. Temperature



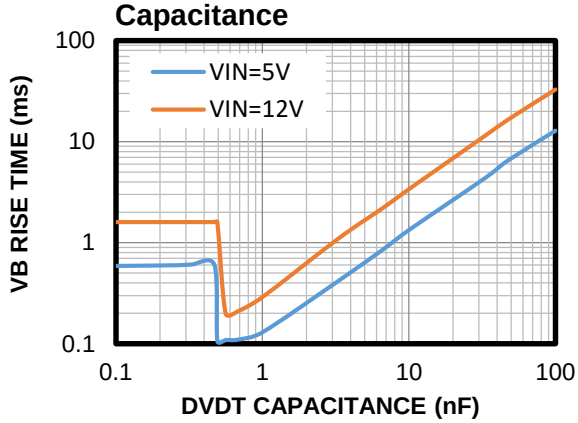
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS_RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

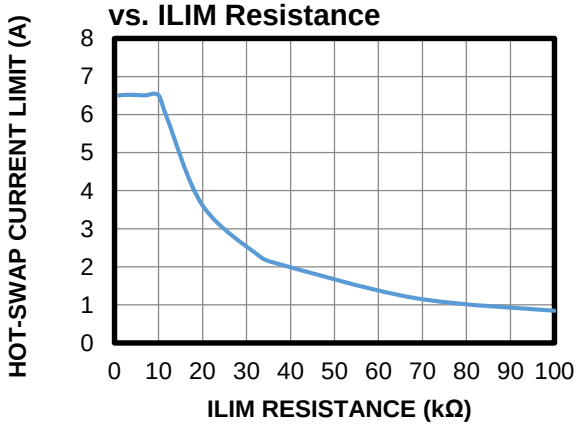
Buck Valley Current Limit vs. Temperature



VB Rise Time vs. DVDT Capacitance

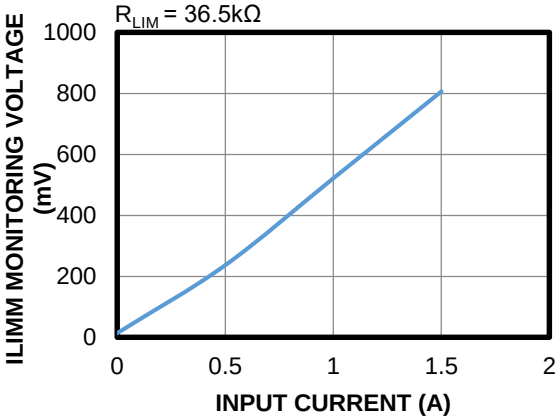


Hot-Swap MOSFET Current Limit vs. ILIM Resistance

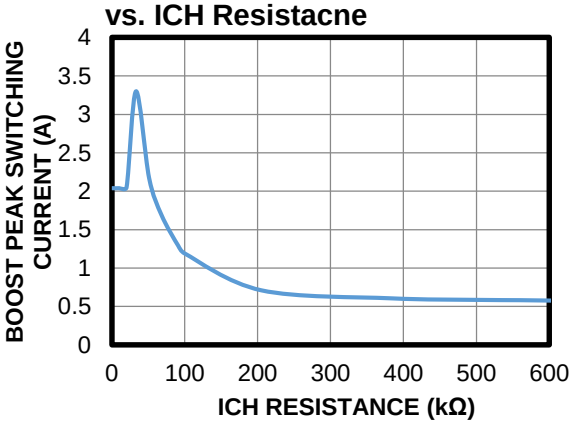


ILIM Monitoring Voltage vs. Input Current

R_{LIM} = 36.5kΩ

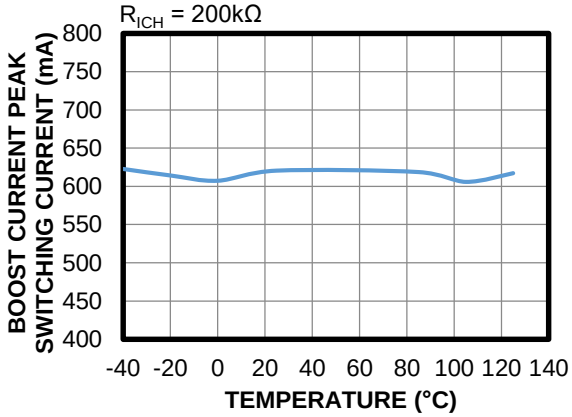


Boost Peak Switching Current vs. ICH Resistacne



Boost Peak Switching Current vs. Temperature

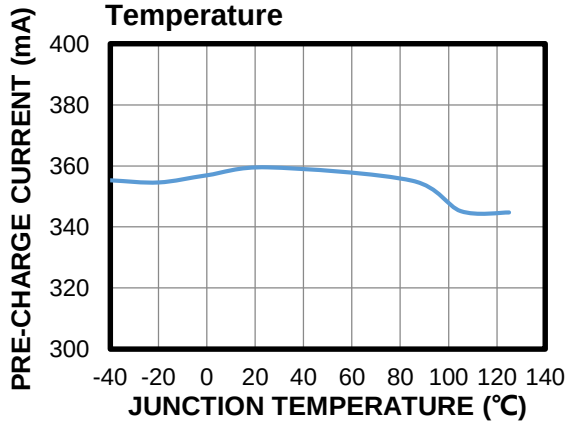
R_{ICH} = 200kΩ



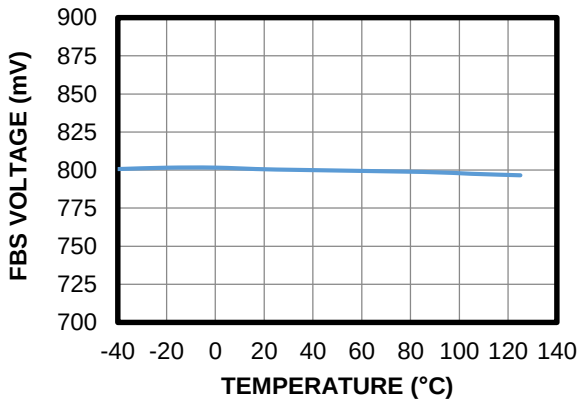
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS_RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

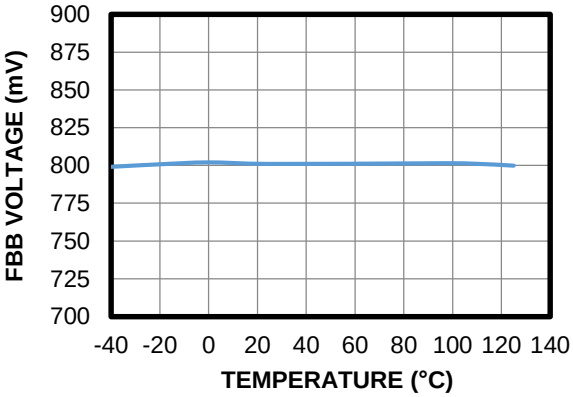
Boost Pre-Chrage Current vs. Temperature



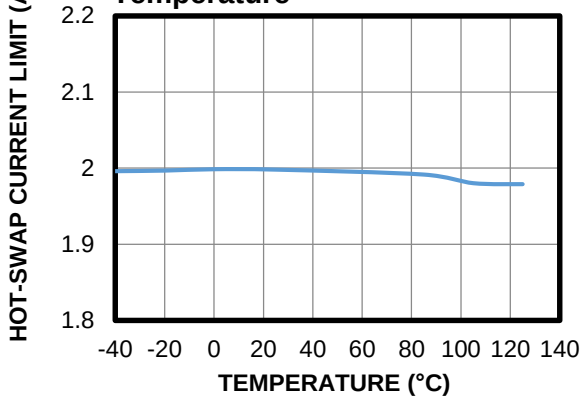
FBS Voltage vs. Temperature



FBB Voltage vs. Temperature



Hot-Swap Current Limit vs. Temperature

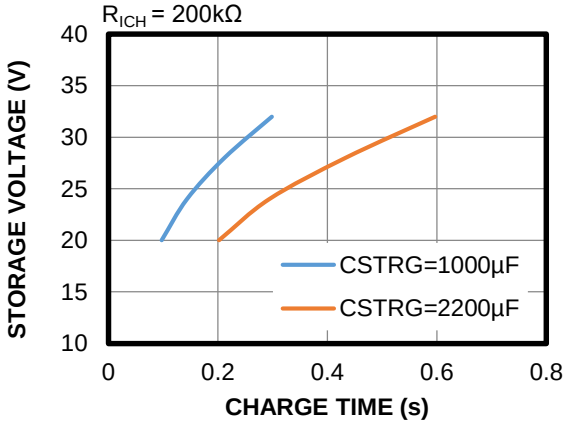


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, V_{BUS_RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

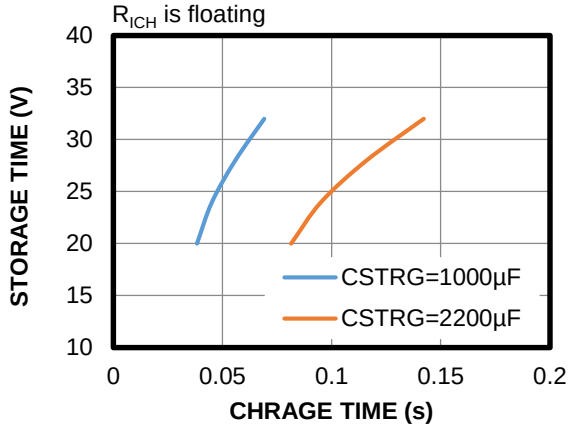
Storage Voltage vs. Charge Time

R_{ICH} = 200kΩ

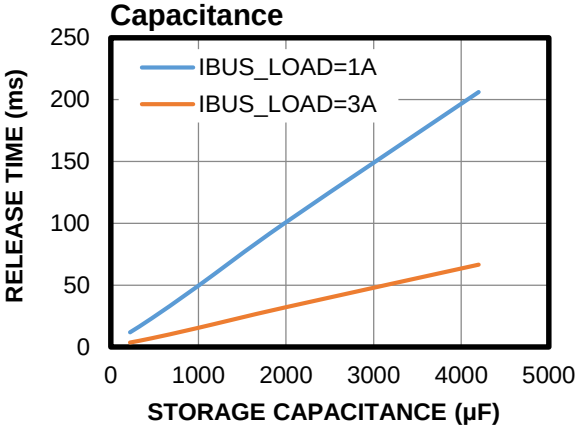


Storage Voltage vs. Charge Time

R_{ICH} is floating

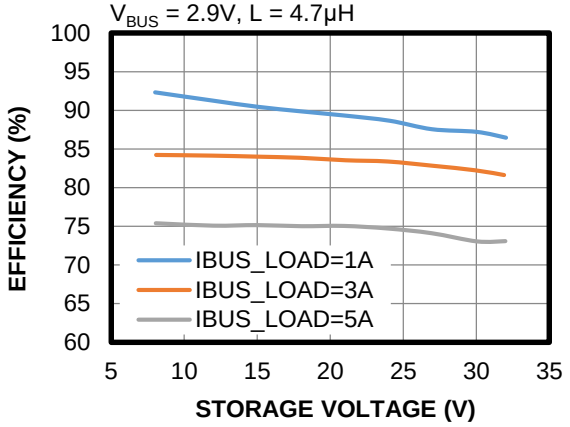


Release Time vs. Storage Capacitance



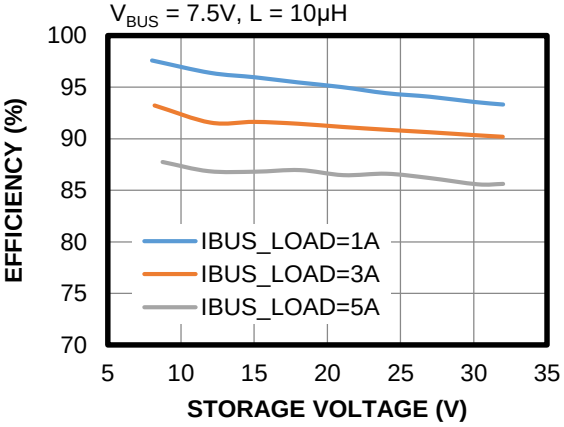
Buck Efficiency

V_{BUS} = 2.9V, L = 4.7µH



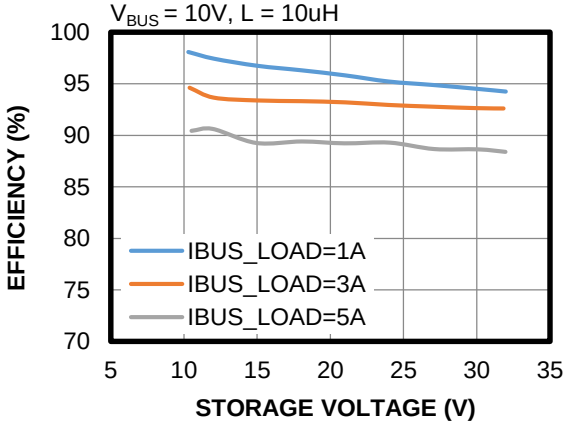
Buck Efficiency

V_{BUS} = 7.5V, L = 10µH



Buck Efficiency

V_{BUS} = 10V, L = 10uH

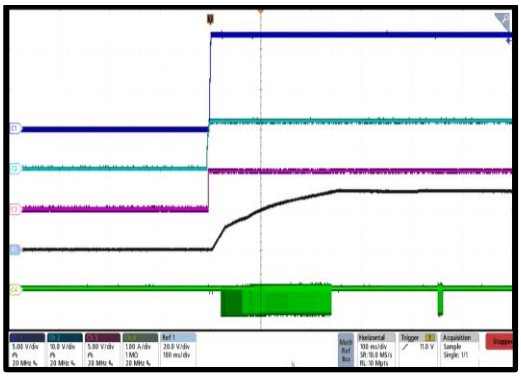


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, V_{BUS_RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

Start-Up through VIN

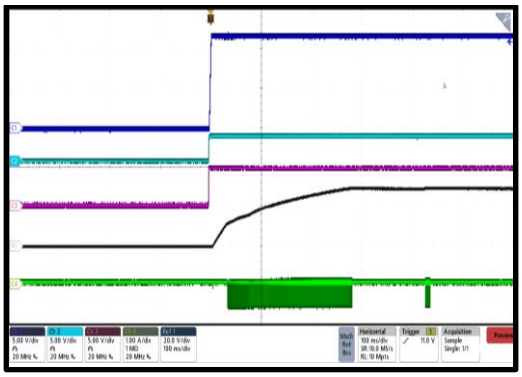
I_{BUS_LOAD} = 5A



100ms/div.

Start-Up through EN

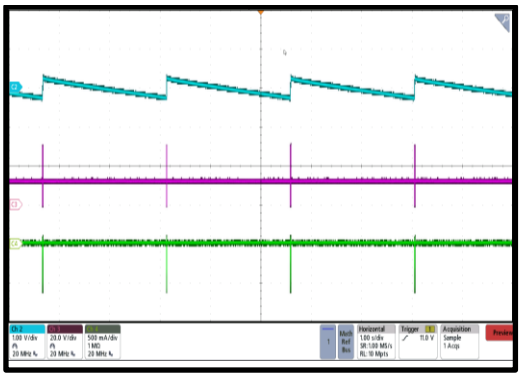
I_{BUS_LOAD} = 5A



100ms/div.

Boost Steady State

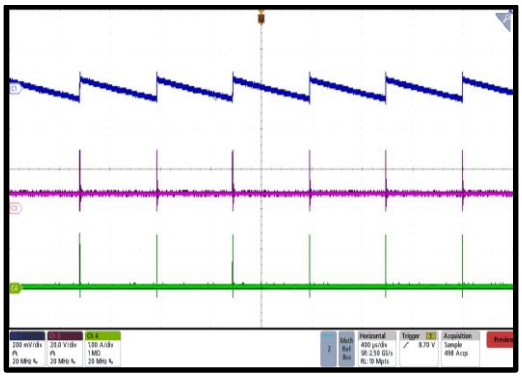
R_{ICH} = 200kΩ



1s/div.

Buck Steady State

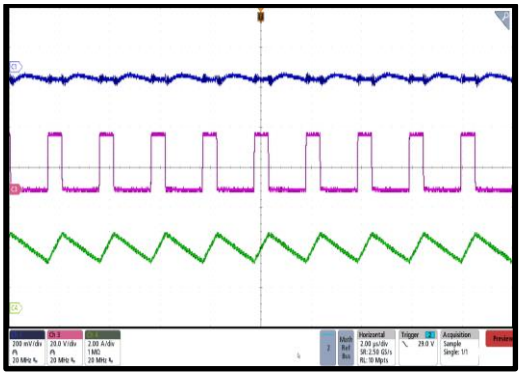
I_{BUS_LOAD} = 0A, 22µF ceramic capacitor on VB



400us/div.

Buck Steady State

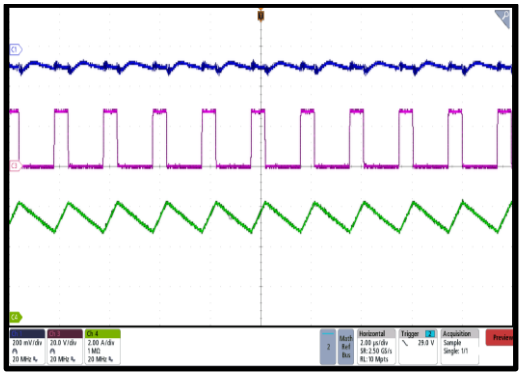
I_{BUS_LOAD} = 3A, 22µF ceramic capacitor on VB



2µs/div.

Buck Steady State

I_{BUS_LOAD} = 5A, 22µF ceramic capacitor on VB



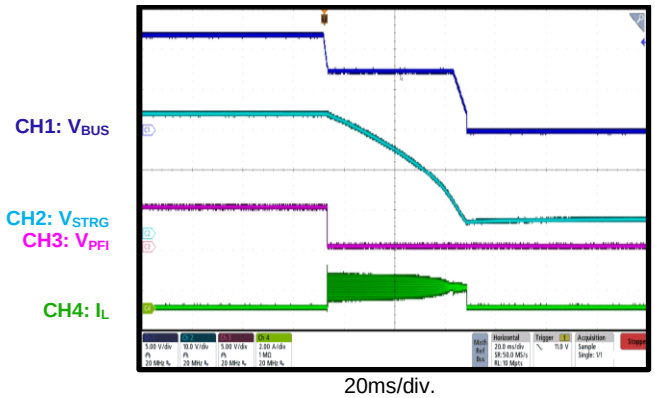
2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, VB_{RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

V_{STRG} Release

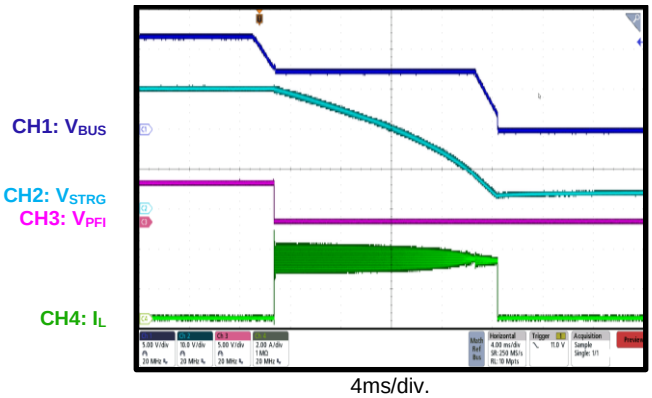
I_{BUS_LOAD} = 1A



20ms/div.

V_{STRG} Release

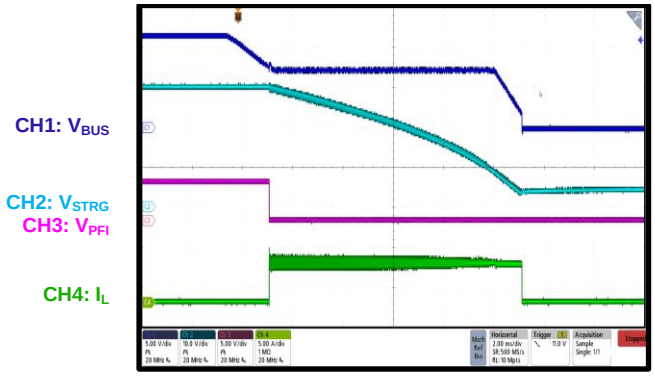
I_{BUS_LOAD} = 3A



4ms/div.

V_{STRG} Release

I_{BUS_LOAD} = 5A



2ms/div.

FUNCTIONAL BLOCK DIAGRAM

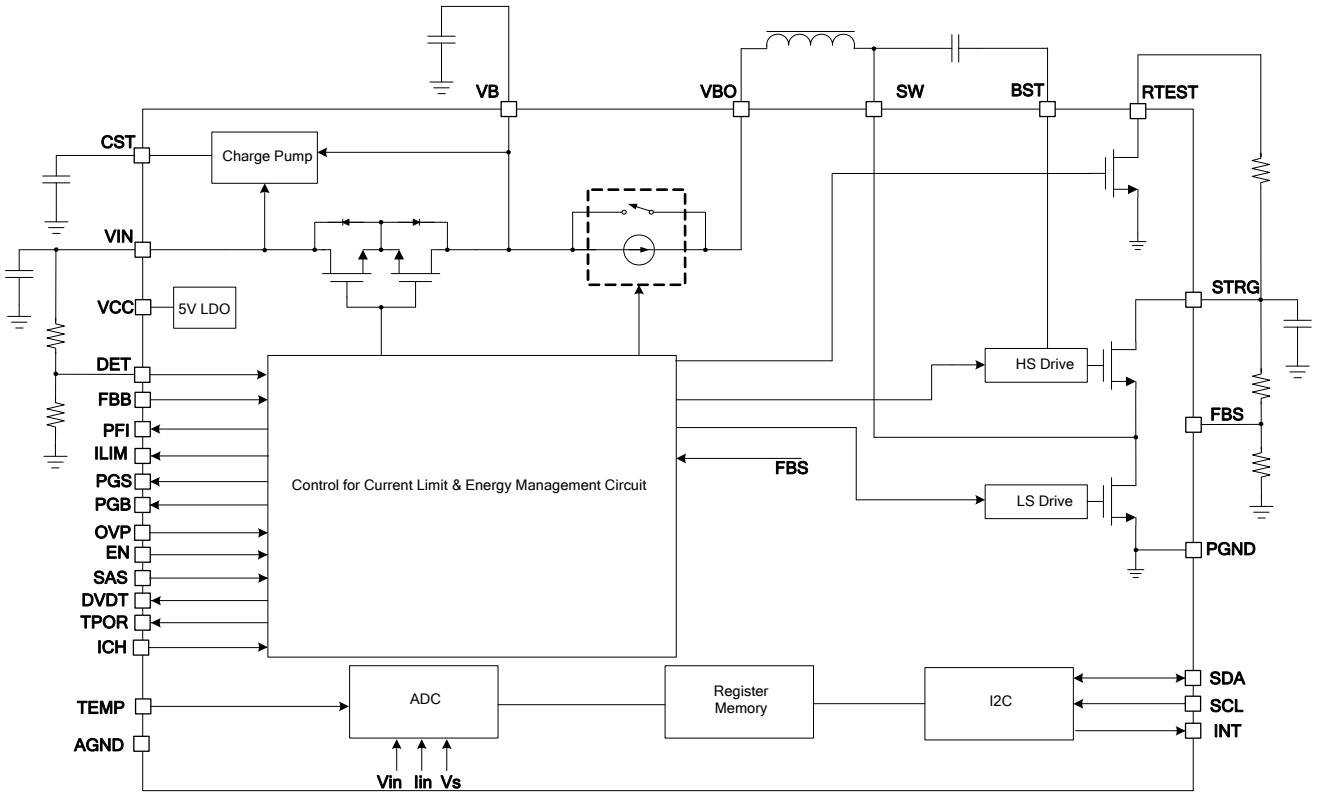


Figure 2: Functional Block Diagram

OPERATION

The MP5514 is an energy storage and management unit in a QFN-30 (5mmx5mm) package. The MP5514 provides a very compact and efficient energy management solution for typical solid-state drives (SSDs) or hard disk drives (HDDs). MPS's patented lossless energy storage and release management circuits use a bidirectional buck-boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter increases the energy storage voltage (V_{STRG}) level. The storage feedback resistor divider sets V_{STRG}. If the input shuts down suddenly, then the internal buck converter transfers the energy from the storage capacitor (C_{STRG}) to the bus, and holds the bus voltage (V_{BUS}) while the system consumes the energy from C_{STRG}.

The MP5514 also features an I^2C interface. The I^2C interface can be used to write the control command and the monitor system status. An integrated analog-to-digital converter (ADC) converts the voltage, current, and temperature sensor signals.

Start-Up

If the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold, then VCC and the I^2C interface are enabled. If VCC is ready and V_{IN} exceeds V_{BUS} by ≥0.2V once the power-on reset delay time is complete, then the isolation MOSFET between VIN and VB turns on, and the bus capacitor (C_{BUS}) is charged to V_{IN} according to the DVDT slew rate.

Once the DVDT voltage (V_{DVDT}) is saturated, the storage boost converter is unlocked and can be enabled by the register bits. There is a delay time (about 1.2ms) before the boost converter starts up to ensure that the isolation MOSFET is fully on.

The storage boost converter is enabled by default. The V_{STRG} is charged by a trickle current (about 350mA) during the pre-charge period. Once V_{STRG} reaches V_{BUS}, the boost switching circuit is initiated, and V_{STRG} regulated at the target voltage (see Figure 3).

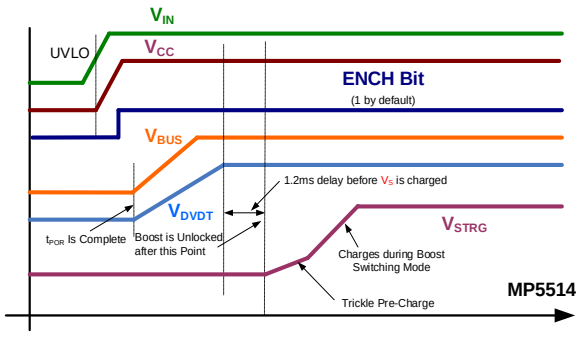


Figure 3: System Power-Up Sequence

Storage Voltage

After the start-up period, the internal boost converter regulates V_{STRG} to the set value automatically. The MP5514 uses burst mode to minimize the converter's power loss. If the FBS voltage (V_{FBS}) drops below the FBS feedback voltage (V_{FBS_REF}), then the parts enters burst mode and charges C_{STRG}. Once V_{STRG} is charged, and V_{FBS} reaches $V_{FBS-REF}$ + FBS_HYS, the converter stops switching. FBS_HYS is adjustable via the I^2C.

During boost charge mode, the boost switching current limit (I_{LIMIT}) and the low-side MOSFET (LS-FET) control the boost converter. If the LS-FET turns on, then the inductor current (I_L) increases until it reaches its peak current level (set by ICH). Once I_L reaches the peak current level, the LS-FET turns off for the set minimum off time. If the feedback voltage is below the internal reference (0.8V) at the end of the minimum off time, then the LS-FET turns on; otherwise, the MP5514 waits until the voltage drops below the reference before the LS-FET turns on again. In boost charge mode, the high-side MOSFET (HS-FET) does not turn on, and I_L is conducted via the HS-FET body diode.

The boost I_{LIMIT} can be configured via the ICH resistor (R_{ICH}). The configured boost switching I_{LIMIT} (I_{CH}) can be estimated with Equation (1):

$$I_{CH}(A) = \frac{88}{R_{ICH}(k\Omega)} + \frac{V_{IN}}{L(H) \times 10^7} + 0.1 \quad (1)$$

Where L is the boost inductor.

The boost switching I_{LIMIT} can be configured via R_{ICH}. It is recommended to set the boost switching I_{LIMIT} between 0.5A and 2A for normal applications. Float ICH to set the boost switching peak current at 2A by default (ICH bits = 11) for typical 12V input and 10µH inductor application conditions. See the ICH register description on page 35 for other boost peak settings while floating ICH.

The MP5514 has V_{STRG} over-voltage protection (OVP). If the feedback V_{STRG} on FBS exceeds 1.1 x V_{FBS_REF}, then the boost converter's LS-FET turns off until V_{STRG} drops to the regulation voltage. Additional external power to STRG provided by a voltage exceeding the regulation voltage is not required.

Shutdown Release

Once the first start-up period is complete, and the boost converter starts switching, the MP5514 registers and enables the release function. Once the input power drops and the DET voltage (V_{DET}) drops to 0.99 x the V_{DET} reference voltage (V_{DET_REF}), then the storage boost converter stops charging and enters buck release mode. At the same time, the isolation MOSFET shuts down to prevent a negative current from flowing between VB and VIN.

In buck release mode, the MP5514 transfers energy from the high-voltage C_{STRG} to the low-voltage C_{BUS}. The regulated V_{BUS} is determined by the V_{FBB} reference voltage (V_{FBB_REF}) and the resistor divider between VB and FBB.

Figure 4 shows the detailed system shutdown process.

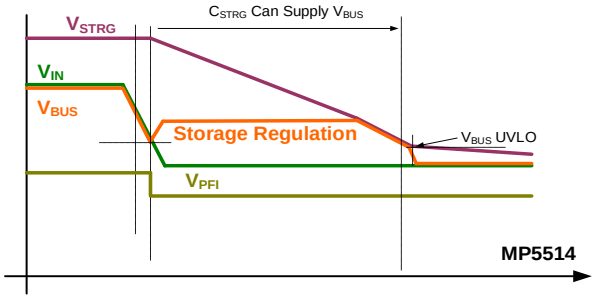


Figure 4: Shutdown through VIN

Buck release mode has a max I_{LIMIT} function that limits the release current. In each buck release mode switching cycle, the HS-FET remains off until I_L drops to the valley I_{LIMIT} (typically 6.5A).

Input Recovery Start-Up

If V_{IN} fails and is restored, then the MP5514 remains in buck release mode. If V_{STRG} is discharged, and V_{BUS} drops below the V_{BUS} UVLO threshold (V_{BUS_UVLO}), then the MP5514 restarts from the recovered V_{IN}. This starts a new V_{IN} start-up cycle with a start-up reset delay time (t_{TPOR}).

Input Current Limit

The input I_{LIMIT} (I_{IN_LIMIT}) controls the input inrush current of the isolation MOSFET to prevent inrush current from flowing between VIN and VB. The internal DVDT bits or external DVDT capacitor (C_{DVDT}) can set the soft-start time (t_{SS}). In addition to soft start (SS), ILIM can limit the steady-state current by connecting a resistor (R_{ILIM}) between the ILIM and AGND pins to set I_{IN_LIMIT}. I_{IN_LIMIT} can be estimated with Equation (2):

$$I_{IN\_LIMIT} = \frac{70.04}{R_{ILIM}(k\Omega)} + 0.08 \quad (2)$$

ILIM also monitors and indicates the isolation MOSFET current. The relationship between the input current (I_{IN}) and the ILIM voltage (V_{ILIM}) can be estimated with Equation (3):

$$I_{IN} = \frac{V_{ILIM} \times 64.26}{R_{ILIM}(k\Omega)} + 0.08 \quad (3)$$

V_{ILIM} can be read via the ADC. V_{ILIM} is below 1.09V for normal applications. If a >1.5V voltage is applied to ILIM externally, then the isolation MOSFET shuts down.

If the VB load is close to the ILIM threshold during each boost refresh cycle, then I_{IN} may trigger I_{IN_LIMIT}, as well as the system interrupt. To avoid continuously triggering the ILIM interrupt, the input over-current (OC) interrupt is masked automatically during each boost refresh cycle. The mask time depends on the boost switching time.

The OC_RLS_EN bit determines the behavior of the backup buck converter once input over-current protection (OCP) is triggered. If OC_RLS_EN is set to 1, then the backup buck converters starts up to maintain V_{BUS} once input OCP is triggered and the FBB voltage (V_{FBB}) drops to V_{FBB_REF}. Once V_{FBB} is charged to

105% of V_{FBB_REF}, the buck converter turns off. The buck converter is off during the boost refresh cycle, even if OCP is triggered. If OC_RLS_EN is set to 0, then the backup buck converter cannot be turned on by FBB.

The isolation MOSFET also has fast OCP for extreme OC conditions. This is the second level of OCP. The fast OCP threshold is about 11A, with a ±10% tolerance. Once fast OCP is triggered, the isolation MOSFET turns off without entering buck release mode. The MOSFET turns on again once the OC fault is removed and VIN is present.

Start-Up Reset Delay and Bus Voltage Start-Up Slew Rate Control

TPOR controls the power-on reset function for hot swapping. Float TPOR to set the start-up reset delay time (t_{TPOR}) to its default time (about 1.5ms). If an external capacitor is connected to TPOR, then an internal 1μA current charges the capacitor between 0V and 1V, and determines t_{TPOR}. t_{TPOR} can be estimated with Equation (4):

$$t_{TPOR} = \frac{C_{TPOR} \times 1V}{1\mu A} \quad (4)$$

After t_{TPOR}, a capacitor across DVDT sets the VB t_{SS}. During t_{SS}, the relationship between VB and DVDT can be estimated with Equation (5):

$$VB = 13 \times V_{DVDT} \quad (5)$$

Where V_{DVDT} is the DVDT capacitor voltage charged by a 3μA current.

The V_{DVDT} charge is saturated to about 1.23V.

t_{SS} between 0V and V_{IN} can be estimated with Equation (6):

$$t_{SS} = \frac{VB \times C_{DVDT}}{13 \times 3\mu A} \quad (6)$$

Float DVDT to configure the VB rise time via the internal DVDT register bits. By default, the DVDT bit is set to 00, and the VB slew rate is about 7.5V/ms. If DVDT is floating, the VB rise time from 0V to 12V is 1.6ms by default.

Reverse-Current Protection (RCP)

The VIN to VB MOSFET turns on once V_{IN} exceeds its UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) and (V_{BUS} + 0.2V). This MOSFET turns off once V_{DET} drops, and the MP5514 enters buck release mode. The MOSFET does not turn on again until the part exits buck release mode.

If energy from the storage capacitors is released to VB, then the isolation MOSFET circuit employs reverse-current protection (RCP). A 250mA reverse current from VB to VIN typically shuts down the isolation MOSFET.

Start-Up Sequence

After start-up, the MP5514 operates with the t_{TPOR} and DVDT t_{SS}. During the VB rise time, an internal charge pump charges the CST capacitor (C_{CST}). This provides a driver source for the hot-swap MOSFET. A shorter DVDT time may trigger the input current-limit threshold. A larger C_{CST} may affect the charge-pump slew rate. It is recommended that C_{CST} be 10nF. During the DVDT t_{SS}, the VB capacitor (C_{VB}) is charged, and C_{STRG} is not charged.

Once C_{VB} is charged, V_{DVDT} charges to about 1.23V and is held at the saturated voltage. If PFI is high and DVDT is saturated, then the charge function is enabled and C_{STRG} charges to the target voltage.

Storage Capacitor Test

The MP5514 provides a capacitor test function that discharges C_{STRG} via an external resistor connected between STRG and RTEST. Figure 5 shows the C_{STRG} test circuit.

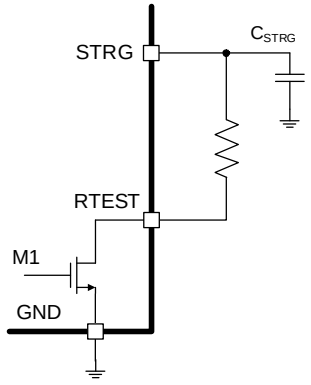


Figure 5: Storage Capacitor Test Circuit

The MOSFET is about 4.5Ω, and the peak discharge current should be limited to below 500mA via an external resistor (even if it is discharged in a short time).

If the START_CAP_TEST bit is set, then the MP5514 disables boost charge switching, and

RTEST is connected to GND via the internal MOSFET (M1) for energy discharging. The MP5514 enables V_{STRG} ADC conversion once V_{FBS} drops below the V_{FBS_REF} threshold. The system-on-chip (SoC) can read V_{STRG} via the I^2C. Simultaneously, an internal counter is enabled to measure the discharge time. The counter continues until the capacitor voltage drops below the PGS threshold. Once V_{STRG} drops to the PGS threshold, the ADC reads V_{STRG} again, and the CAP_TEST_DONE bit is set to indicate that the capacitor test is complete. CAP_TEST_DONE produces one interrupt signal to inform the SoC that the test has been completed. The SoC can read V_{STRG} and the counter timer register. With the initial voltage and end voltage reading, the SoC determines whether the discharge time is acceptable.

At the first ADC conversion, the MP5514 reads V_{STRG} and stores it in the ADC_BACKUP_VOLTAGE_DATA2 register. Once the capacitor is discharged, the ADC records the end voltage to the ADC_BACKUP_VOLTAGE_DATA1 register. The counter result is stored in the CAP_TEST_TIMER register.

Once the capacitor test is complete, the START_CAP_TEST bit is reset, and the recharge function is enabled. Figure 6 on page 23 shows the capacitor test flowchart.

The SoC capacitor test function operates as follows:

1. Write “1” to register 04h, bit[2] and bit[6] to mask the PGS not good interrupt and ADC complete input.
2. Write a value to register 06h, bits[3:0] to set the PGS threshold. Write “00” to register 06h, bits[3:0] to set the PGS threshold at 80% of V_{STRG}.
3. If V_{IN} is below 3.8V, then write “1” to register 1Bh, bit[1] to turn on the internal V_{STRG} for the VCC LDO. If V_{IN} exceeds 3.8V, then ignore this step.
4. Write “1” to register 01h, bit[3] to start the capacitor test. The MP5514 disables the V_{STRG} charge function once V_{STRG} exceeds the set V_{FBS}. Register 01h, bit[0] does not change. Once V_{STRG} is charged, C_{STRG} is discharged via an external resistor. The ADC starts once V_{FBS} drops below the V_{FBS_REF} threshold. The ADC reads V_{STRG}, and stores data in ADC_BACKUP_VOLTAGE_DATA2 register. The internal timer starts once V_{FBS} drops below the V_{FBS_REF} threshold.
5. If register 02h, bit[7] is set to 1, then the capacitor test is complete once the interrupt signal is received from the MP5514. Once V_{STRG} drops to the PGS threshold, the part stops discharging V_{STRG}, and the timer value is written to the CAP_TEST_TIMER register. If the PGS falling threshold is triggered, then the MP5514 starts up the ADC again and stores the data in the ADC_BACKUP_VOLTAGE_DATA1 register. Once ADC conversion is complete, the MP5514 sets the CAP_TEST_DONE bit. Register 01h, bit[3] is reset to 0 to clear the START_CAP_TEST bit. The boost charge function is enabled automatically.
6. Read register 12h, bits[7:0] and register 13h, bits[1:0] to store the final voltage (V_{FINAL}) (10 bits total). Register 12h is the high byte, and register 13h is the low byte. Read register 14h, bits[7:0] and register 15h, bits[1:0] to the initial voltage ($V_{INITIAL}$) (10 bits total). Register 14h is the high byte, and register 15h is the low byte. Read register 16h, bits[7:0] and register 17h, bits[7:0] to store the time (16 bits total). Register 16h is the low byte, and register 17h is the high byte.
7. Write “1” to register 02h, bit[7] to reset the capacitor test interrupt. Write “1” to register 04h, bit[2] and bit[6] to enable the PGS_NOT_ OK and ADC_DONE functions. If register 1Bh, bit[1] was set to 1 in step 3, write “0” to this bit.
8. The ADC results can be calculated with Equation (7):

$$C_{STRG} = \frac{Time}{R_{DISCH} \times \ln\left(\frac{V_{INITIAL} + R_{DISCH} \times I_{LDO}}{V_{FINAL} + R_{DISCH} \times I_{LDO}}\right)} \quad (7)$$

Where $V_{INITIAL}$ is V_{STRG} before the discharge timer starts (stored in ADC_BACKUP_VOLTAGE_DATA2), V_{FINAL} is V_{STRG} after being discharged (stored in ADC_BACKUP_VOLTAGE_DATA1), R_{DISCH} is the resistor between STRG and RTEST, and I_{LDO} is the VCC LDO current.

If V_{IN} drops below 5V, and register 1Bh, bit[1] is set to 1, then I_{LDO} is typically 2mA; otherwise, I_{LDO} is 0mA. Once the capacitor test is complete, reset the LDO_EN bit to save the operation current (the LDO unit for the capacitor test should be mA). The time is recorded in the CAP_TEST_TIMER register (the unit for the register data is 1ms).

See the ADC Results section on page 37 for the test times and voltage calculations.

If V_{IN} fails during the capacitor test, then the MP5514 enters buck release mode. The capacitor test does not work in buck release mode. In buck release mode, the capacitor test cannot start, and "1" cannot be written to START_CAP_TEST.

If an OC fault occurs during the capacitor test, and OC_RLS_EN is set to 1, then the capacitor test stops. The isolation MOSFET clamps the current, and the backup circuit enters buck release mode to support the additional current.

For more information, refer to the MPS application note AN125.

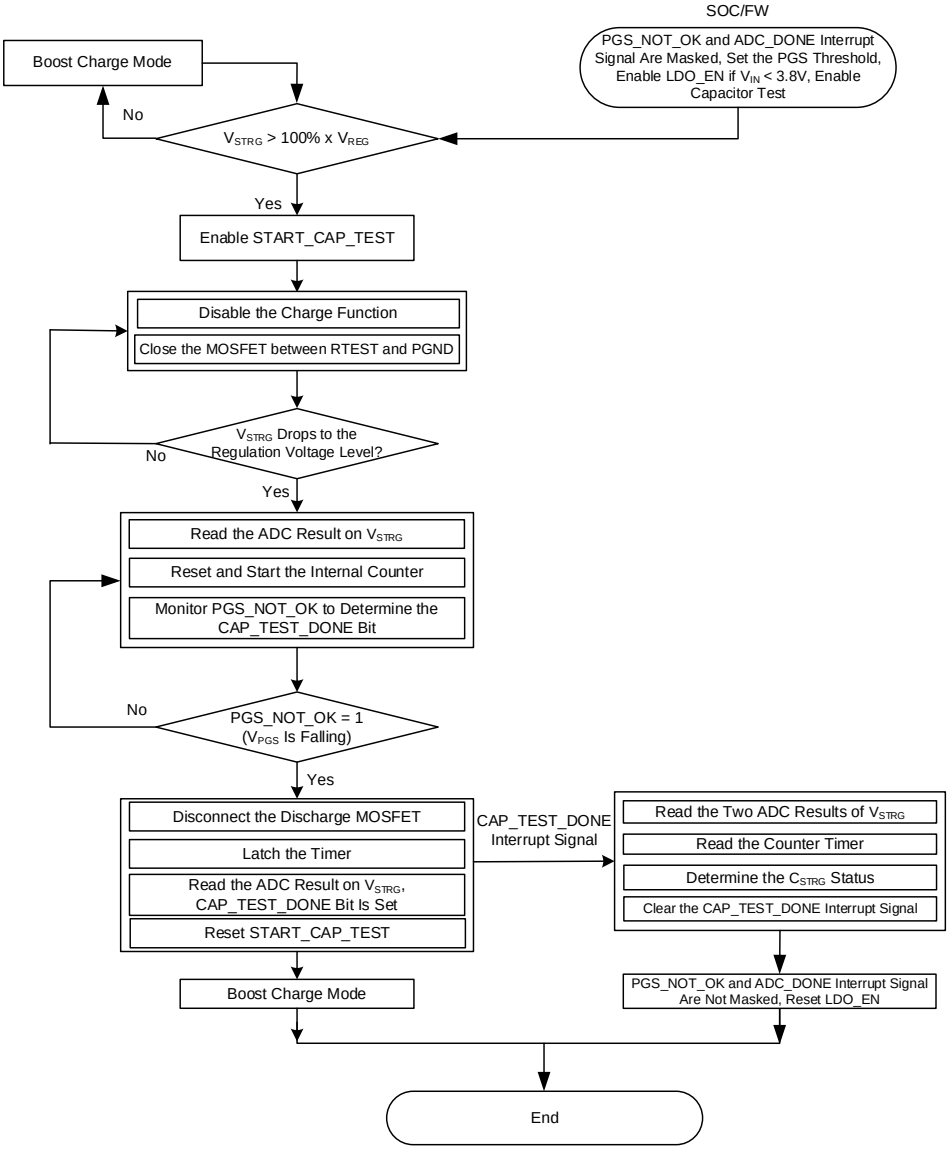


Figure 6: Storage Capacitor Test Flowchart

VCC Power Management

The MP5514's internal circuitry is powered by the VCC capacitor (C_{VCC}). VCC is supplied by V_{IN}, V_{BUS}, or V_{STRG} (see Table 1).

Table 1: VCC Power Sources

Operation Mode	LDO_EN Bit	Power Source
Boost charge	0 (default)	VCC is supplied by V_{IN} or V_{BUS} (whichever is higher)
Buck discharge	0 (default)	If V_{CC} > 4.5V, then VCC is supplied by V_{IN} or V_{BUS} (whichever is higher). If V_{CC} < 4.5V, then the LDO between STRG and VCC is enabled and regulates V_{CC} at about 4.5V.
Boost charge	1	
Buck discharge	1	

The LDO_EN bit (register 1Bh, bit[1]) is used for ADC conversion, including the capacitor test while V_{IN} and V_{BUS} are low. If V_{IN} and V_{BUS} are low, enable the LDO_EN bit before ADC operation. See to the 10-Bit Analog-to-Digital Converter (ADC) section on page 25 for more details.

A ≥1µF capacitor is required on VCC. If the part starts up from a ≤3V V_{IN}, then V_{CC} is low due to the VIN to VCC voltage drop. Any external current on VCC (e.g. a PFI pull-up resistor) pulls V_{CC} down, and makes it difficult to start up the MP5514. It is recommended to use a 100kΩ pull-up resistor for the PFI and INT pins. If V_{BUS} is below 5V, then PFI and INT can be pulled up to V_{BUS}.

The MP5514 can start up from a low V_{IN} (2.7V) at ≥25°C temperatures. If the temperature is below 25°C, then the UVLO threshold increases. Connect an external Schottky diode between the VIN and VCC pins to have the IC start up from a 2.7V V_{IN} at low temperatures (below 25°C). It is recommended to add this diode, even if V_{IN} is 3V at temperatures below -40°C.

Enable (EN) Control

The MP5514's enable (EN) pin works with the EN bit to enable the internal circuit. The MP5514 is enabled once both the EN pin and EN bit are high. During application, the EN pin cannot be connected to a voltage exceeding 6.5V. For resistor pull-up conditions, an internal Zener diode clamps the voltage at the EN pin voltage (V_{EN}). The maximum pull-up current for the internal Zener diode should be <1mA. 100kΩ pull-up resistors connected to both VIN and VB are recommended if the resistors are pulled up to V_{IN} and V_{BUS}.

SAS Function

The MP5514 provides a forced backup mode for energy discharging. This function works together with the SAS_DLY, SAS_ASSERT_TIME, and SAS_NEGATE_TIME I^2C register bits.

After start up, the MP5514 ignores the SAS voltage (V_{SAS}) being pulled high for the time set via the SAS_DLY bit. If V_{SAS} remains high for longer than the time set via the SAS_ASSERT_TIME bit, then the isolation MOSFET turns off, the part enters buck release mode, and the PFI voltage (V_{PFI}) is pulled low to indicate the power status. If V_{BUS} drops below V_{BUS_UVLO} before SAS negates, then the buck converter shuts down, and V_{CC} continues working. The MP5514 operates with a new start cycle once SAS is negated by holding V_{SAS} low for the time set via the SAS_NEGATE_TIME bit. If V_{BUS} exceeds V_{BUS_UVLO} while SAS is negated, then V_{PFI} is pulled high, and the isolation MOSFET operates as the V_{IN} power recovery once V_{BUS} triggers V_{BUS} UVLO.

Input Power Failure Indicator (PFI)

If V_{DET} drops below 0.99 x V_{DET_REF}, then V_{PFI} is pulled low internally to indicate a power failure, and the part exits boost charge mode. If V_{DET} exceeds 1.02 x V_{DET_REF}, then V_{PFI} is pulled high (if it is pulled up via an external resistor). The MP5514 does not exit buck release mode until V_{BUS} is discharged to V_{BUS_UVLO} or the IC resets (even if V_{PFI} is high).

Bus Voltage Power Good (PG) Indication

If the bus feedback voltage (V_{FBB}) drops below 0.9 x V_{FBB_REF}, then PGB is pulled low internally. If V_{FBB} exceeds 0.95 x V_{FBB_REF}, then PGB is pulled high.

Storage Voltage PG Indication

The storage power good (PG) threshold can be configured via by the PGS threshold bits (register 06h, bits[3:0]). The default PGS falling threshold is 95% of V_{FBS_REF}. If the storage feedback voltage (V_{FBS}) drops below 0.95 x V_{FBS_REF}, then PGS is pulled low internally. If V_{FBS} exceeds 0.97 x V_{FBS_REF}, then PGS is pulled high.

Input Over-Voltage Protection (OVP)

A resistor divider from V_{IN} to OVP sets the input over-voltage protection (OVP) threshold (V_{IN_OVP}). Once the OVP pin voltage (V_{OVP}) exceeds 0.81V, the MP5514 enters buck backup mode. Once V_{OVP} drops below 0.765V, and the buck stop operating, V_{BUS} triggers V_{BUS_UVLO}, and the MP5514 restarts automatically via a new start-up cycle with a TPOR process. An INPUT_OVER-VOLTAGE register bit records the OVP event, and generates an interrupt signal on INT if it is unmasked.

10-Bit Analog-to-Digital Converter (ADC)

The MP5514 integrates a 10-bit ADC to measure V_{IN}, I_{IN}, V_{STRG}, and the TEMP pin's temperature sensor voltage. The START_ADC register enables ADC conversion. ADC_DONE bit is set if an ADC conversion completes. An interrupt request to the controller can be set if the ADC_DONE bit is set. Figure 7 shows the ADC setting flowchart. See the ADC Results register on page 37 for more details.

If V_{IN} drops below 3.8V, use the host chip to set register 0x1Bh, bit[1] to 1 before enabling the ADC or capacitor test functions. Setting this bit enables the LDO between STRG and VCC, provides more margins for the internal ADC reference, and insures ADC accuracy. The LDO draws about 2mA of current from STRG. The LDO should be disabled once ADC conversion or the capacitor test is complete. The LDO_EN bit is set to 0 by default.

Interrupt Control

If a fault condition in the interrupt register occurs when the fault bits are not masked, then the INT pin is pulled high. This interrupt signal is asserted to indicate to the SoC that a fault has occurred. While there is an existing interrupt event, and a second interrupt event can occur before the SoC resets INT (while the INT voltage is high). The MP5514 keeps INT high until the SoC resets all interrupt events (see Figure 8).

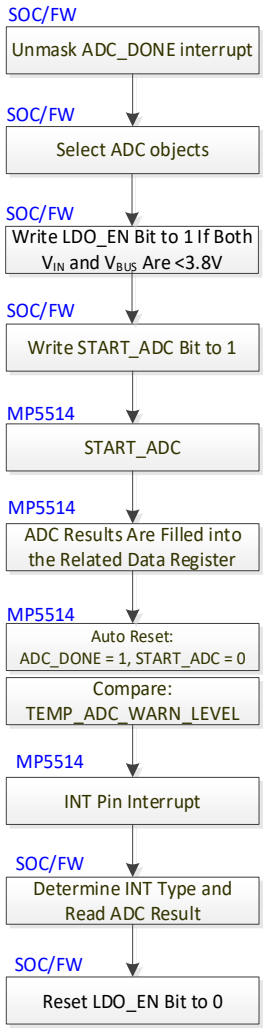


Figure 7: ADC Converter Flowchart

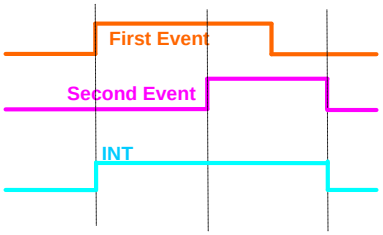


Figure 8: Interrupt Sequence

If a fault occurs, the MP5514 generates an interrupt and other actions (see Table 2 on page 26).

I²C Timeout

If SCL is pulled low or high for up to 25ms, or SDA is pulled low for up to 450ms, the I²C is reset. The I²C timeout function can be enabled by setting I2C_TO_EN to 1, and can be disabled by setting I2C_TO_EN to 0.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds 120°C, the IC_TJ_WARN bit is set to 1, which sends an interrupt signal to the SoC. Write 1 to the IC TJ WARN bit to reset the interrupt event once the temperature drops below 100°C.

If T_J exceeds 150°C, the MP5514 enters buck backup mode, and discharges energy from V_{STRG} to V_{BUS}. In this scenario, the isolation MOSFET is off and PFI is low. The buck is released until the energy is fully discharged. Once T_J drops below 125°C, the MP5514 starts up again through VIN, and operates as the V_{IN} power recovery. There is an interrupt signal for a 150°C over-temperature (OT) fault. This interrupt signal can be reset by writing 1 to the IC_TJ_WARN bit.

If T_J exceeds 165°C, the device shuts down.

Register Default Value Configuration

The MP5514 has multiple control register bits, all of which have a fixed default value after a power reset. After start-up, all of the bits can be configured by writing to the I²C. Registers 0x06h, 0x07h, 0x21h, 0x26h, and the device I²C address default value can be configured. Different default values can be configured to fit different system requirements.

Table 2: Fault Response

Event	Status Bit	Status/INT Reset Condition	PFI	INT	MP5514 Power Action
Input OC fault	INPUT_OVER-CURRENT	POR, write 1 to this bit	No action	Yes (high)	The device limits I_{IN}; If OC_RLS_EN = 1, then the buck starts up once V_{BUS} drops below V_{FBB_REF}
Input power failure	N/A	N/A	Yes (low)	No action	The isolation MOSFET is off, and the IC enters buck release mode
OVP pin over-voltage (OV) fault	INPUT OVER-VOLTAGE	POR, write 1 to this bit	Yes (low)	Yes (high)	The isolation MOSFET is off, and IC enters buck release mode
V_{STRG} triggers PGS falling threshold	PGS_NOT_OK	POR, write 1 to this bit	No action	Yes (high)	No action
TEMP pin warning	TEMP_WARN	POR, write 1 to this bit	No action	Yes (high)	No action
Die high-temperature warning	IC_TJ_WARN	POR, write 1 to this bit	No action	Yes (high)	No action
Die OT to forced buck	IC_TJ_ SHUTDOWN	POR, write 1 to this bit	Yes (low)	Yes (high)	The isolation MOSFET is off, and the IC enters buck release mode, then shuts down once the power is discharged
SAS disabled supply	SAS_DIS	POR, write 1 to this bit	Yes (low)	Yes (high)	The isolation MOSFET is off, and the IC enters buck release mode
ADC complete	ADC_DONE	POR, write 1 to this bit	No action	Yes (high)	No action
Capacitor test complete	CAP_TEST_ DONE	POR, write 1 to this bit	No action	Yes (high)	See Figure 6 on page 23

It is suggested to use the default register value of registers 0x06h, 0x07h, 0x21h, and device I²C address for application. If different default values are needed for these registers, please contact MPS for a program solution.

I²C Interface

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP5514 interface is an I²C slave. The I²C interface adds flexibility to the SSD power system control by different register configurations.

The MP5514 7-bit device address is defined as 33h (011 0011). When the master sends an 8-bit address value, the 7-bit I²C address should be followed by a 0 or 1 to indicate a write or read operation, respectively.

I²C Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. A high or low state of the data line can change only when the clock signal on the SCL line is low as shown in Figure 9.

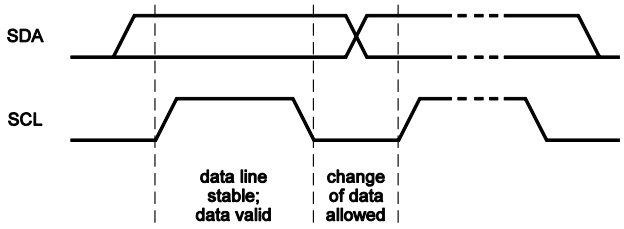


Figure 9: Bit Transfer on the I²C Bus

The start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

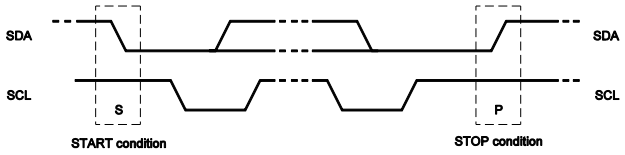


Figure 10: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again after a minimum of 4.7µs after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are identical functionally.

I²C Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so it remains stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 11. After the start condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit, which is a data direction bit (R/W). A zero (0) indicates a transmission (write), and a one (1) indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

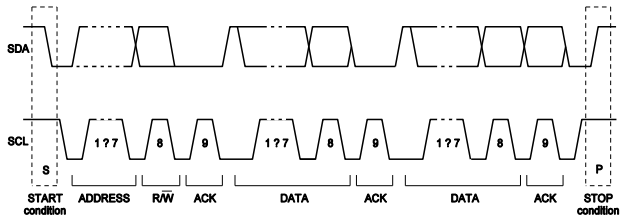


Figure 11: Complete Data Transfer

The MP5514 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements and requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP5514 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5514. The MP5514 performs an update on the falling edge of the LSB byte.

Figure 12 shows an example of an I²C read and write command.

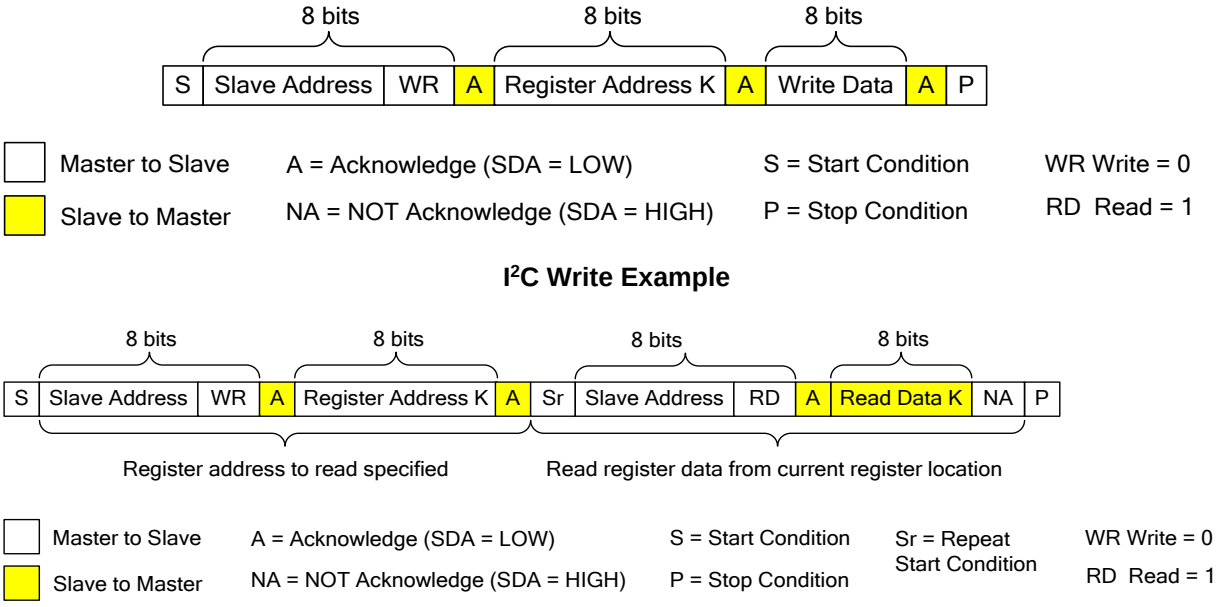


Figure 12: I²C Read and Write

ONE-TIME PROGRAMMABLE MEMORY (OTP)

Table 3: OTP Table

Address	Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x06h	BACKUP_CAP_THRESHOLD	FBS_HYS	VIN_RECOVER_MODE	ICH		PGS_THRESHOLD			
0x07h	TEMP_WARN_THRESHOLD	EFUSE_UVLO		OC_RLS_EN	TEMP_ADC_WARN_LEVEL				
0x08h	REVERSE_CURRENT_FAST_OFF	REVERSE_CURRENT_FAST_OFF_DISABLE	-	-	-	-	-	-	-
0x21h	SYS_CONTROL_3	INTERNAL_ILIM_THRESHOLD			DVDT		TPOR		EN
0x26h	SAS_CONTROL	I2C_TO_EN	SAS_DLY	SAS_ASSERT_TIME		SAS_NEGATE_TIME		-	-

Table 3: Default OTP Values

Register	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
06h	FBS_HYS (0: 9mV)	VIN_RECOVER_MODE (0: Operates in buck release mode until V_{BUS} drops below V_{BUS_UVLO} once V_{IN} recovers)	ICH (11: 2A)		PGS_THRESHOLD (1111: 95% of V_{FBS_REF})			
07h	EFUSE_UVLO (11: 9.5V rising threshold, 3.4 falling threshold)		OC_RLS_EN (0: PLP enter buck release mode only if DET is triggered)	TEMP_ADC_WARN_LEVEL (11111)				
08H	RC_FAST_OFF_DISABLE (0: Enabled)	-	-	-	-	-	-	-
21h	INTERNAL_ILIM_THRESHOLD (000: 6.6A)			DVDT (00: 7.5V/ms)		TPOR (00: 1.6ms)		EN (1: Enabled)
26h	I2C_TO_EN (1: I^2C resets if SCL is pulled low or high for up to 25ms, or if SDA is pulled low for up to 450ms)	SAS_DLY (1: 30s)	SAS_ASSERT_TIME (10: 5s)		SAS_NEGATE_TIME (11:30s)		-	-

I²C REGISTER MAP

Address	Register	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Reset State	
00h	VENDOR_ID	R	FAB		MAJOR_REV		MINOR_REV		VENDOR_ID		0000 0000	
01h	SYSTEM_CONTROL_1	R/W	-	-	-	-	START_CAP_TEST	START_ADC	-	ENCH	0000 0001	
02h	INTERRUPT1_STATUS	R/W	CAP_TEST_DONE	ADC_DONE	-	INPUT_OVER-CURRENT	INPUT_OVER-VOLTAGE	PGS_NOT_OK	-	TEMP_WARN	0000 0100	
03h	INTERRUPT2_STATUS	R/W	-	SAS_DIS	ISOFET_OFF	IC_TJ_SHUTDOWN	IC_TJ_WARN	-	-	-	0010 0000	
04h	INTERRUPT1_MASK_CONTROL	R/W	CAP_TEST_DONE_MASK	ADC_DONE_MASK	-	INPUT_OVER-CURRENT_MASK	INPUT_OVER-VOLTAGE_MASK	PGS_NOT_OK_MASK	-	TEMP_WARN_MASK	0010 0100	
05h	INTERRUPT2_MASK_CONTROL	R/W	-	SAS_DIS_MASK	ISOFET_OFF_MASK	IC_TJ_SHUTDOWN_MASK	IC_TJ_WARN_MASK	-	-	-	0010 0101	
06h	BACKUP_CAP_THRESHOLD	R/W	FBS_HYS	VIN_RECOVER_MODE	ICH		PGS_THRESHOLD				0011 1111	
07h	TEMP_WARN_THRESHOLD	R/W	EFUSE_UVLO		OC_RLS_EN	TEMP_ADC_WARN_LEVEL					1101 1111	
08h	REVERSE_CURRENT_FAST_OFF	R/W	REVERSE_CURRENT_FAST_OFF_DISABLE	-	-	-	-	-	-	-	0001 1110	
09h	ADC_SOURCE_SELECT	R/W	-	-	-	BACKUP_VOLTAGE	-	TEMP_PIN	INPUT_CURRENT	INPUT_VOLTAGE	0000 0000	
0Ah	ADC_INPUT_VOLTAGE_DATA	R	VIN_HIGH_BYTE								0000 0000	
0Bh		R	-	-	-	-	-	-	VIN_LOW_BYTE		0000 0000	
0Ch	ADC_INPUT_CURRENT_DATA	R	I_IN_HIGH_BYTE								0000 0000	
0Dh		R	-	-	-	-	-	-	I_IN_LOW_BYTE		0000 0000	
0Eh	ADC_TEMP_VOLTAGE_DATA	R	TEMP_HIGH_BYTE								0000 0000	
0Fh		R	-	-	-	-	-	-	TEMP_LOW_BYTE		0000 0000	
12h	ADC_BACKUP_VOLTAGE_DATA1	R	VSTRG1_HIGH_BYTE								0000 0000	
13h		R	-	-	-	-	-	-	VSTRG1_LOW_BYTE		0000 0000	
14h	ADC_BACKUP_VOLTAGE_DATA2	R	VSTRG2_HIGH_BYTE								0000 0000	
15h		R	-	-	-	-	-	-	VSTRG2_LOW_BYTE		0000 0000	
16h	CAP_TEST_TIMER	R	CAP_TEST_TIMER_LOW_BYTE								0000 0000	
17h		R	CAP_TEST_TIMER_HIGH_BYTE								0000 0000	
1Bh	VIN_RECOVER_CONTROL	R/W	-	-	-	-	-	-	LDO_EN	-	0000 0000	
1Fh	RESERVED	R	-	RESERVED (13)							0011 0011	
20h	SYS_CONTROL_2	R/W	RESERVED (13)	INPUT_ILIMT SET	RESERVED (13)	RESERVED (13)	BUCK_FSW				FORCE_BUCK_RELEASE	1000 1000
21h	SYS_CONTROL_3	R/W	INTERNAL_ILIM_THRESHOLD			DVDT			TPOR		EN	0000 0001
22h	SYS_CONTROL_4	R/W	-	-	-	-		ILIM_EN	ILIM_TUNE			0000 0000
26h	SAS_CONTROL	R	I2C_TO_EN	SAS_DLY	SAS_ASSERT_TIME			SAS_NEGATE_TIME		RESERVED (13)	RESERVED (13)	1110 1100

Note:

15) Reserved bits. Do not write different values to these bits in application.

Vendor ID (00h)

Access: Read-only

Bits	Name	Description	Default Value
7:6	FAB	Fab location.	00
5:4	MAJOR_REV	Major revision.	00
3:2	MINOR_REV	Minor revision.	00
1:0	VENDOR_ID	Vendor ID.	00

System Control 1 (01h)

Access: Read/Write

Bits	Name	Description	Default Value
D[3]	START_CAP_TEST	Capacitor test start enable bit. If the input voltage (V_{IN}) is below 3.8V, then the LDO_EN bit should be set to 1 before the capacitor test starts. The LDO_EN bit should be disabled once the capacitor test is complete. 1: Starts the capacitor test on the storage capacitors; resets to 0 once the capacitor test is complete 0: Capacitor test function is disabled	00
D[2]	START_ADC	Analog-to-digital converter (ADC) conversion enable bit. The LDO_EN bit should be set to 1 before starting the ADC. If both V_{IN} and VB are below 3.8V, then disable the LDO_EN bit after ADC is completed. 1: ADC conversion begins; resets to 0 once the capacitor test is complete 0: An ADC conversion event has not occurred	00
D[0]	ENCH	Storage boost enable bit. This bit cannot be written to in buck release mode. This bit does not affect buck release mode once the storage voltage (V_{STRG}) is charged high (even if ENCH is set to 0). 1: Boost charge function is enabled 0: Boost charge function is disabled	00

Interrupt 1 Status (02h)

Access: Read/Write

Bits	Name	Description	Default Value
D[7]	CAP_TEST_DONE	Capacitor test complete indication bit. 1: The capacitor test is complete, and the discharge time is stored in the CAP_TEST_TIMER registers. This generates an interrupt on INT if unmasked. Write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: A capacitor test event has not occurred	0
D[6]	ADC_DONE	Analog-to-digital (ADC) conversion complete indication bit. 1: ADC conversion is complete. This generates an interrupt on INT if unmasked. Write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: An ADC event has not occurred	0
D[4]	INPUT_OVER_CURRENT	VIN to VB input current limit (I_{IN_LIMIT}) trigger indication bit. 1: V_{IN} has triggered I_{IN_LIMIT}. This generates an interrupt on INT if unmasked. Once the I_{IN_LIMIT} event is removed, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: An I_{IN_LIMIT} event has not occurred	0
D[3]	INPUT_OVER_VOLTAGE	Over-voltage (OV) on the OVP pin indication bit. 1: The OVP pin voltage (V_{OVP}) has exceeded the OVP threshold (V_{IN_OVP}). This generates an interrupt on INT if unmasked. Once the over-voltage event is removed, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: An OV event has not occurred	0
D[2]	PGS_NOT_OK	Storage voltage (V_{STRG}) power not good indication bit. 1: V_{STRG} is below the PGS threshold. If the PGS pin detects that V_{STRG} is too low, the device generates an interrupt on INT if unmasked. Once V_{STRG} exceeds the PGS threshold, write 1 to this bit to reset the interrupt event (and to reset this bit to 0). PGS resets to high automatically once V_{STRG} exceeds the PGS threshold 0: V_{STRG} power has not dropped below the PGS threshold	1
D[0]	TEMP_WARN	Temperature sensor high-voltage warning indication bit. 1: The external temperature sensor on the TEMP pin has exceeded the TEMP_WARN level. This generates an interrupt on INT if unmasked. If a new ADC result from TEMP is below the threshold, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: There is no TEMP_ADC result, or the TEMP_ADC result is below the TEMP_WARN level	0

Interrupt 2 Status (03h)

Access: Read/Write

Bits	Name	Description	Default Value
D[6]	SAS_DIS	SAS-forced buck mode indication bit. 1: The IC is disabled by the SAS signal, and forced into buck mode. This generates an interrupt on INT if unmasked. After SAS resets to low, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: A SAS force buck event has not occurred	0
D[5]	ISOFET_OFF	VIN to VB MOSFET is off indication bit. 1: The input isolation MOSFET is off. This generates an interrupt on INT if unmasked. Once the isolation MOSFET turns on again, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: The isolation MOSFET is always on	1
D[4]	IC_TJ_ SHUTDOWN	Thermal shutdown indication bit. 1: The junction temperature (T_J) has exceeded 150°C. This generates an interrupt on INT if unmasked. After the temperature drops below 125°C, write 1 to this bit to reset the interrupt event (and to reset this bit to 0). The MP5514 resumes operation once T_J drops, even if the interrupt signal is not cleared 0: Thermal shutdown has not occurred	0
D[3]	IC_TJ_WARN	High temperature warning bit. 1: T_J has exceeded 125°C. This generates an interrupt on INT if unmasked. Once T_J drops below 100°C, write 1 to this bit to reset the interrupt event (and to reset this bit to 0) 0: T_J has not exceeded 125°C; a high temperature warning has not occurred	0

Interrupt 1 Mask Control (04h)

Access: Read/Write

Bits	Name	Description	Default Value
D[7]	CAP_TEST_ DONE_MASK	Capacitor test complete interrupt mask. 1: The CAP_TEST_DONE interrupt is masked. The CAP_TEST_DONE status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The CAP_TEST_DONE interrupt is not masked	0
D[6]	ADC_DONE_MASK	ADC complete interrupt mask. 1: The ADC_DONE interrupt is masked. The ADC_DONE status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The ADC_DONE interrupt is not masked	0
D[4]	INPUT_OVER_ CURRENT_MASK	VIN to VB I_{IN_LIMIT} interrupt mask. 1: The INPUT_OVER_CURRENT interrupt is masked. The INPUT_OVER_CURRENT status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The INPUT_OVER_CURRENT interrupt is not masked	0
D[3]	INPUT_OVER_ VOLTAGE_MASK	OVP interrupt mask. 1: The INPUT_OVER_VOLTAGE interrupt is masked. The INPUT_OVER_VOLTAGE status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: INPUT_OVER_VOLTAGE is not masked	0
D[2]	PGS_NOT_ OK_MASK	PGS power not good interrupt mask. 1: The PGS_NOT_OK interrupt is masked. The PGS_NOT_OK status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The PGS_NOT_OK interrupt is not masked	1
D[0]	TEMP_ WARN_MASK	Temperature sensor high-voltage warning interrupt mask. 1: The TEMP_WARN interrupt is masked. The TEMP_WARN status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The TEMP_WARN interrupt is not masked	0

Interrupt 2 Mask Control (05h)

Access: Read/Write

Bits	Name	Description	Default Value
D[6]	SAS_DIS_MASK	SAS force buck event interrupt mask. 1: The SAS_DIS interrupt is masked. The SAS_DIS status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The SAS_DIS interrupt is not masked	0
D[5]	ISOFET_OFF_MASK	Isolation MOSFET off event interrupt mask. 1: The ISOFET_OFF interrupt is masked. The ISOFET_OFF status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The ISOFET_OFF interrupt is not masked	1
D[4]	IC_TJ_ SHUTDOWN_MASK	OTP interrupt mask. 1: The IC_TJ_SHUTDOWN interrupt is not masked. The IC_TJ_SHUTDOWN status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The IC_TJ_SHUTDOWN interrupt is not masked	0
D[3]	IC_TJ_WARN_MASK	High temperature warning interrupt mask. 1: The IC_TJ_WARN interrupt is masked. The IC_TJ_WARN status bit is set after an interrupt event, but this bit suppresses the interrupt signal on INT 0: The IC_TJ_WARN interrupt is not masked	0

Backup Capacitor Threshold (06h)

Access: Read/write

Bits	Name	Description	Default Value
D[7]	FBS_HYS	Boost refresh threshold. When FBS drops to V_{FBS_REF}, PLP starts switching and charges V_{FBS} to V_{FBS_REF} + FBS_HYS. 0: 9mV (typically), 13.5mV max 1: 10mV (typically), 15mV max	0
D[6]	VIN_RECOVER_ MODE	V_{IN} recovery mode. 0: The part operates in buck release mode until V_{BUS} drops below V_{BUS_UVLO} once V_{IN} recovers 1: The part exits buck release mode and charges V_S once V_{IN} recovers	0
D[5:4]	ICH	Sets the peak boost switching current limit while ICH is floating. 00: 0.5A 01: 1A 10: 1.5A 11: 2A	11
D[3:0]	PGS_THRESHOLD	Configurable PGS falling threshold, with a 1% step 0000: 80% of V_{FBS_REF} … 1111: 95% of V_{FBS_REF}	1111

Temperature Warning Threshold (07h)

Access: Read/Write

Bits	Name	Description	Default Value
D[7:6]	EFUSE_UVLO	E-fuse UVLO threshold. These bits are assigned to the OTP pin. After cycling the power, the UVLO rising and falling threshold are set to the OTP value. 00: The UVLO rising threshold is 2.5V, and the falling threshold is 2.3V 01: The UVLO rising threshold is 3.7V, and the falling threshold is 3.4V 10: The UVLO rising threshold is 7.2V, and the falling threshold is 3.4V 11: The UVLO rising threshold is 9.5V, and the falling threshold is 3.4V	11
D[5]	OC_RLS_EN	Backup buck converter over-current (OC) response. 0: PLP enters buck release mode only if DET is triggered. 1: PLP enters buck release mode if DET is triggered or EFUSE_OC and FBB drop below V_{FBB_REF}	0
D[4:0]	TEMP_ADC_ WARN_ LEVEL	Sets the warning level for the TEMP pin voltage ADC results (from external sensor). The TEMP_ADC results high bits are compared to this warning level.	11111

Reverse Current Fast-Off (08h)

Access: Read/Write

Bits	Name	Description	Default Value
D[7]	REVERSE_ CURRENT_FAST_ OFF_DISABLE	Enables the reverse-current fast-off function. 0: The reverse-current fast-off function is enabled 1: The reverse-current fast-off function is disabled	0

ADC Source Select (09h)

Access: Read/Write

Bits	Name	Description	Default Value
D[4]	BACKUP_VOLTAGE	Enables the V_{STRG} ADC conversion. 1: V_{STRG} ADC conversion is enabled 0: V_{STRG} ADC conversion is disabled	0
D[2]	TEMP_PIN	Enables the temperature sensor voltage ADC conversion. 1: Temperature sensor voltage ADC conversion is enabled 0: Temperature sensor voltage ADC conversion is disabled	0
D[1]	INPUT_CURRENT	Enables the input current signal ADC conversion. The input current (I_{IN}) is monitored via the ILIM pin. If the current triggers the I_{IN} limit (I_{IN_LIMIT}), then the ILIM voltage (V_{ILIM}) is 1.09V. Calculate the current based on the ILIM resistor (R_{ILIM}) setting. 1: I_{IN} signal ADC conversion is enabled 0: I_{IN} signal ADC conversion is disabled	0
D[0]	INPUT_VOLTAGE	Enables the V_{IN} ADC conversion. 1: V_{IN} ADC conversion is enabled 0: V_{IN} ADC conversion is disabled	0

ADC Results (0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 12h, 13h, 14h, and 15h)

Access: Read-Only

Bits	Name	Description	Default Value
0Ah, D[7:0]	ADC_INPUT_ VOLTAGE_DATA	High bits of the V_{IN} ADC results.	0000 0000
0Bh, D[1:0]		Low bits of the V_{IN} ADC results. LSB = 18.4 / 1023(V)	00
0Ch, D[7:0]	ADC_INPUT_ CURRENT_DATA	High bits of the I_{IN} ADC results.	0000 0000
0Dh, D[1:0]		Low bits of the I_{IN} ADC results. V_LSB = 1.28 / 1023 (V) IN = V_LSB x BIN2DEC(D[9:0]) x 64.26 / R_{ILIM} + 0.241 / R_{ILIM} + 0.08(A) Where R_{ILIM} is in kΩ.	00
0Eh D[7:0]	ADC_TEMP_ VOLTAGE_DATA	High bits of the temperature sensor voltage ADC results.	0000 0000
0Fh D[1:0]		Low bits of the temperature sensor voltage ADC results. LSB = 1.28 / 1023 (V)	00
12h, D[7:0]	ADC_BACKUP_ VOLTAGE_DATA1	High bits of the V_{STRG} ADC1 results.	0000 0000
13h, D[1:0]		Low bits of the V_{STRG} ADC1 results. LSB = 40.1 / 1023 (V)	00
14h D[7:0]	ADC_BACKUP_ VOLTAGE_DATA2	High bits of backup storage voltage ADC2 results.	0000 0000
15h D[1:0]		Low bits of the V_{STRG} ADC2 results. LSB = 40.1 / 1023 (V)	00

Capacitor Test Timer (16h and 17h)

Access: Read-Only

Bits	Name	Description	Default Value
16h, D[7:0]	CAP_TEST_ TIMER	Low bits of the capacitor test timer results. LSB = 1ms	0000 0000
17h, D[7:0]		High bits of the capacitor test timer results.	0000 0000

VIN Recover Control (1Bh)

Access: Read/Write

Bits	Name	Description	Default Value
D[1]	LDO_EN	0: Disables the LDO from STRG to VCC. 1: Enables the LDO from STRG to VCC. It is recommended to only enable the LDO during the ADC or capacitor test if both V_{IN} and V_{BUS} are below 3.8V. Disable the LDO_EN bit after the ADC or capacitor test is complete.	0

System Control 2 (20h)

Access: Read/Write

Bits	Name	Description	Default Value
D[6]	INPUT_ILIM_SET	This bit determines how I_{IN_LIMIT} is set. 1: I_{IN_LIMIT} is set by the internal circuit 0: I_{IN_LIMIT} is set by the external R_{ILIM}	0
D[3:1]	BUCK_FSW	These bits set the buck switching frequency (f_{SW}). 000: 270kHz 001: 300kHz 010: 360kHz 011: 420kHz 100: 480kHz 101: 570kHz 110: 860kHz 111: 1.25MHz	100
D[0]	FORCE_BUCK_RELEASE	This bit forces the IC to operate in buck release mode. Once this bit is reset to 0, the MP5514 remains in buck release mode until V_{BUS} drops below V_{BUS_UVLO}. 0: No action 1: The IC is forced to enter buck release mode	0

System Control 3 (21h)

Access: Read/Write

Bits	Name	Description	Default Value
D[7:5]	INTERNAL_ILIM_ THRESHOLD	These bits set the internal I_{IN_LIMIT} threshold. 000: 6.6A 001: 5.6A 010: 2.3A 011: 2.3A 100: 2.3A 101: 1.3A 110: 4.7A 111: 3.4A	000
D[4:3]	DVDT	These bits set the V_{BUS} slew rate. 00: 7.5V/ms 01:1.5V/ms 10: 1V/ms 11: 0.67V/ms	00
D[2:1]	TPOR	These bits set the TPOR delay time while the TPOR pin is floating. 00: 1.6ms 01: 8ms 10: 32ms 11: 64ms	00
D[0]	EN	This bit enables the device. The EN bit is not writable during buck release mode unless until V_{BUS} drops below V_{BUS_UVLO}. 0: The MP5514 is disabled 1: The MP5514 is enabled	1

System Control 4 (22h)

Access: Read/Write

Bits	Name	Description	Default Value
D[3]	ILIM_EN	This bit enables the isolation MOSFET current limit (I_{LIMIT}). 0: The isolation MOSFET I_{LIMIT} is enabled 1: The isolation MOSFET I_{LIMIT} is disabled (I_{LIMIT} can be disabled while the input OC limit status bit is set)	0
D[2:0]	ILIM_TUNE	These bits tune I_{IN_LIMIT}. 000: Keeps I_{IN_LIMIT} set at 100% 001: Decreases I_{IN_LIMIT} by 2% 010: Increases I_{IN_LIMIT} by 2% 011: Decreases I_{IN_LIMIT} by 4% 100: Increases I_{IN_LIMIT} by 4%	000

SAS_CTRL (26h)

Access: Read-only

Bits	Name	Description	Default Value
D[7]	I2C_TO_EN	I^2C reset. 0: I^2C does not reset after the timeout time 1: I^2C resets if SCL is pulled low or high for up to 25ms, or if SDA is pulled low for up to 450ms	1
D[6]	SAS_DLY	During start-up, the SAS input is ignored for the first interval set by this bit. After a reset is complete, the value changes to the set OTP value. 0: 0s 1: 30s	1
D[5:4]	SAS_ASSERT_TIME	To assert SAS signal, hold the SAS high for longer than SAS_ASSERT_TIME. After a reset is complete, changes to the set OTP value. 00: No hold time 01:1s 10: 5s 11: 10s	10
D[3:2]	SAS_NEGATE_TIME	To negate the SAS signal, hold the SAS pin low for longer than SAS_NEGATE_TIME. After a reset is complete, changes to the set OTP value. 00: No hold time 01: 1s 10: 10s 11: 30s	11

APPLICATION INFORMATION

Setting the Storage Voltage

V_{STRG} is set by the external feedback (FB) resistors R5 and R6 (see Figure 13).

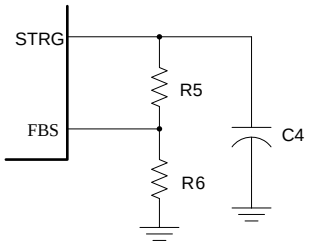


Figure 13: Storage Feedback Circuit

V_{STRG} can be calculated with Equation (8):

$$V_{STRG} = (1+\frac{R5}{R6}) \times V_{FBS\_REF} \quad (8)$$

Where V_{FBS_REF} is typically 0.8V.

R5 and R6 are not critical for normal operation. Choose R6 to be between 10kΩ and 50kΩ to reduce the bleed current and improve noise immunity. For example, if R6 is 10kΩ, then R5 can be calculated with Equation (9):

$$R5 = \frac{10k\Omega \times (V_{STRG} - V_{FBS\_REF})}{V_{FBS\_REF}} \quad (9)$$

For a 30V V_{STRG}, R5 should be 365kΩ.

Table 3 lists the recommended R5 and R6 resistances for different storage voltages.

Table 3: R5 and R6 Resistances for Different Storage Voltages

V_{STRG} (V)	R5 (kΩ)	R6 (kΩ)
12	140	10
20	240	10
30	365	10

Setting the V_{IN} Power Failure Threshold Voltage and Bus Release Regulation Voltage

The release trigger voltage is set by the external FB resistors R1 and R2 (see Figure 14).

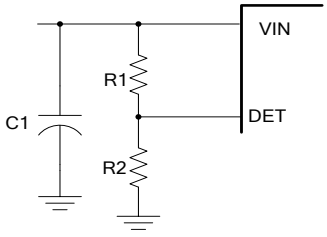


Figure 14: Release Feedback Circuit

The release trigger voltage is determined by (0.99 x V_{DET_REF}), which is 0.792V.

The input power failure release threshold (V_{PFI}) can be calculated with Equation (10):

$$V_{PFI} = (1+\frac{R1}{R2}) \times 0.792V \quad (10)$$

V_{DET} determines the release trigger voltage, and V_{FBB} determines V_{BUS_RLS} (see Figure 15).

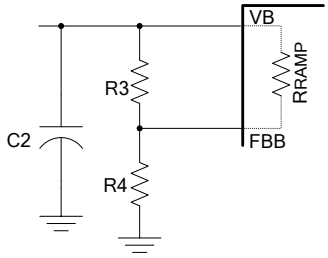


Figure 15: VB Regulation Feedback Circuit

The bus regulation voltage (V_{BUS_RLS}) can be calculated with Equation (11):

$$V_{BUS\_RLS} = (1+\frac{R3//R_{RAMP}}{R4}) \times V_{FBB\_REF} \quad (11)$$

Where V_{FBB_REF} is typically 0.8V, and R_{RAMP} is an equivalent resistor that stabilizes the circuit internally (typically 9MΩ).

R3 and R4 are related to the buck release stability. Since release buck mode works during constant-on-time (COT) control, avoid using smaller resistor values that can affect the internal voltage ramp. Choose R3 to be parallel to R4. R3 and R4 should exceed 10kΩ for stable performance with a C_{BUS} between 22μF and 44μF.

Selecting the Storage Capacitor

C_{STRG} stores energy during normal operation and releases this energy to VB once VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POSCAP for most applications. Select a C_{STRG} with a voltage margin 20% above the targeted V_{STRG}. When choosing the capacitors, consider the capacitance reduction with the DC voltage offset. Different capacitors have different capacitance derating performances. Choose a capacitor with a voltage rating large enough to guarantee enough capacitance.

The required C_{STRG} depends on the length of the dying gasp (t_{DASP}) for a typical application. The required C_{STRG} can be calculated with Equation (12):

$$C_{STRG} = \frac{2 \times V_{BUS\_RLS} \times I_{RELEASE} \times t_{DASP}}{(V_{STRG}^{2} - V_{BUS\_RLS}^{2}) \times Eff} \quad (12)$$

Where $I_{RELEASE}$ is the bus release current when V_{BUS} is regulated at V_{BUS_RLS} for the DC/DC converter, t_{DASP} is the required dying gasp time, Eff is the buck converter's energy release efficiency (see the Buck Efficiency curves on page 15 for more details).

Choose a C_{STRG} that ensures enough capacitance for buck power loss. If $I_{RELEASE}$ is 3A, t_{DASP} is 20ms, V_{STRG} is 28V, V_{BUS_RLS} is 7.5V, and the efficiency is 90%, then C_{STRG} should be 1374µF.

Setting the Input Hot-Swap Current Limit

Connect a resistor between the ILIM and AGND pins to set I_{IN_LIMIT}. For example, if the ILIM resistor (R_{ILIM}), then I_{IN_LIMIT} is set to about 2A. See to the Input Current Limit section on page 20 for more details.

The MP5514 also supports an internal ILIM configuration function, which can be set by the INPUT_ILIM_SET and INTERNAL_ILIM_THRESHOLD register bits via the I^2C interface. See the INPUT ILIM SET register description on page 38 and the INTERNAL_ILIM_THRESHOLD register description on page 39 for more details.

Setting the Boost Peak Current Limit

Connect a resistor between the ICH and AGND pins to set the boost peak I_{LIMIT}. See the Storage Voltage section on page 19 for more details.

Float the ICH pin to configure the boost peak I_{LIMIT} via the ICH register bits. The boost peak current is about 2A, with a default register value of 11 (under typical conditions where V_{IN} = 12V and L = 10µH).

Selecting the Inductor

An inductor is required for supplying constant current to the load. Since boost charge mode and buck release mode share the same inductor (and the buck mode current is typically larger), it is recommended to choose an inductor that supports the buck release mode current.

If the buck is operating at a fixed frequency (480kHz), then the inductance (L) can be calculated with Equation (13):

$$L = \frac{V_{BUS\_RLS}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{BUS\_RLS}}{V_{STRG}}) \quad (13)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which can be set between 20% and 40% of the full release current.

The inductor should not saturate under the maximum peak I_L.

Setting the Start-Up Reset Delay Time

Connect a ≥1nF TPOR capacitor (C_{TPOR}) to the TPOR pin to set t_{TPOR}. Float C_{TPOR} for the default delay time (about 1.5ms). Table 4 lists the recommended capacitances for different delay times.

Table 4: TPOR Capacitances for Different t_{TPOR}

t_{TPOR} (ms)	C_{TPOR} (nF)
10	10
100	100
500	500

Setting the Bus Voltage Rise Time

Connect a ≥1nF capacitor to DVDT to set the bus voltage start-up slew rate and t_{SS}. Float this capacitor for the default soft-start slew rate (about 7.5V/ms, and 1.6ms from 0V to 12V). Table 5 lists the recommended capacitors for different soft-start slew rates.

Table 5: Capacitor Values for Different Soft-Start Slew Rates

Soft-Start Slew Rate (V/ms)	$C_{DV/DT}$ (nF)
3.9	10
0.39	100

Recommended ADC Input Range

The MP5514 ADC V_{IN} is between 0V to 1.28V. To improve ADC monitoring accuracy, it is recommended to set the target monitor voltage between 0.64V and 1.28V (i.e. in the front half of the ADC V_{IN} range). If a wider V_{IN} range is necessary, do not set the ADC V_{IN} below 0.1V to avoid errors.

The TEMP pin is used as the temperature-sense input from the thermistor to the ADC.

Do not use the ADC when the TEMP pin voltage is below 0.1V.

VCC Power Supply

VCC is powered by the VIN pin during start-up. An external load on VCC is not permitted. If the PFI and INT signals are pulled up to VCC while V_{IN} is below 3V, use 100kΩ resistors to decrease the VCC sink current during start-up.

The MP5514 can start up from a 2.7V V_{IN} at temperatures ≥25°C. If the temperature is below 25°C, then the UVLO point increases slightly. Connect an external Schottky diode between VIN and VCC if the IC should to start up with a 2.7V V_{IN} at low temperatures. This diode is recommended even if V_{IN} is 3V at -40°C).

Selecting the Bootstrap (BST) and CST Capacitors

The bootstrap (BST) capacitor (C_{BST}) supplies power to the buck converter's HS-FET. A 0.1µF to 1µF ceramic capacitor is recommended for BST decoupling. C_{CST} supplies power to the input hot-swap MOSFET and the VBO disconnect MOSFET. C_{CST} is charged by an internal charge pump. C_{CST} should be below 47nF, as it can affect the voltage charge-up slew rate. A 10nF ceramic capacitor is recommended for C_{CST}.

Storage Capacitor Test Resistor

The MP5514 discharges C_{STRG} via an external resistor between the STRG and RTEST pins. The MOSFET between RTEST and GND is about 4.5Ω, and the discharge peak current should be limited below 500mA by an external resistor. Consider the resistance if the selected RTEST resistance (R_{RTEST}) is close to 4.5Ω. Typically, a 1kΩ to 10kΩ discharge resistor is recommended to reduce the resistor's size. Other resistor values are also sufficient.

Selecting the Input Capacitor and TVS Diode

VIN capacitors are recommended to absorb voltage spikes at the input during start-up, input switching hard-off (during shutdown), or other conditions. The application determines the capacitance required. For example, if the input power trace is too long (and has a higher parasitic inductance) during the input-switch hard-off period, then more energy is pumped into the input. This means that more input capacitors are required to reduce the V_{IN} spike and remain within the safe operating range. A 0.1µF or larger input capacitor (C_{IN}) is recommended.

Consider the application inrush current requirements when selecting C_{IN}. Typically, more input capacitors result in a higher input-inrush current during hot-plugging. A smaller C_{IN} is required for a smaller inrush current. The MP5514 can operate normally with a very small C_{IN} or without any input capacitance; however, this may lead to high voltage spikes. An efficient solution is to add a TVS diode at the input to absorb the possible V_{IN} spike. This also keeps the inrush current small during hot-plugging. A typical TVS diode (e.g. SMA6J13A) V_{BUS_RLS}, is recommended.

Design Example

Table 6 is a design example following the application guidelines for the following specifications.

Table 6: Design Example

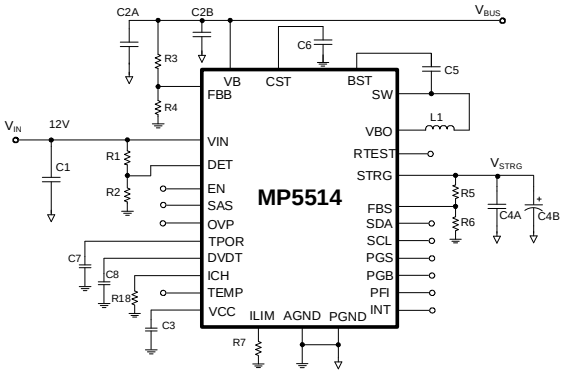
V_{IN}	12V
V_{STRG}	30V
V_{PFI}	8V
V_{BUS_RLS}	7.5V
$I_{RELEASE}$	5A

Figure 17 on page 45 shows a typical application circuit. For more device applications, refer to the related evaluation board datasheet.

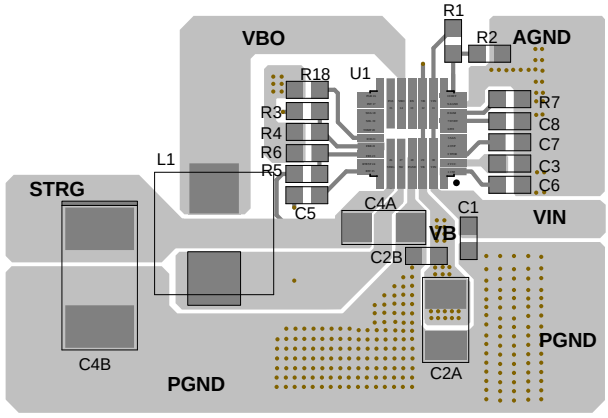
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 16, and follow the guidelines below.

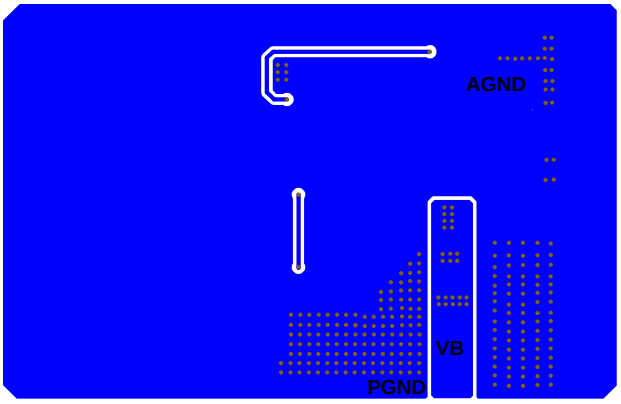
1. Connect the high-current paths (VIN, VB, VBO, SW, STRG, and PGND) using short, wide, and direct traces.
2. Keep the SW trace as short as possible.
3. Route the VBO trace away from SW.
4. Place the decoupling capacitor between VB and PGND. Place this capacitor as close to VB and PGND as possible.
5. Place the decoupling capacitor between STRG and PGND. Place this capacitor as close STRG and PGND as possible. If using a larger-value capacitor, a small ≥1µF ceramic capacitor is required. Place this small capacitor as close to STRG and PGND as possible.
6. Place the decoupling capacitor between VCC and AGND. Place this capacitor as close to VCC and AGND as possible.
7. Keep the switching node SW short and away from the feedback network.
8. Place the external feedback resistors near FBB, FBS, and DET.
9. Keep the BST voltage path (BST, C5 and SW) as short as possible.
10. Connect all of the signal grounds together at PGND with a one-point connection.



Schematic for Layout



Top Layer



Bottom Layer

Figure 16: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

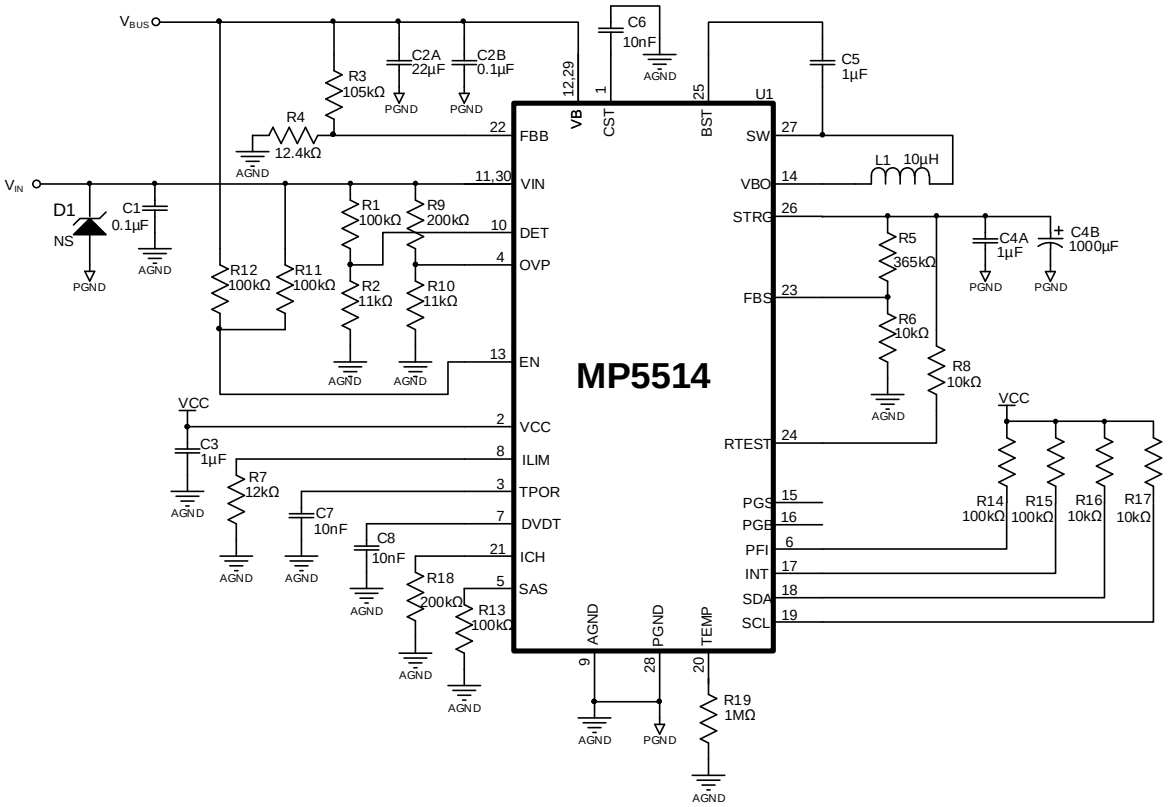
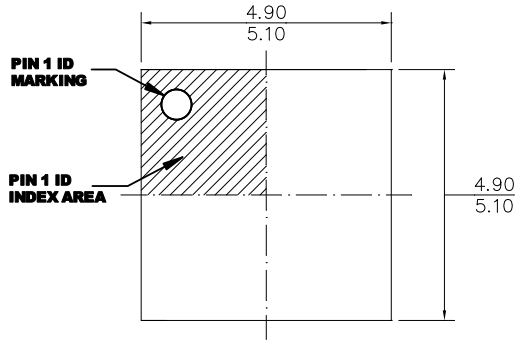


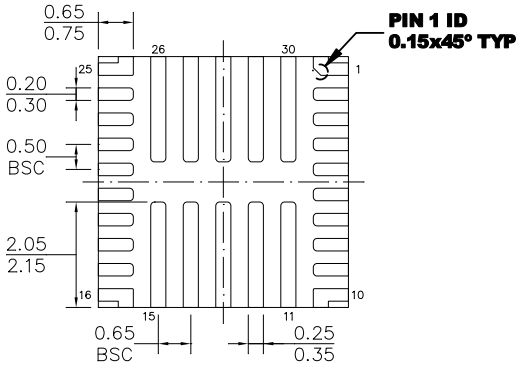
Figure 17: Typical Application Circuit (12V Input, 30V Storage)

PACKAGE INFORMATION

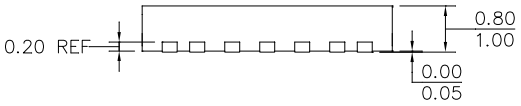
QFN-30 (5mmx5mm)



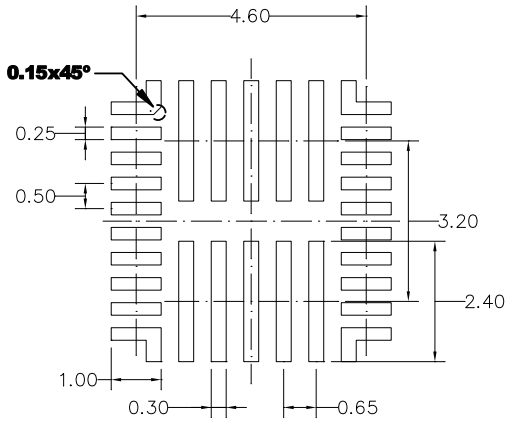
TOP VIEW



BOTTOM VIEW



SIDE VIEW

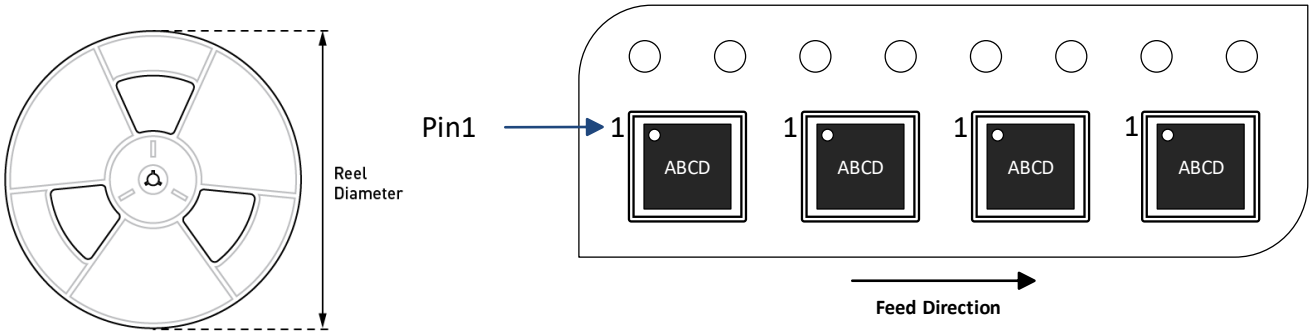


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) REFERENCEIS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5514GU-xxxx-Z	QFN-30 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/16/2023	Initial Release	-
1.1	7/18/2024	Updated part number in Ordering Information section to “MP5514GU-xxxx”; updated MSL Rating to 1	3
		Updated part number in Carrier Information section to “MP5514GU-xxxx-Z”	47