

### DESCRIPTION

The MP60G series of power modules are highly efficient synchronous switching DC/DC converters with an integral connector conforming to Intel Corporation's Voltage Regulator Module specification (VRM 8.1 DC-DC Converter Specification). The modules have additional monitoring functions for Power Good Signal, Output Enable and optional Over Voltage Protection.

A five bit voltage identification code (VID) programs the output voltage between 1.8V and 3.5V to support existing and future versions of the Pentium® II processor. The MP60G is available in several options to provide superior cost/performance tradeoff. The MP60G-5N, -5P and -NH modules convert 5V to the programmed VID output. The N designation signifies no Over Voltage Protection (OVP) while the P represents OVP. The NH module does not provide OVP and does not have heat sinks.

The MP60G-12XX modules are intended for 12V server applications. Again, the N and P designations denote the OVP option. The MP60G-12A will work from either 5V or 12V input on the 5Vin pins (Pins 1A, 2A, 3A, 1B and 2B).

### FEATURES

- Integral 40-pin header connector
- Programmable output voltage to suit processor (by VID code); adjustable from 1.8 to 3.5V
- Maximum output current 16A
- Efficiency >85% at full load
- Fast transient response

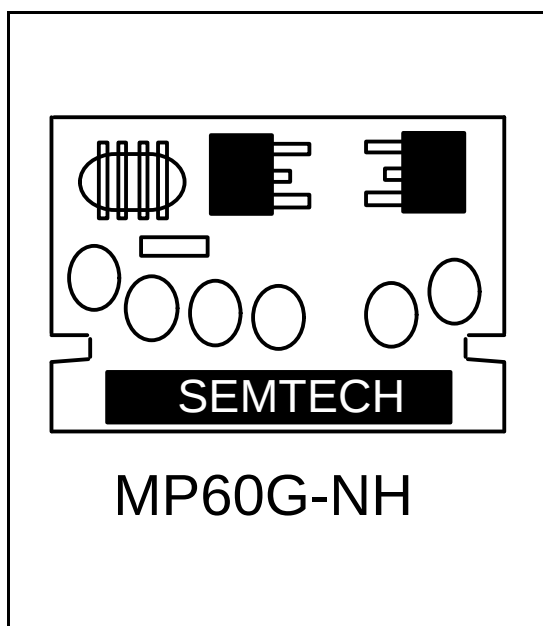
### APPLICATIONS

- Intel Pentium® II Power Supply
- Deschutes Power Supply
- Deschutes Memory Power Supply

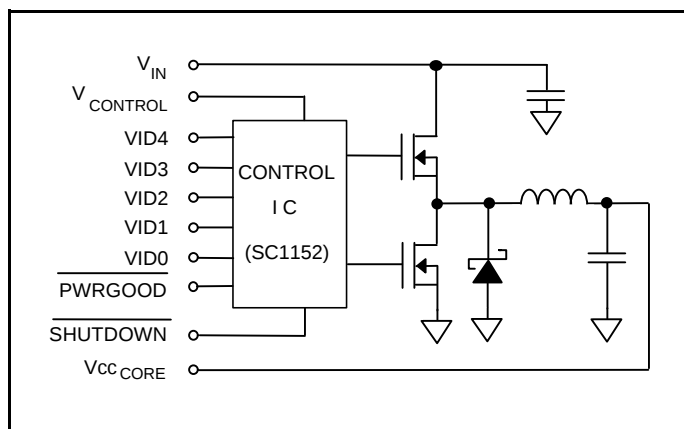
### ORDERING INFORMATION

| DEVICE     | V <sub>CONTROL</sub> | V <sub>IN</sub> | OVP |
|------------|----------------------|-----------------|-----|
| MP60G-5N   | 12V                  | 5V              | No  |
| MP60G-5P   | 12V                  | 5V              | Yes |
| MP60G-12N  | 12V                  | 12V             | No  |
| MP60G-12P  | 12V                  | 12V             | Yes |
| MP60G-12AN | 12V                  | 12 or 5V        | No  |
| MP60G-12AP | 12V                  | 12 or 5V        | Yes |
| MP60G-NH   | 12V                  | 5V              | No  |

### MODULE DIAGRAM



### SIMPLIFIED BLOCK DIAGRAM



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### ELECTRICAL CHARACTERISTICS

Conditions:  $V_O = V_{ID}$ ,  $V_{IN} = 4.75 - 12.6V$ ,  $I_O = 10A$ , unless otherwise stated.

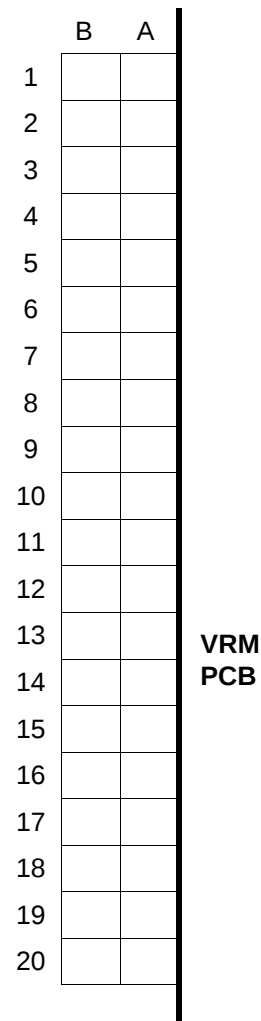
| PARAMETER                           | SYMBOL   | MIN            | TYP   | MAX           | UNITS             |
|-------------------------------------|----------|----------------|-------|---------------|-------------------|
| Output Voltage                      | $V_O$    | $0.95IV_{OI}$  | $V_O$ | $1.05IV_{OI}$ | V                 |
| Output Current MP60G-NH, 5X         | $I_O$    | 0.3            |       | 15            | A                 |
| Output Current MP60G-12X, 12AX      | $I_O$    | 0.3            |       | 15            | A                 |
| Current Surge Limit MP60G-NH, 5X    | $I_S$    | 15.5           |       |               | A                 |
| Current Surge Limit MP60G-12X, 12AX | $I_S$    | 15.5           |       |               | A                 |
| Output Over Voltage Protection      | OVP      | Setpoint + 20% |       |               | V                 |
| Output Slew Rate                    |          | 30             |       |               | A/ $\mu$ s        |
| Quiescent Current                   | $I_Q$    |                | 15    |               | mA                |
| Temperature Coefficient             | $T_C$    |                | TBD   |               | %/ $^{\circ}C$    |
| Temperature Stability               | $T_S$    |                | TBD   |               | %                 |
| Operating Efficiency (full load)    | $\eta$   |                | 85    |               | %                 |
| Switching Frequency                 | $f_{SW}$ |                | 200   |               | kHz               |
| DC Output Ripple Voltage            |          |                |       | 50            | mV <sub>p-p</sub> |
| Operating Temperature Range         | $T_J$    | 0              |       | 70            | $^{\circ}C$       |

| VOLTAGE IDENTIFICATION CODE |      |      |      |      |                 |
|-----------------------------|------|------|------|------|-----------------|
| Input Pins                  |      |      |      |      | $V_{CC_{CORE}}$ |
| VID4                        | VID3 | VID2 | VID1 | VID0 | (VDC)           |
| 0                           | 0    | 1    | 0    | 1    | 1.80            |
| 0                           | 0    | 1    | 0    | 0    | 1.85            |
| 0                           | 0    | 0    | 1    | 1    | 1.90            |
| 0                           | 0    | 0    | 1    | 0    | 1.95            |
| 0                           | 0    | 0    | 0    | 1    | 2.00            |
| 0                           | 0    | 0    | 0    | 0    | 2.05            |
| 1                           | 1    | 1    | 1    | 1    | 2.0             |
| 1                           | 1    | 1    | 1    | 0    | 2.1             |
| 1                           | 1    | 1    | 0    | 1    | 2.2             |
| 1                           | 1    | 1    | 0    | 0    | 2.3             |
| 1                           | 1    | 0    | 1    | 1    | 2.4             |
| 1                           | 1    | 0    | 1    | 0    | 2.5             |
| 1                           | 1    | 0    | 0    | 1    | 2.6             |
| 1                           | 1    | 0    | 0    | 0    | 2.7             |
| 1                           | 0    | 1    | 1    | 1    | 2.8             |
| 1                           | 0    | 1    | 1    | 0    | 2.9             |
| 1                           | 0    | 1    | 0    | 1    | 3.0             |
| 1                           | 0    | 1    | 0    | 0    | 3.1             |
| 1                           | 0    | 0    | 1    | 1    | 3.2             |
| 1                           | 0    | 0    | 1    | 0    | 3.3             |
| 1                           | 0    | 0    | 0    | 1    | 3.4             |
| 1                           | 0    | 0    | 0    | 0    | 3.5             |

0 = processor pin connected to  $V_{SS}$ , 1 = open

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| INPUT AND OUTPUT CONNECTIONS |                                 |                                 |         |
|------------------------------|---------------------------------|---------------------------------|---------|
| Pin No.                      | Row A                           | Row B                           | Pin No. |
| 1                            | 5V in                           | 5V in                           | 1       |
| 2                            | 5V in                           | 5V in                           | 2       |
| 3                            | 5V in                           | Reserved                        | 3       |
| 4                            | 12V in                          | 12V in                          | 4       |
| 5                            | Reserved                        | Reserved                        | 5       |
| 6                            | Reserved                        | OUTEN                           | 6       |
| 7                            | VID0                            | VID1                            | 7       |
| 8                            | VID2                            | VID3                            | 8       |
| 9                            | VID4                            | PWRGD                           | 9       |
| 10                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 10      |
| 11                           | V <sub>SS</sub>                 | V <sub>CC</sub> <sub>CORE</sub> | 11      |
| 12                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 12      |
| 13                           | V <sub>SS</sub>                 | V <sub>CC</sub> <sub>CORE</sub> | 13      |
| 14                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 14      |
| 15                           | V <sub>SS</sub>                 | V <sub>CC</sub> <sub>CORE</sub> | 15      |
| 16                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 16      |
| 17                           | V <sub>SS</sub>                 | V <sub>CC</sub> <sub>CORE</sub> | 17      |
| 18                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 18      |
| 19                           | V <sub>SS</sub>                 | V <sub>CC</sub> <sub>CORE</sub> | 19      |
| 20                           | V <sub>CC</sub> <sub>CORE</sub> | V <sub>SS</sub>                 | 20      |



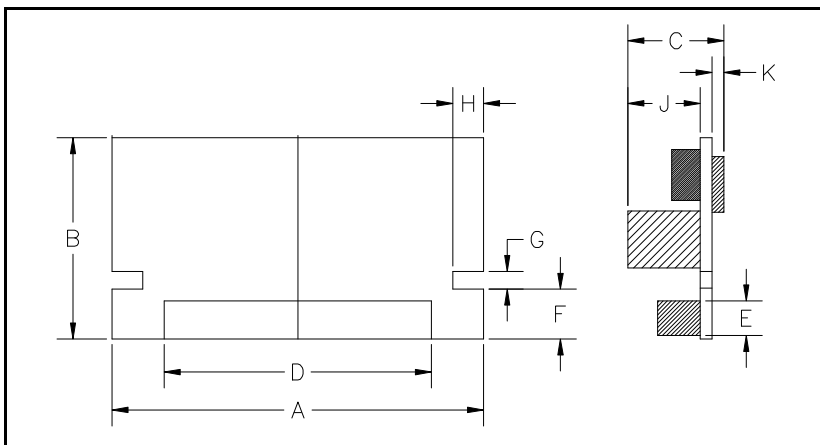
End view of VRM connector  
(viewed from motherboard side)

### VOLTAGE REGULATOR MODULE CONNECTOR PIN REFERENCE

| Pin Name                        | Pin Function                                                                                                                                                                                                                                                                |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PWRGD                           | <b>Power Good:</b> When the output voltage is not within specifications (nominal or selected voltage $\pm 7\%$ ) this signal will be in the low state. The PWRGD signal will change to the proper state within 5ms of the output coming into or going out of specification. |
| OUTEN                           | <b>Output Enable:</b> A low state disables the output voltage. When disabled, the PWRGD signal shall be in the low state.                                                                                                                                                   |
| V <sub>CC</sub> <sub>CORE</sub> | Microprocessor core voltage programmed with VID inputs                                                                                                                                                                                                                      |
| V <sub>SS</sub>                 | System Ground                                                                                                                                                                                                                                                               |
| VID[0:4]                        | <b>Voltage Identification:</b> The module will accept five open collector signals, used to indicate the voltage required by the processor, as defined by Intel                                                                                                              |
| 5V in                           | Main power input for regulation.                                                                                                                                                                                                                                            |
| 12V in                          | Must also be connected (input for control circuits only)                                                                                                                                                                                                                    |

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### MECHANICAL DIMENSIONS



Component size and  
location for illustration only

| Dimension | mm           | inch         |     |
|-----------|--------------|--------------|-----|
| A         | 79.7         | 3.14         | Max |
| B         | 38.1         | 1.50         | Max |
| C         | 24.4         | 0.96         | Max |
| D         | 57.4         | 2.26         | Typ |
| E         | 8.13         | 0.32         | Typ |
| F         | 10.67 ± 0.13 | 0.42 ± 0.005 | Typ |
| G         | 3.81         | 0.15         | Typ |
| H         | 6.50         | 0.26         | Min |
| J         | 21.6         | 0.85         | Max |
| K         | 3.6          | 0.14         | Max |