MP6508A

2.7V to 18V, 1.2A, Bipolar Stepper Motor Driver in a QFN-16 (3mmx3mm) Package

DESCRIPTION

The MP6508A is a bipolar stepper motor driver with dual, built-in full-bridges consisting of N-channel power MOSFETs. The device operates across a 2.7V to 18V input voltage (V_{IN}) range and can deliver a motor current up to 1.2A per channel.

Internal safety features include over-current protection (OCP), under-voltage lockout protection (UVLO), and thermal shutdown. The MP6508A provides a fault output flag to indicate OCP and thermal shutdown.

The MP6508A is available in a QFN-16 (3mmx3mm) package with an exposed thermal pad on the backside.

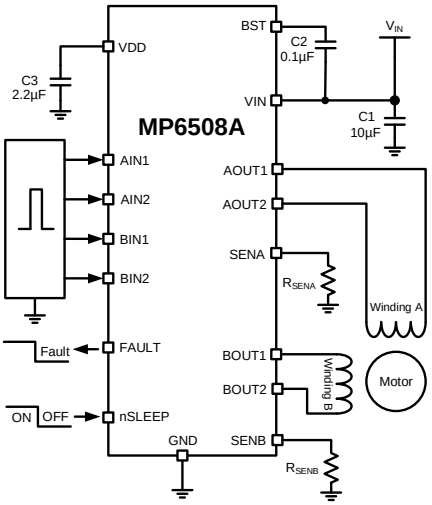
FEATURES

- Wide 2.7V to 18V Input Voltage (V_{IN}) Range
- Two Internal Full-Bridge Drivers
- Low On Resistance ($R_{DS(ON)}$): 250mΩ High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)
- Internal Charger Pump for the High-Side (HS) Driver
- Low 1.6mA Quiescent Current (I_Q)
- Low 1µA Sleep Current
- Over-Current Protection (OCP)
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package
- Available in a QFN-16 (3mmx3mm) Package

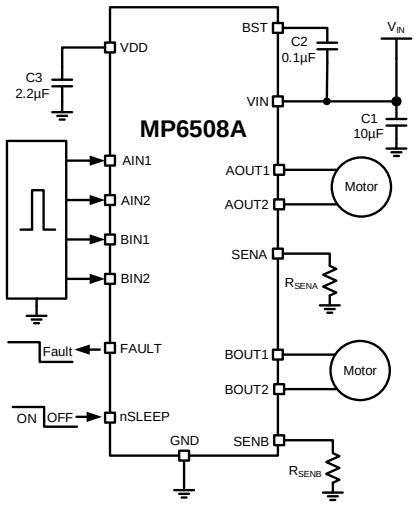
APPLICATIONS

- Point-of-Sale (POS) Printers
- Video Security Cameras
- Digital Still Cameras
- Battery-Powered Toys

TYPICAL APPLICATION



Typical Application (Stepper Motor)



Typical Application (Dual DC Motor)

ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6508AGQ*	QFN-16 (3mmx3mm)	*See Below*	1

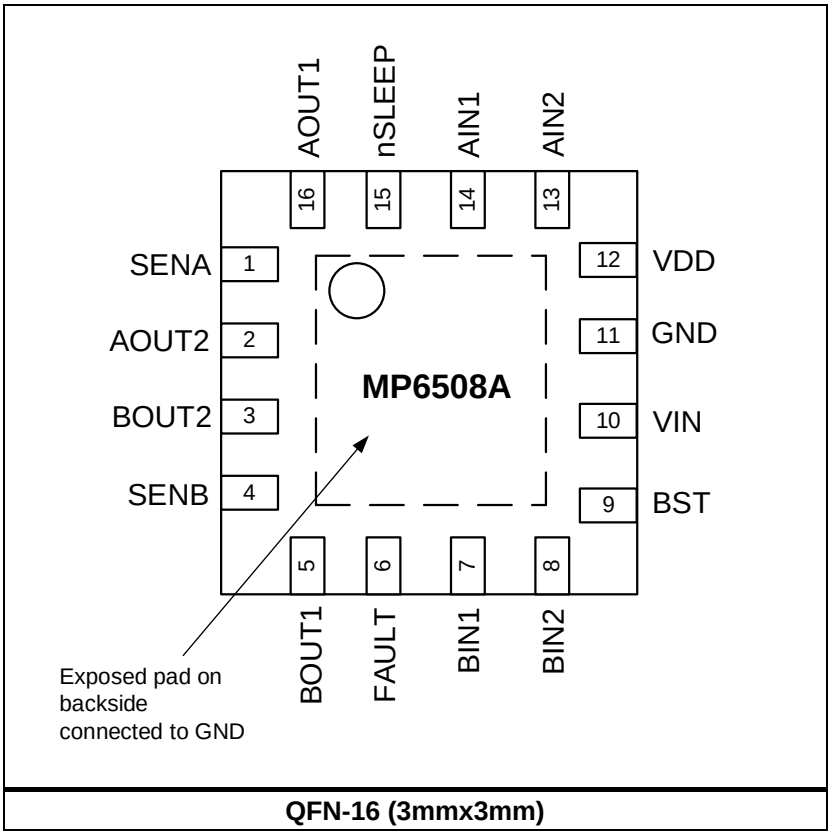
* For Tape & Reel, add suffix -Z (e.g. MP6508AGQ-Z).

TOP MARKING

BXHY
LLLL

BXH: Product code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SENA	**Channel A sense input.** Connect the SENA pin to the current-sense resistor for channel A.
2	AOUT2	**Bridge A output terminal 2.** Connect the AOUT2 pin to motor winding A.
3	BOUT2	**Bridge B output terminal 2.** Connect the BOUT2 pin to motor winding B.
4	SENB	**Channel B sense input.** Connect the SENB pin to the current-sense resistor for channel B.
5	BOUT1	**Bridge B output terminal 1.** Connect the BOUT1 pin to motor winding B.
6	FAULT	**Fault indication.** Pull the FAULT pin logic low if an over-temperature (OT) fault is detected.
7	BIN1	**Gate signal input to control BOUT1.**
8	BIN2	**Gate signal input to control BOUT2.**
9	BST	**Charge pump output.** Connect a 10nF to 100nF ceramic capacitor between the BST and VIN pins.
10	VIN	**Power supply input.** The input voltage (V_{IN}) ranges between 2.7V and 18V.
11	GND	**Ground.**
12	VDD	**Internal control and logic supply voltage.**
13	AIN2	**Gate signal input to control AOUT2.**
14	AIN1	**Gate signal input to control AOUT1.**
15	nSLEEP	**Sleep logic input.** Pull the nSLEEP pin logic low to enter sleep mode; pull nSLEEP logic high to enable the device.
16	AOUT1	**Bridge A output terminal 1.** Connect the AOUT1 pin to motor winding A.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +20V
AOUTx voltage (V_{AOUTx}) .....-0.3V to V_{IN} + 1V
BOUTx voltage (V_{BOUTx}) .....-0.3V to V_{IN} + 1V
BST voltage (V_{BST}) .....-0.3V to V_{IN} + 6.5V
Sense voltage (V_{SENx}) .....-0.3V to +0.5V
All other pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-16 (3mmx3mm) 2.5W
Operating temperature..... -40°C to +85°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM).....±750V

Recommended Operating Conditions (3)

V_{IN}.....2.7V to 18V
Output current (I_{AOUT}, I_{BOUT})..... 1.2A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-16 (3mmx3mm) .....50 ..... 12 ... °C/W

Notes:

8) Exceeding these ratings may damage the device.
9) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
10) The device is not guaranteed to function outside of its operating conditions.
11) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 9V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		2.7		18	V
VDD voltage	V_{DD}			4.85		V
Quiescent current	I_{IN}	nSLEEP = 1, I_{OUT} = 0A, output disabled		1.6	1.8	mA
	I_{IN_SLEEP}	nSLEEP = 0, V_{IN} = 9V			1	µA
Integrated MOSFETs						
Output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 500mA, V_{IN} = 9V, T_J = 25°C		250	350	mΩ
		I_{OUT} = 500mA, V_{IN} = 2.7V, T_J = 25°C		310	400	mΩ
		I_{OUT} = 500mA, V_{IN} = 9V, T_J = 85°C (5)		350		mΩ
		I_{OUT} = 500mA, V_{IN} = 2.7V, T_J = 85°C (5)		400		mΩ
	$R_{DS(ON)\_LS}$	I_{OUT} = 500mA, V_{IN} = 9V, T_J = 25°C		235	350	mΩ
		I_{OUT} = 500mA, V_{IN} = 2.7V, T_J = 25°C		310	400	mΩ
		I_{OUT} = 500mA, V_{IN} = 9V, T_J = 85°C (5)		310		mΩ
		I_{OUT} = 500mA, V_{IN} = 2.7V, T_J = 85°C (5)		400		mΩ
Body diode forward voltage	V_F	I_{OUT} = 500mA			1	V
Control Logic						
Under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$				2.5	V
UVLO hysteresis	V_{UVLO_HYS}		30	75	120	mV
Logic-low input threshold	V_{IL}				0.6	V
Logic-high input threshold	V_{IH}		2			V
nSLEEP logic low voltage	V_{SLEEP_L}				0.4	V
nSLEEP logic high voltage	V_{SLEEP_H}		2			V
Fault output logic low	V_{FAULT_L}	Flag triggered by OTP, 1mA current			200	mV
Fault output leakage current	I_{LEAK_FAULT}	V_{FAULT} = 5V			1	µA
Constant off time	t_{OFF}		21	26	31	µs
Propagation delay on time	$t_{ON\_DELAY\_HS}$	10mA source current	80	200	300	ns
	$t_{ON\_DELAY\_LS}$		10	55	90	ns
Propagation delay off time	$t_{OFF\_DELAY\_HS}$		110	180	225	ns
	$t_{OFF\_DELAY\_LS}$		40	130	180	ns

Note:

12) Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 9V, T_A = 25°C, unless otherwise noted.

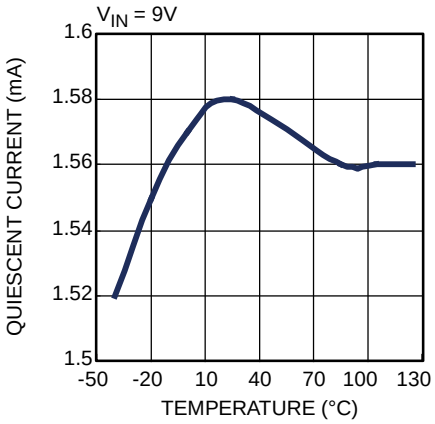
Parameter	Symbol	Condition	Min	Typ	Max	Units
Cross-over delay	t_{CROSS}	Low-side MOSFET (LS-FET) off to high-side MOSFET(HS-FET) on for one bridge arm (Bridge A or Bridge B)	350	450	550	ns
		HS-FET off to LS-FET on for one bridge arm (Bridge A or Bridge B)	250	355	435	ns
Sleep mode wakeup time	t_{WAKE}	Sleep mode (active high) to full bridge on (V_{BST} = 100nF)	0.65	0.75	0.9	ms
Protection Circuitry						
Current limit sense trip voltage	V_{REF}		175	204	233	mV
Blanking time	t_{BLANK}		2	2.5	3	µs
Over-current (OC) trip threshold	I_{OCP1}	HS-FET	2.2	3.4	4.6	A
	I_{OCP2}	LS-FET	1.8	2.4	3	A
OC deglitch time	t_{DEG}		0.75	1.1	1.45	µs
Over-current protection (OCP) period	t_{OCP}		1.3	1.8	2.3	ms
Thermal shutdown (6)				165		°C
Thermal shutdown hysteresis (6)				15		°C

Note:

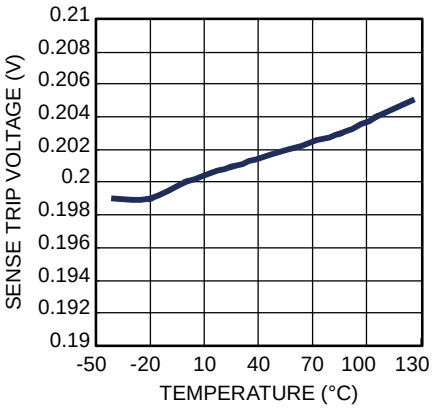
13) Not tested in production.

TYPICAL CHARACTERISTICS

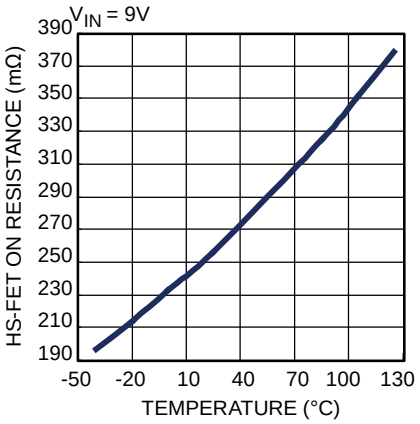
Quiescent Current vs. Temperature



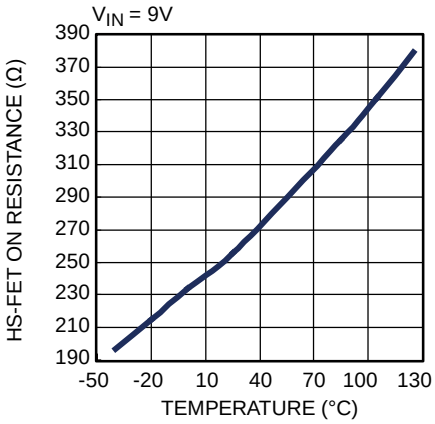
Sense Trip Voltage vs. Temperature



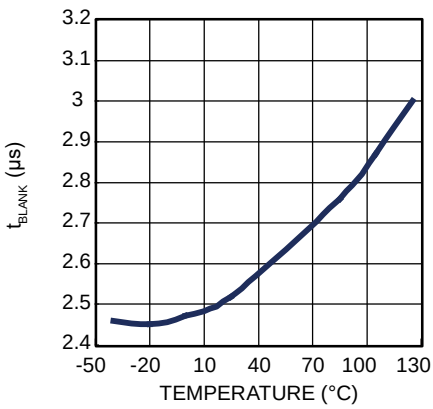
Bridge A HS-FET On Resistance vs. Temperature



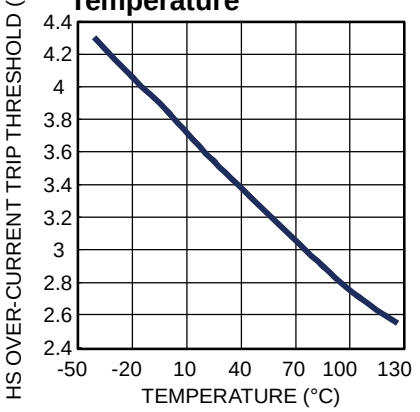
Bridge B HS-FET On Resistance vs. Temperature



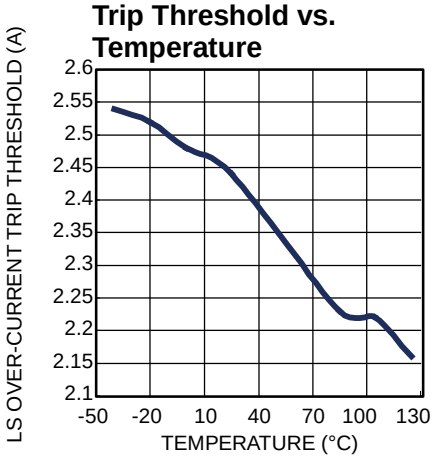
Blanking Time vs. Temperature



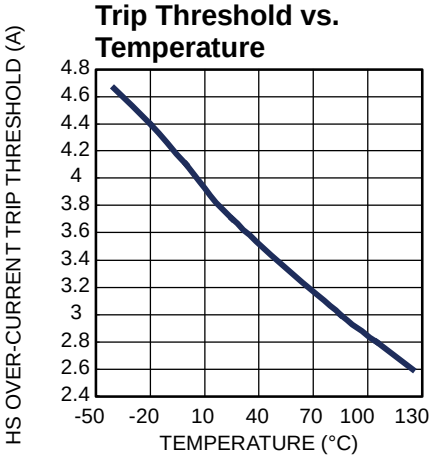
Bridge A HS Over-Current Trip Threshold vs. Temperature



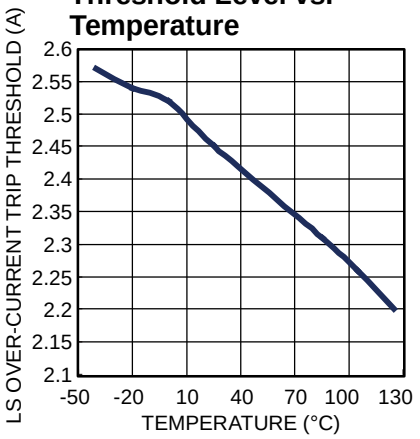
Bridge A LS Over-Current Trip Threshold vs. Temperature



Bridge B HS Over-Current Trip Threshold vs. Temperature



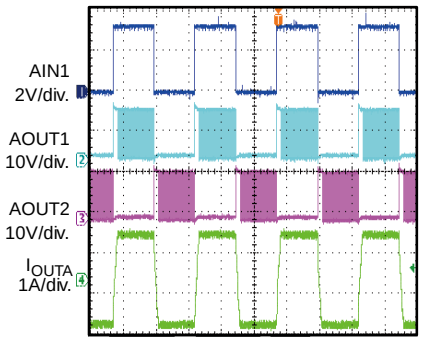
Bridge B LS Over-Current Threshold Level vs. Temperature



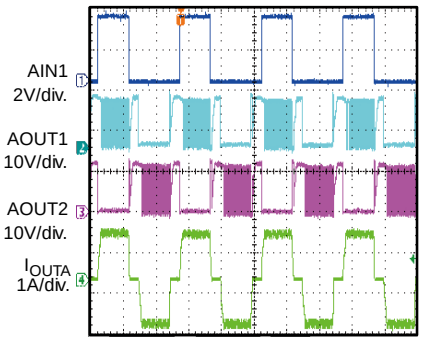
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 12. V_{IN} = 12V, I_{OUT} = 1.2A, f_{STEP} = 200Hz, R + L load: L = 2mH, R = 3.3Ω, T_A = 25°C, unless otherwise noted.

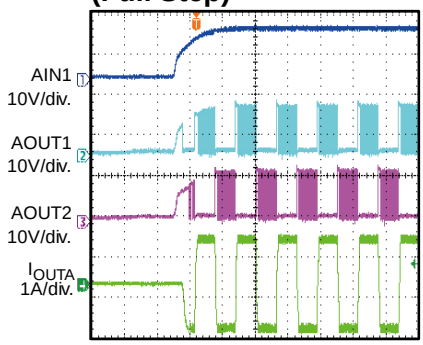
Steady State (Full Step)



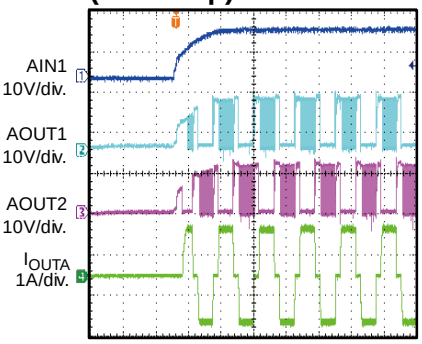
Steady State (Half-Step)



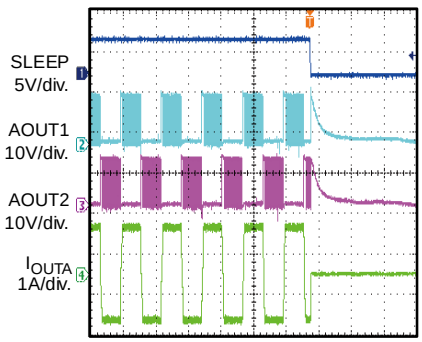
Power Ramping Up (Full Step)



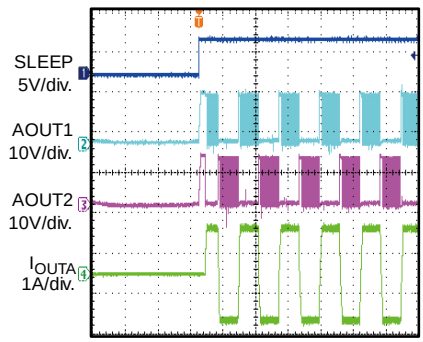
Power Ramping Up (Half-Step)



Sleep Entry (Full Step)



Sleep Recovery (Full Step)



FUNCTIONAL BLOCK DIAGRAM

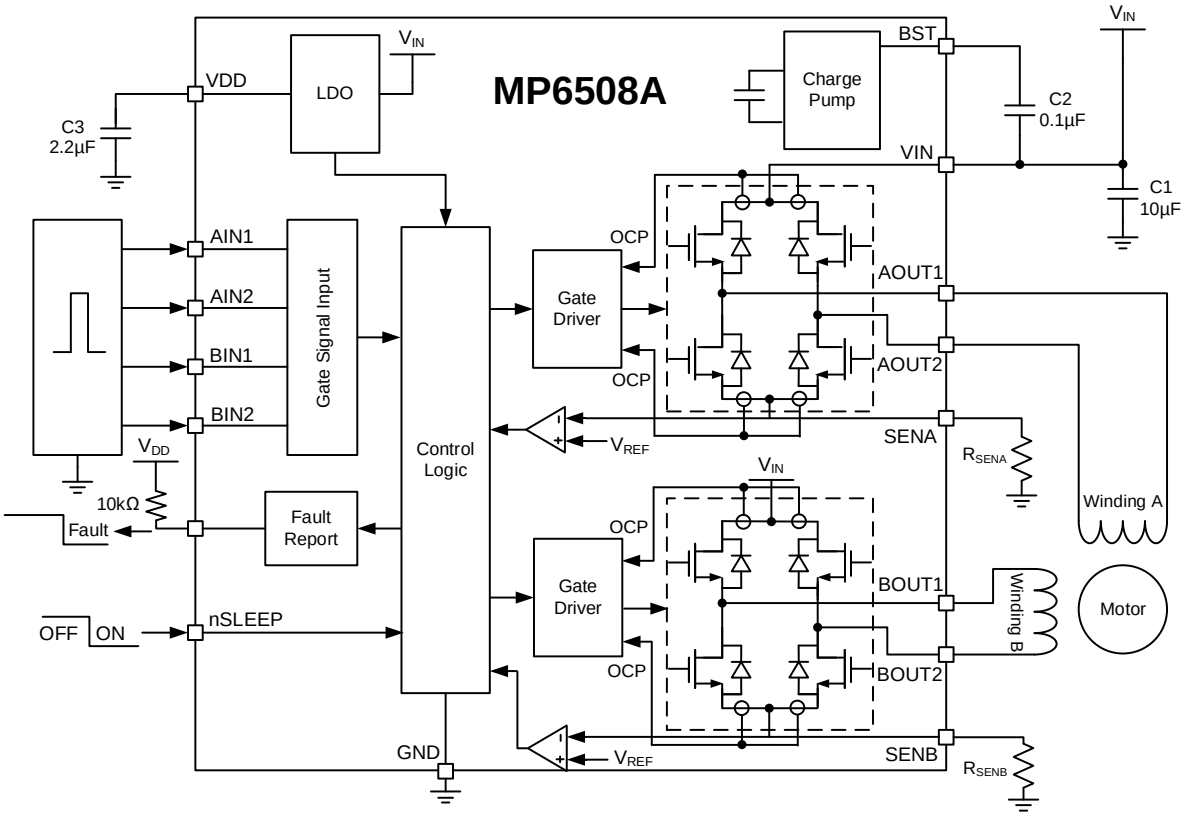


Figure 1: Functional Block Diagram

OPERATION

The MP6508A is a stepper motor driver that integrates eight N-channel power MOSFETs connected as two, internal full-bridges. The device can deliver an output current (I_{OUT}) up to 1.2A across a 2.7V to 18V input voltage (V_{IN}) range. It can drive a stepper motor or two DC motors.

The MP6508A's I_{OUT} can be controlled by either an external or internal pulse-width modulation (PWM) current controller. Fault protections include over-current protection (OCP), under-voltage lockout (UVLO), and over-temperature protection (OTP). The device also provides low-power sleep mode.

External Pulse-Width Modulation (PWM) Current Control

For external PWM current control, I_{OUT} can be regulated by applying external PWM signals on the input pins (AIN1, AIN2, BIN1, and BIN2). For phase A, AIN1 and AIN2 control the AOUT1 and AOUT2 states. Similarly, for phase B, BIN1 and BIN2 control the BOUT1 and BOUT2 states.

Figure 2 shows the input signal logic and bridge output states.

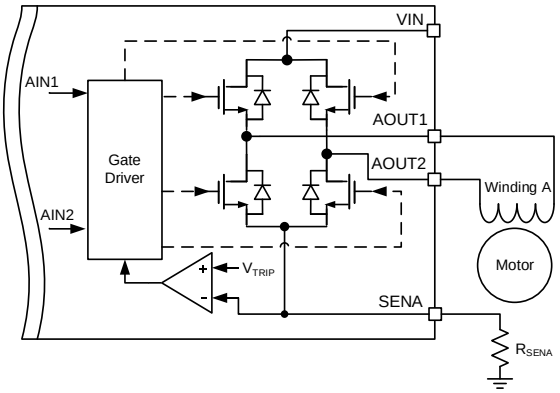


Figure 2: Full-Bridge Control Circuit

Table 1 shows the full-bridge gate logic.

Table 1: Full-Bridge Gate Logic

AIN1 and BIN1	AIN2 and BIN2	AOUT1 and BOUT1	AOUT2 and BOUT2
Low	Low	Hi-Z	Hi-Z
Low	High	GND	VIN
High	Low	VIN	GND
High	High	GND	GND

In external PWM control mode, the winding's inductor current (I_L) ramps up when the high-side MOSFET (HS-FET) is on and freewheels during the HS-FET's off time (t_{OFF}) to generate the recirculation current.

There are two modes for this recirculation current: slow decay and fast decay. Figure 3 shows the two modes for forward operation.

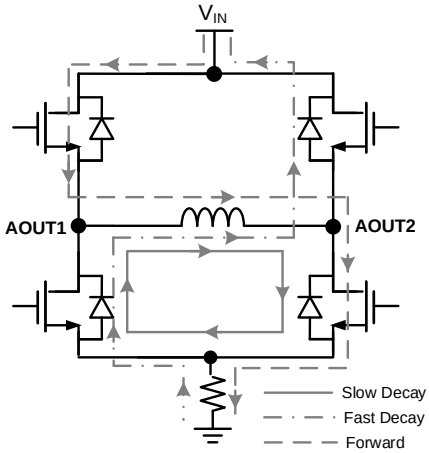


Figure 3: Forward Operation

Figure 4 shows slow decay and fast decay for reverse operation.

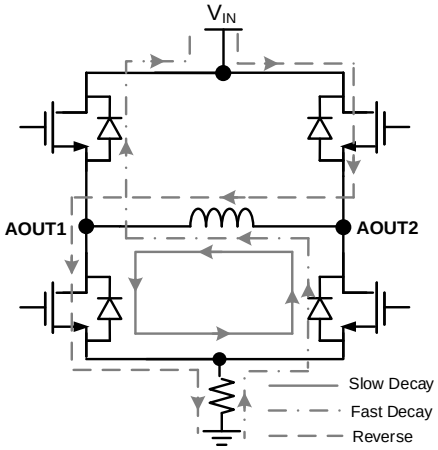


Figure 4: Reverse Operation

In slow decay mode, the current circulates through the two low-side MOSFETs (LS-FETs). In fast decay mode, the current flows through the body diodes of the other two diagonal MOSFETs.

To configure the MP6508A for fast decay mode, apply the PWM signal to one input pin and keep

the other input pin low. To configure the device for slow decay mode, apply the PWM signal to one input pin and keep the other input pin high. Table 2 shows the configuration for PWM control.

Table 2: PWM Control

AIN1 and BIN1	AIN2 and BIN2	Mode
High (PWM)	Low	Forward
Low (PWM)	Low	Fast decay
Low	High (PWM)	Reverse
Low	Low (PWM)	Fast decay
High	Low (PWM)	Forward
High	High (PWM)	Slow decay
Low (PWM)	High	Reverse
High (PWM)	High	Slow decay

Figure 5 shows the external PWM current control waveform.

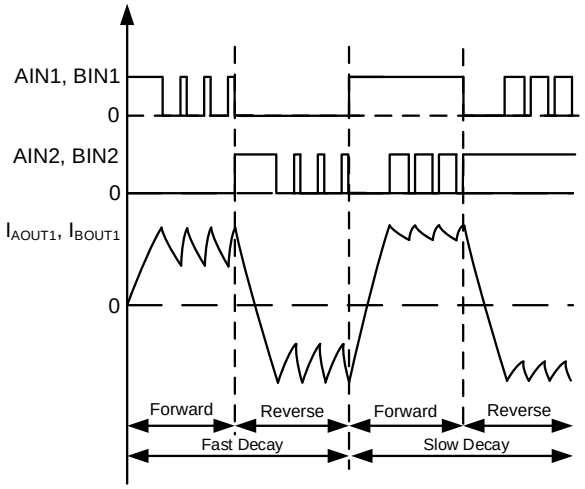


Figure 5: External PWM Current Control Waveform

Internal Pulse-Width Modulation (PWM) Current Control

For internal PWM current control, I_{OUT} is regulated by an internal, constant off-time PWM current control circuit, described below:

1. A diagonal pair of MOSFETs turns on to enable current to flow through the motor winding.
2. The current increases in the motor winding, which is sensed by an external sense resistor (R_{SENSE}). During the initial blanking time (t_{BLANK}) (3µs), the HS-FET always turns on despite the current limit detection.
3. When the voltage across R_{SENSE} reaches the internal reference voltage threshold (V_{TRIP}) (200mV), the internal current comparator shuts off the HS-FET.
4. The stepper motor's inductance causes the current to freewheel through the two LS-FETs (slow decay).
5. During this freewheeling time, the current decreases until the internal clock reaches its constant t_{OFF} (typically 30µs). After that, the HS-FET is enabled to increase the winding current again.
6. This cycle continues to repeat.

The current limit (I_{LIMIT}) can be calculated with Equation (1):

$$I_{LIMIT}\,(A) = \frac{V_{REF}\,(V)}{R_{SENSE}\,(\Omega)} \quad (1)$$

Figure 6 shows the internal PWM current control waveform.

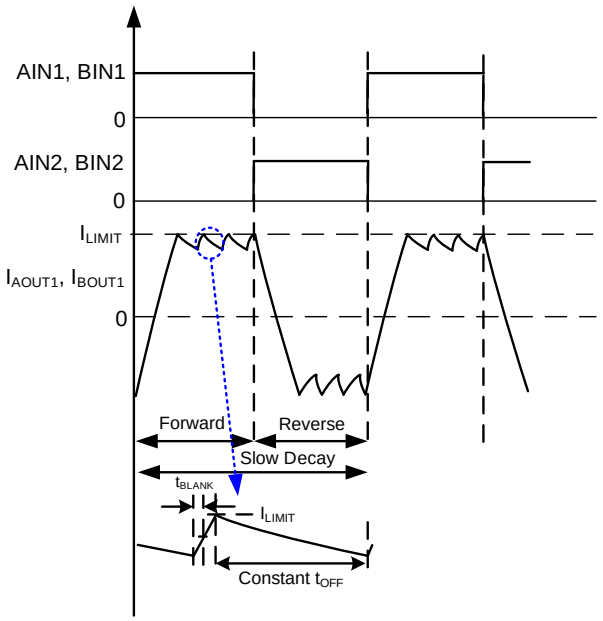


Figure 6: Internal PWM Current Control Waveform

Sleep Mode

The MP6508A provides low-power standby sleep mode. Pull the nSLEEP pin logic low to enable low-power sleep mode. In this state, the two full-bridges are disabled and the internal circuits such as the gate drive, internal regulator, and charge pump all shut down. Pull nSLEEP logic high to wake up the MP6508A from sleep mode. Approximately 1ms must pass before the internal circuitry stabilizes.

Blanking Time

A current spike typically occurs during the switching transition due to the body diode's reverse-recovery current, or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the HS-FET. An internal t_{BLANK} blanks the current-sense comparator's output when the outputs are switched, which is also the HS-FET's minimum on time (t_{ON}).

Enable

If all the inputs (AIN1, AIN2, BIN1, and BIN2) are logic low, the MP6508A's outputs are disabled while the charger pump and internal regulator remain active.

Synchronous Rectifier (SR) Mode

The MP6508A enters synchronous rectifier (SR) mode during the constant t_{OFF} when I_{OUT} exceeds the current limit threshold, and the load current freewheels in slow decay SR mode. In slow decay mode, the current freewheels through one LS-FET and the other LS-FET's body diode to short the winding. SR mode enables both LS-FETs, which provide a lower voltage drop and power dissipation during decay operation.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through the FET by disabling the gate driver. If the over-current (OC) limit threshold is reached and lasts for longer than the OC deglitch time, all the MOSFETs in the H-bridge are disabled and the nFAULT pin is pulled low. The driver remains disabled and is enabled again after 2ms (typically). Note that only the H-bridge in which OCP is detected is disabled while the other bridge continues to operate normally.

OC conditions on both the HS-FET and LS-FET (e.g. a short to ground, supply, or across the motor winding) all result in an OC shutdown. Note that OCP does not use the current-sense circuitry used for PWM current control and is independent of the sense resistance or V_{REF}.

Thermal Shutdown

The IC's junction temperature (T_J) is internally monitored. If T_J exceeds the thermal shutdown threshold (typically 165ºC), the converter shuts down and the FAULT pin goes low. Once T_J drops to about 150ºC (15ºC hysteresis), the converter recovers.

Under-Voltage Lockout (UVLO) Protection

The MP6508A provides UVLO protection. If V_{IN} exceeds the UVLO rising threshold ($V_{IN\_UVLO\_R}$), the MP6508A starts up. The device shuts off once V_{IN} drops below the UVLO falling threshold.

APPLICATION INFORMATION

Driver Mode

The MP6508A can be configured for full-step mode and half-step mode by energizing the two windings sequentially.

The full-step drive energizes two winding phases at any given time. Table 3 shows the full-step sequence in which the stator windings are energized.

Table 3: Full-Step Drive Sequence (8)

Sequence (Full Step)	1	2	3	4
A	+	N/A	N/A	+
B	+	+	N/A	N/A
$\overline{A}$	N/A	+	+	N/A
$\overline{B}$	N/A	N/A	+	+

There are a total of four steps in one cycle of the full-step drive sequence: AB→$\overline{A}$B→$\overline{A}$ $\overline{B}$→A $\overline{B}$. (7)

Table 4 shows the half-step sequence in which the stator windings are energized.

Table 4: Half-Step Drive Sequence (8)

Sequence (Half-Step)	1	2	3	4	5	6	7	8
A	+	N/A	N/A	N/A	N/A	N/A	+	+
B	+	+	+	N/A	N/A	N/A	N/A	N/A
$\overline{A}$	N/A	N/A	+	+	+	N/A	N/A	N/A
$\overline{B}$	N/A	N/A	N/A	N/A	+	+	+	N/A

There are a total of eight steps in one cycle of the half-step drive sequence: AB→B→$\overline{A}$B→$\overline{A}$ →$\overline{A}$ $\overline{B}$→$\overline{B}$→A$\overline{B}$→A.

Notes:

7) A means +VIN between AOUT1 and AOUT2 for winding A, while $\overline{A}$ means -VIN between AOUT1 and AOUT2. The same applies to winding B.

8) "+" is the selected winding voltage.

Figure 7 shows the operating waveforms for both full-step and half-step drives.

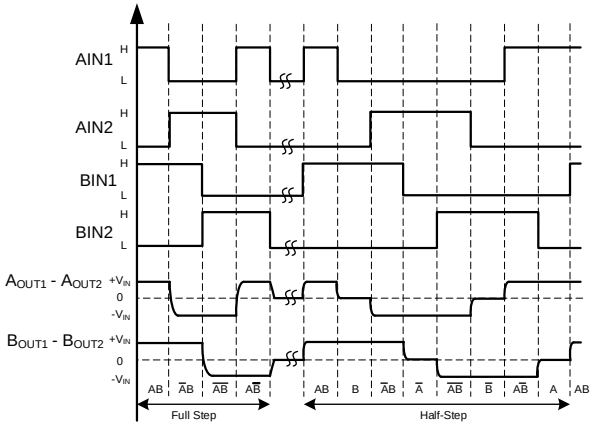


Figure 7: Signal Logic Sequences for the Full-Step and Half-Step Drives

Design Example

Table 5 shows the specifications for a design example based on the application guidelines.

Table 5: Design Example

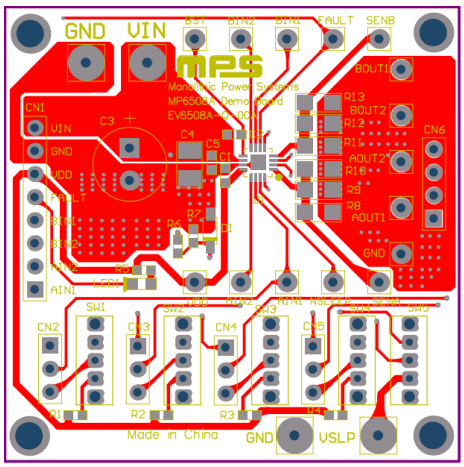
V_{IN}	I_{OUT}
2.7V to 18V	1.2A

For the detailed application schematic, see Figure 9 on page 14. See the Typical Performance Characteristics section on page 7 for the typical performance and circuit waveforms. Refer to the related EV6508A-Q-00A datasheet for more details on applications.

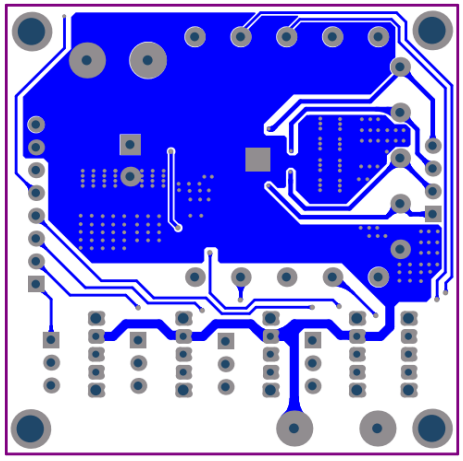
PCB Layout Guidelines

Efficient PCB layout using a heavy ground plane is critical for stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. Solder the MP6508A directly on the board to improve electrical and thermal performance.
2. Place the sense resistors as close as possible to the MP6508A for accurate current detection.
3. Use an exposed pad to provides a path for enhanced thermal dissipation.
4. Solder the thermal pad directly to the copper on the PCB.
5. Use thermal vias to transfer heat to the other layers of the PCB.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

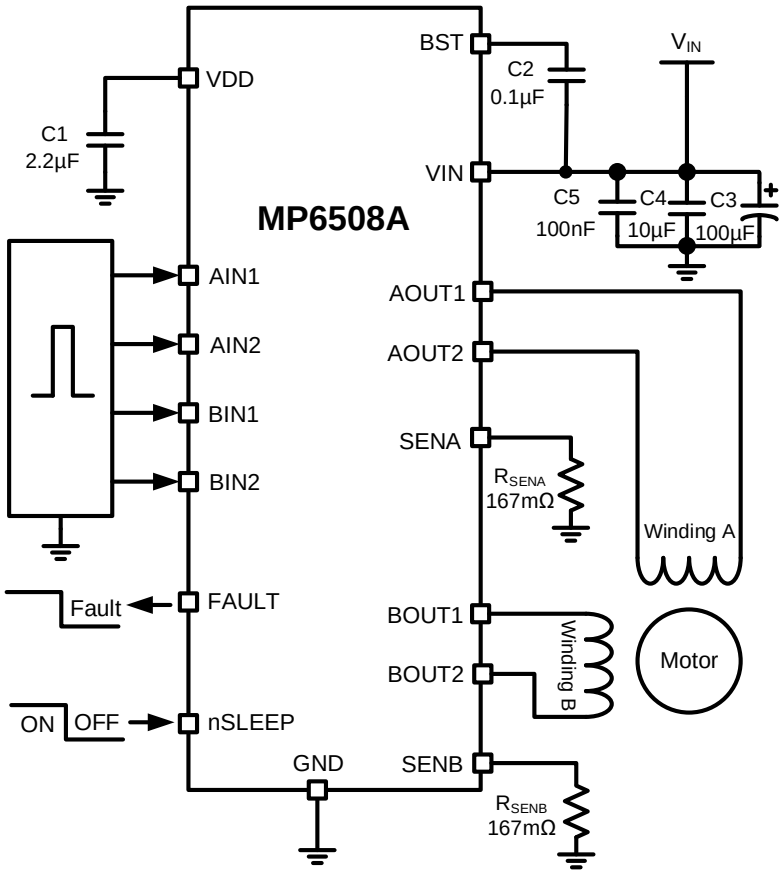
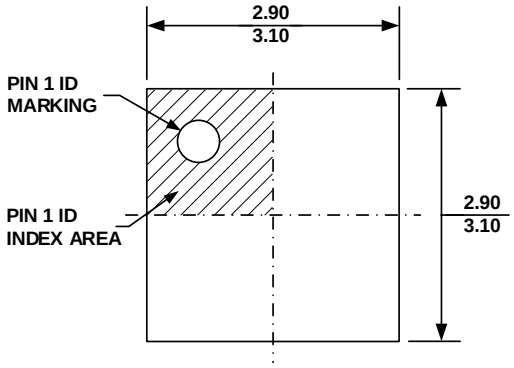


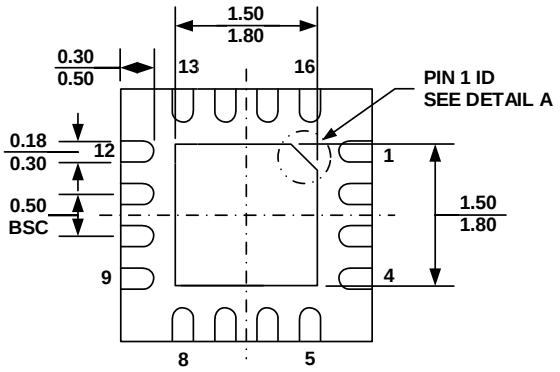
Figure 9: Typical Application Circuit

PACKAGE INFORMATION

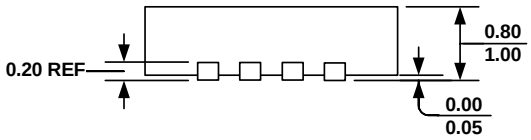
QFN-16 (3mmx3mm)



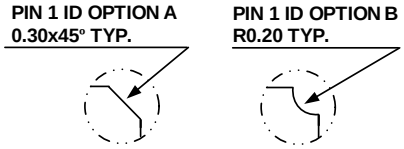
TOP VIEW



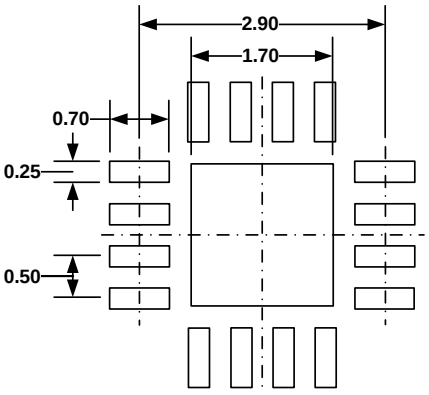
BOTTOM VIEW



SIDE VIEW



DETAIL A

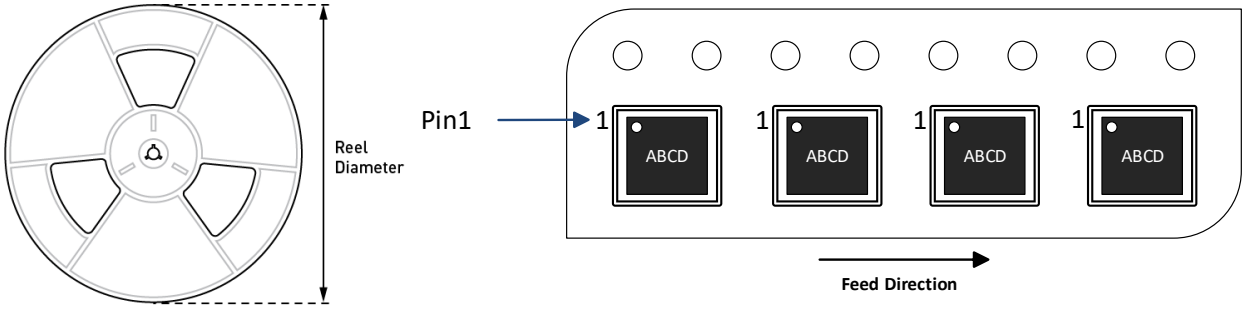


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VEED-4.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6508AGQ-Z	QFN-16 (3mmx3mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/12/2023	Initial Release	-