# MP6541, MP6541A

## 40V, 8A, Three-Phase Power Stage

## DESCRIPTION

The MP6541 and MP6541A are three-phase brushless DC (BLDC) motor drivers with three integrated half-bridges, consisting of six N-channel power MOSFETs. The MP6541 and MP6541A also integrate six pre-drivers, two gate drive power supplies, and three current-sense amplifiers.

The MP6541 integrates enable and pulse-width modulation (PWM) inputs for each half-bridge. The MP6541A integrates separate high-side (HS) and low-side (LS) inputs. Otherwise, the parts are identical. References to the MP6541 in this datasheet also apply to the MP6541A, unless otherwise noted.

The MP6541 can deliver up to 12A of peak output current ($I_{OUT}$) for 1 second, and 8A continuously (depending on thermal and PCB conditions). The device uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs (HS-FETs), and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6541 is available in a TQFN-26 (6mmx6mm) package.

## FEATURES

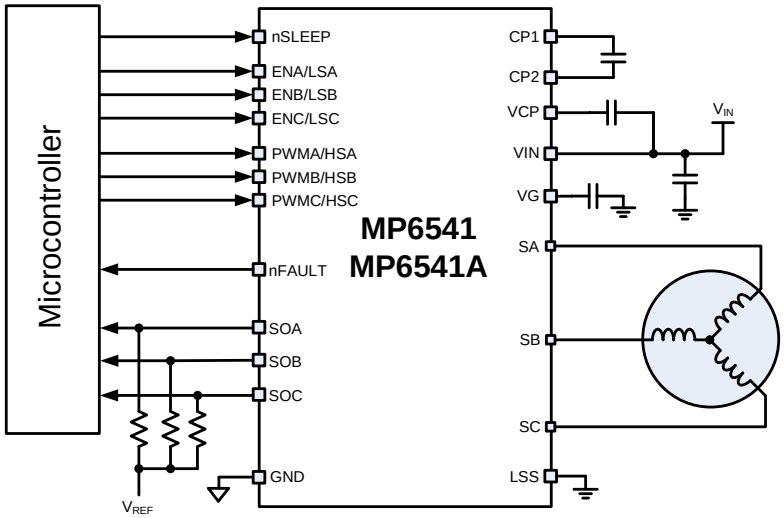
- 4.75V to 40V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- 8A Continuous Output Current ($I_{OUT}$)
- MOSFET On Resistance: 15mΩ per FET
- MP6541: PWM and ENBL Inputs
  MP6541A: High-Side (HS) and Low-Side (LS) Inputs
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)
- Thermal Shutdown Protection
- Over-Current Protection (OCP)
- Integrated Bidirectional Current-Sense Amplifiers
- Available in a TQFN-26 (6mmx6mm) Package

## APPLICATIONS

- Brushless DC (BLDC) Motor Drives
- Permanent Magnet Synchronous Motors (PMSMs)



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP6541GQKT* | TQFN-26 (6mmx6mm) | *See Below* | 1 |
| MP6541AGQKT** | TQFN-26 (6mmx6mm) | *See Below* | 1 |

* For Tape & Reel, add suffix -Z (e.g. MP6541GQKT-Z).

** For Tape & Reel, add suffix -Z (e.g. MP6541AGQKT-Z).

## TOP MARKING (MP6541GQKT)

MPSYYWW
MP6541
LLLLLLLLL

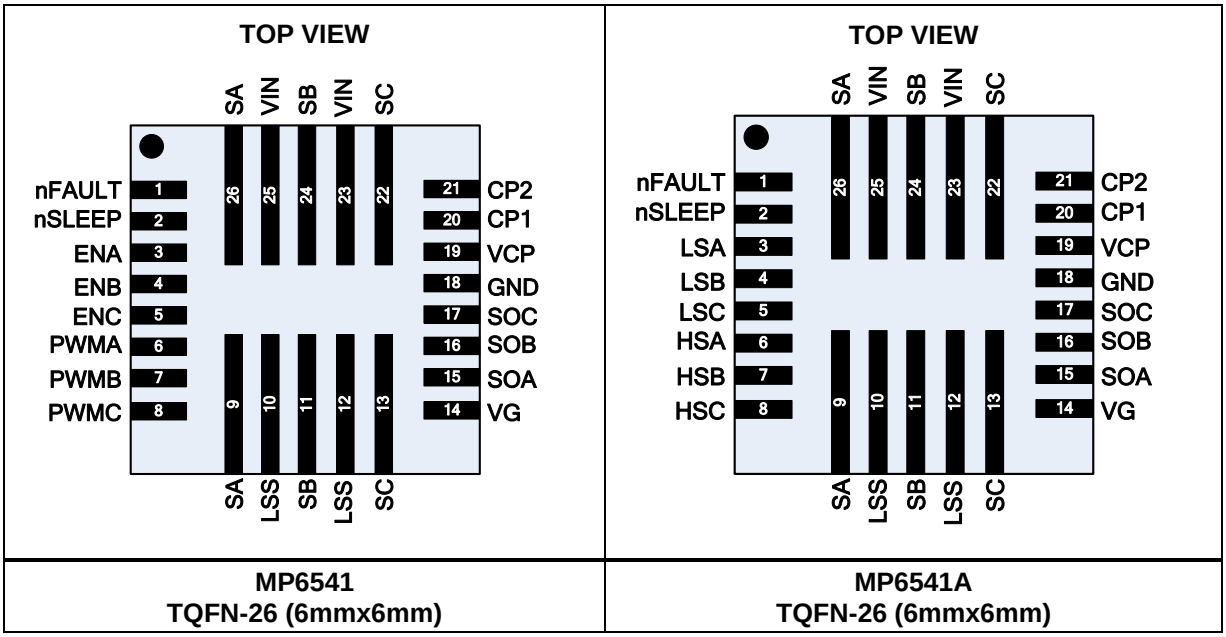
MPS: MPS prefix
YY: Year code
WW: Week code
MP6541: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP6541AGQKT)

MPSYYWW
MP6541A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6541A: Part number
LLLLLLLLL: Lot number

## PACKAGE REFERENCE




| MP6541<br>TQFN-26 (6mmx6mm) | MP6541A<br>TQFN-26 (6mmx6mm) |
|---|---|

## PIN FUNCTIONS

| Pin # | MP6541 | MP6541A | Description |
|---|---|---|---|
| 1 | nFAULT | | **Fault indication.** This pin is an open-drain output. nFAULT is pulled logic low if a fault occurs. |
| 2 | nSLEEP | | **Sleep mode input.** Pull nSLEEP logic low to enter low-power sleep mode; pull it high for normal operation. This pin has an internal pull-down resistor. |
| 3 | ENA | - | **Enable pin for phase A.** |
| | - | LSA | **Enables the low-side MOSFET (LS-FET) for phase A.** |
| 4 | ENB | - | **Enable pin for phase B.** |
| | - | LSB | **Enables the LS-FET for phase B.** |
| 5 | ENC | - | **Enable pin for phase C.** |
| | - | LSC | **Enables the LS-FET for phase C.** |
| 6 | PWMA | - | **Pulse-width modulation (PWM) input pin for phase A.** |
| | - | HSA | **Enables the high-side MOSFET (HS-FET) for phase A.** |
| 7 | PWMB | - | **PWM input pin for phase B.** |
| | - | HSB | **Enables the HS-FET for phase B.** |
| 8 | PWMC | - | **PWM input pin for phase C.** |
| | - | HSC | **Enables the HS-FET for phase C.** |
| 9, 26 | SA | | **Phase A output.** |
| 10, 12 | LSS | | **Low-side (LS) source connection for phase A, B, C.** Connect LSS directly to GND. |
| 11, 24 | SB | | **Phase B output.** |
| 13, 22 | SC | | **Phase C output.** |
| 14 | VG | | **Low-side (LS) gate drive output.** Connect a 4.7µF, 10V, X7R ceramic capacitor from VG to ground. |
| 15 | SOA | | **Current-sense output for phase A.** |
| 16 | SOB | | **Current-sense output for phase B.** |
| 17 | SOC | | **Current-sense output for phase C.** |
| 18 | GND | | **Ground.** |
| 19 | VCP | | **Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor from VCP to VIN. |
| 20 | CP1 | | **Charge pump capacitor pins.** Connect a 100nF, X7R ceramic capacitor rated for at least VIN between CP1 and CP2. |
| 21 | CP2 | | |
| 23, 25 | VIN | | **Input supply voltage.** |

## ABSOLUTE MAXIMUM RATINGS (1)

Input voltage ($V_{IN}$) ..... -0.3V to +45V
CP2, VCP ..... $V_{IN}$ to $V_{IN}$ + 6.5V
SA/B/C..... -0.3V to +45V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation ($T_A$ = 25°C) (2)
TQFN-26 (6mmx6mm)…….5.84W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

### *ESD Ratings*

Human body model (HBM).....2kV
Charged device model (CDM).....2kV

### *Recommended Operating Conditions* (3)

Input voltage ($V_{IN}$) ..... 4.75V to 40V
Operating junction temp ($T_J$) .... -40°C to +125°C

### *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

TQFN-26
(6mmx6mm)……...21.4….12.8…°C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, LSS = GND = 0V, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input supply voltage | $V_{IN}$ | | 4.75 | | 40 | V |
| Quiescent current | $I_Q$ | nSLEEP = 1, ENx = 0 | | 4 | 8 | mA |
| | $I_{SLEEP}$ | nSLEEP = 0 | | 1 | | µA |
| **Control Logic** | | | | | | |
| Logic low input threshold | $V_{IL}$ | | | | 0.8 | V |
| Logic high input threshold | $V_{IH}$ | | 2 | | | V |
| Input current logic | $I_{IN(H)}$ | V = 5V | -20 | | +20 | µA |
| | $I_{IN(L)}$ | V = 0V | -20 | | +20 | µA |
| Start-up delay | $t_{OD}$ | At $V_{IN}$ rising or nSLEEP rising | | 1 | | ms |
| Internal pull-down resistance | $R_{PD}$ | All logic inputs | | 500 | | kΩ |
| nFAULT pull-down on resistance | $R_{ON(NFAULT)}$ | | | 10 | | Ω |
| **Protection Circuit** | | | | | | |
| Under-voltage lockout (UVLO) threshold | $V_{UVLO}$ | $V_{IN}$ rising | 4 | 4.4 | 4.8 | V |
| UVLO hysteresis | $\Delta V_{UVLO}$ | | | 470 | | mV |
| Over-voltage protection (OVP) threshold | $V_{OVP}$ | $V_{IN}$ rising | 44.5 | 48 | 51.5 | V |
| OVP hysteresis | $\Delta V_{OVP}$ | | | 1.3 | | V |
| High-side (HS) over-current protection (OCP) threshold | $I_{OCP(HS)}$ | | 10 | 19 | | A |
| Low-side (LS) OCP threshold | $I_{OCP(LS)}$ | | 17.5 | 25 | | A |
| OCP deglitch time (5) | $t_{OCD}$ | | | 0.4 | | µs |
| OCP retry time | $t_{OCR}$ | | | 2 | | ms |
| Thermal shutdown (5) | $T_{TSD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (5) | $\Delta T_{TSD}$ | | | 25 | | °C |
| **Current Sense** | | | | | | |
| Current-sense ratio | | A phase | 1/13000 | 1/11600 | 1/10000 | A/A |
| | | B phase | 1/13000 | 1/11500 | 1/9750 | |
| | | C phase | 1/12500 | 1/11000 | 1/9500 | |
| Current-sense output offset current | $I_{SOx}$ | A phase current = 0A | -35 | -5 | +25 | µA |
| | | B phase current = 0A | -26 | -3 | +21 | |
| | | C phase current = 0A | -33 | -5 | +26 | |
| Current-sense output voltage swing (5) | | | 0 | | 5 | V |
| Current-sense minimum load impedance (5) | | Pull-up | | 1.8 | | kΩ |
| | | Pull-down | | 1 | | kΩ |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, LSS = GND = 0V, unless otherwise noted.**

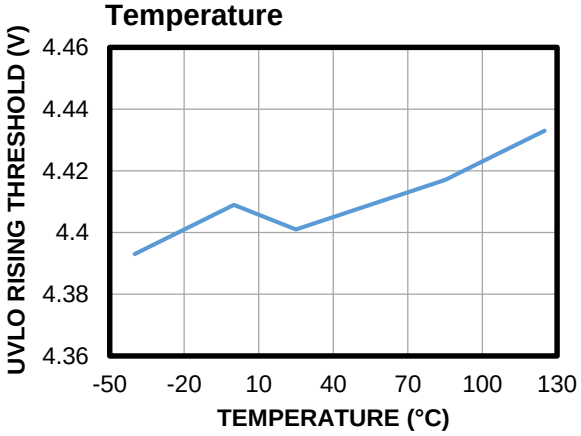
| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Output** | | | | | | |
| High-side MOSFET (HS-FET) on resistance | $R_{ON(HS)}$ | $I_{OUT}$ = 1A, $T_J$ = 25°C | | 15 | 18 | mΩ |
| Low-side MOSFET (LS-FET) on resistance | $R_{ON(LS)}$ | $I_{OUT}$ = 1A, $T_J$ = 25°C | | 15 | 18 | |
| Output rise time (5) | | $I_{OUT}$ = 1A | | 0.45 | | V/ns |
| Output fall time (5) | | $I_{OUT}$ = 1A | | 0.85 | | V/ns |
| **Charge Pump** | | | | | | |
| Charge pump output voltage | $V_{CP}$ | | | $V_{IN}$ + 5 | | V |
| $V_{CP}$ switching frequency | $f_{CP}$ | | | 2000 | | kHz |

**Note:**

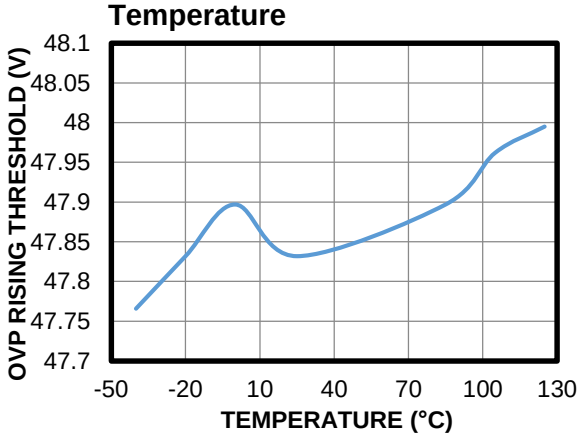
5) Not tested in production.

## TYPICAL CHARACTERISTICS

**UVLO Rising Threshold vs. Temperature**

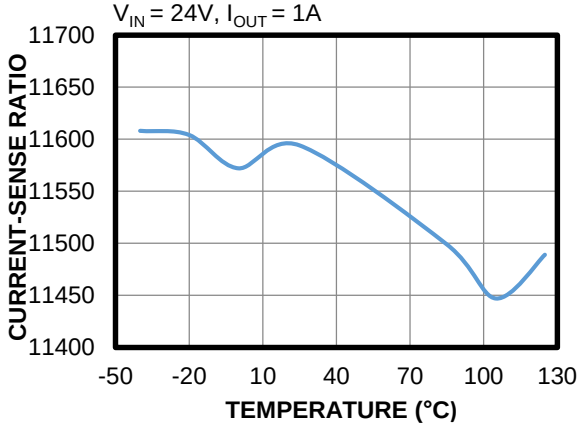



**OVP Rising Threshold vs. Temperature**



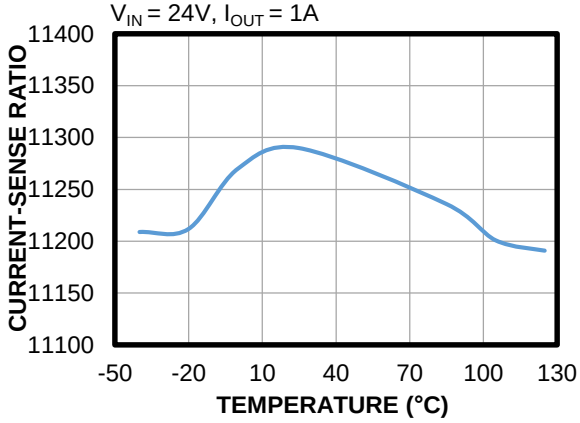

**Phase A Current-Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



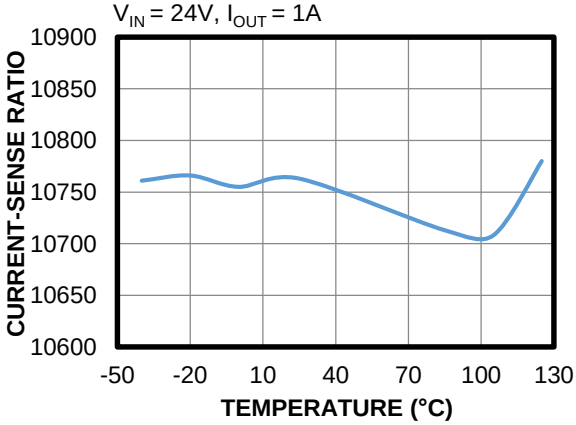

**Phase B Current-Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



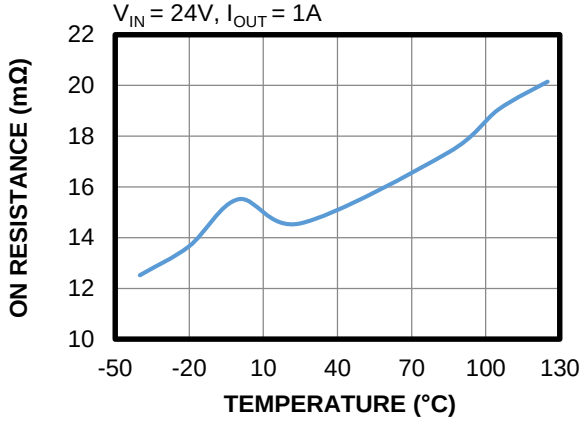

**Phase C Current-Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A




**HS-FET On Resistance vs. Temperature**

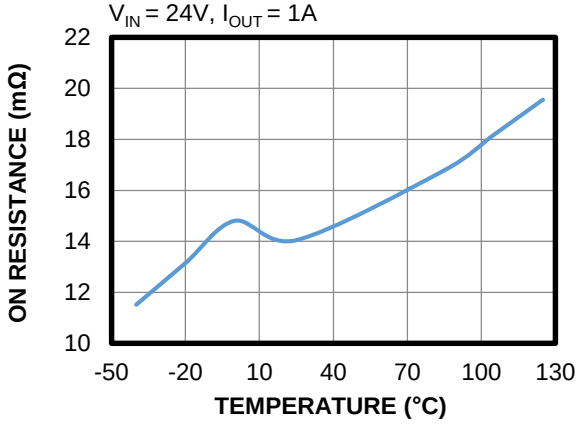
$V_{IN}$ = 24V, $I_{OUT}$ = 1A



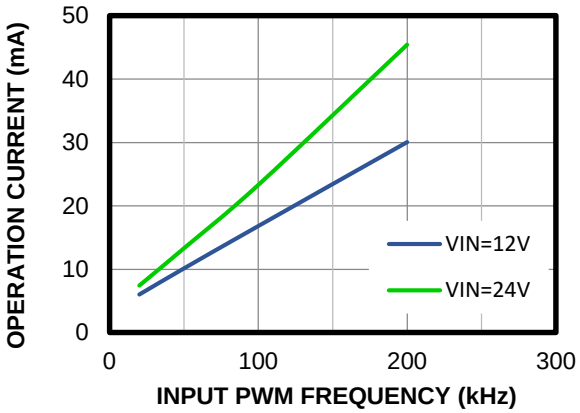
## TYPICAL CHARACTERISTICS *(continued)*

**LS-FET On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



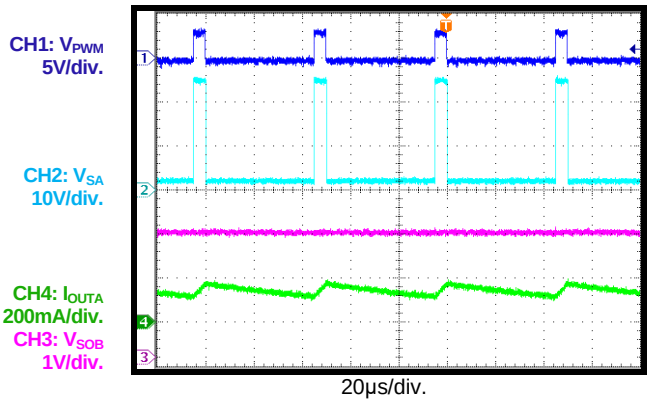

**Operation Current vs. PWM Frequency**



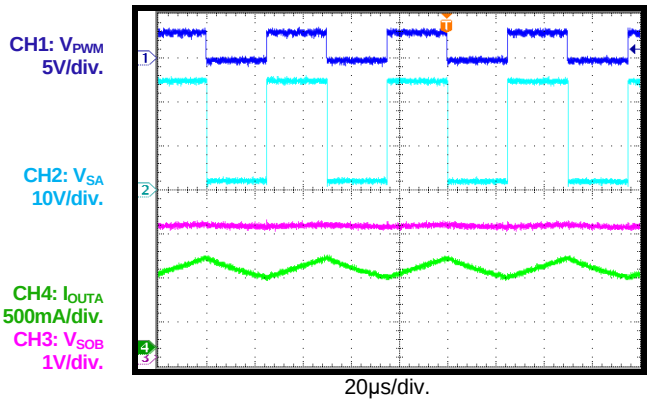
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 24V, phase A switching with 20kHz frequency, phase B LS-FET on, phase C disabled, $V_{REF}$ = 5V, current-sense resistor divider = 5kΩ, $T_A$ = 25°C, resistor + inductor load is 5Ω + 1mH/phase with a star connection, unless otherwise noted.**

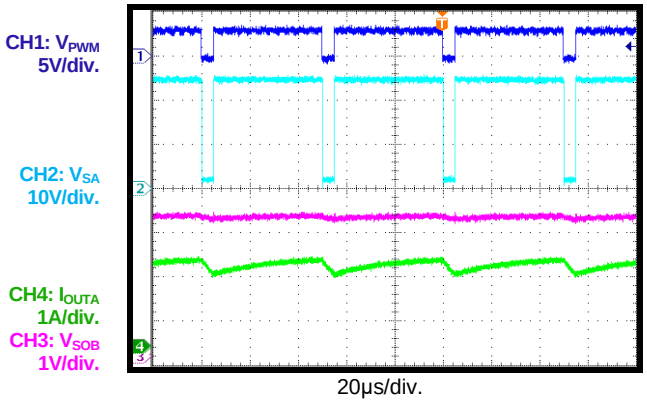
### Steady State
Duty = 10%



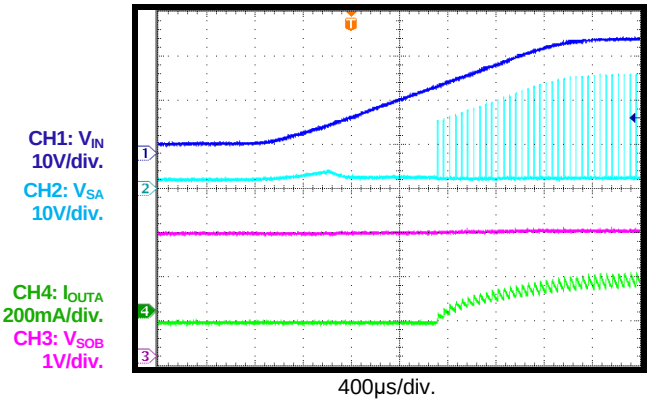

### Steady State
Duty = 50%



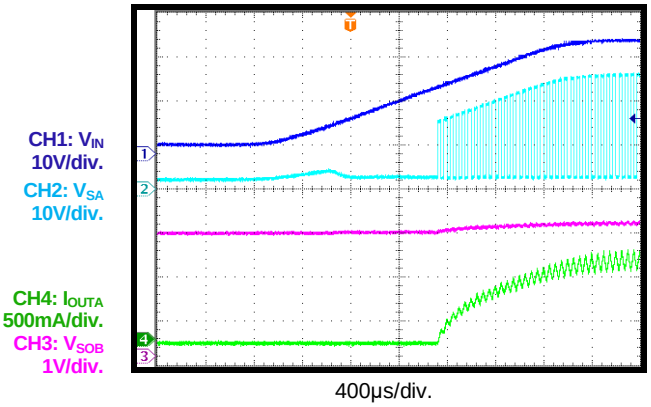

### Steady State
Duty = 90%




### Power Ramping Up
Duty = 10%




### Power Ramping Up
Duty = 50%




### Power Ramping Up
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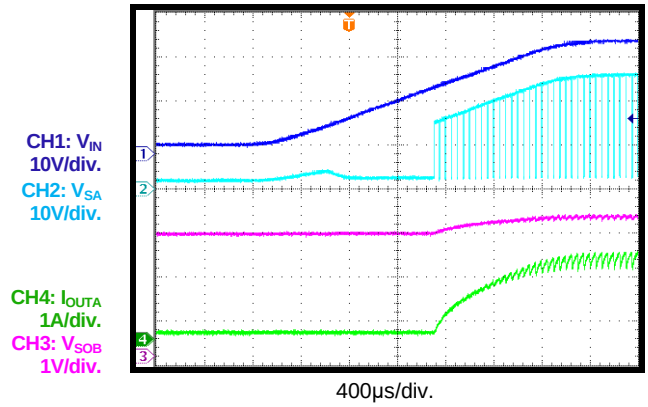
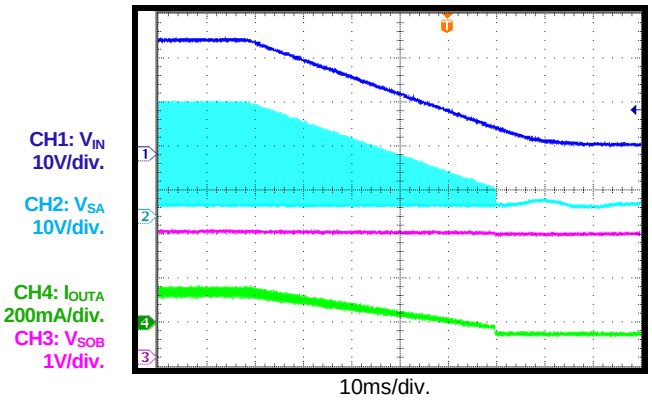


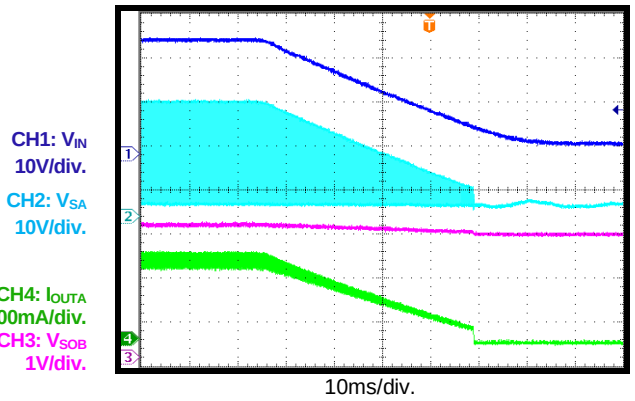
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, phase A switching with 20kHz frequency, phase B LS-FET on, phase C disabled, $V_{REF}$ = 5V, current-sense resistor divider = 5kΩ, $T_A$ = 25°C, resistor + inductor load is 5Ω + 1mH/phase with a star connection, unless otherwise noted.**

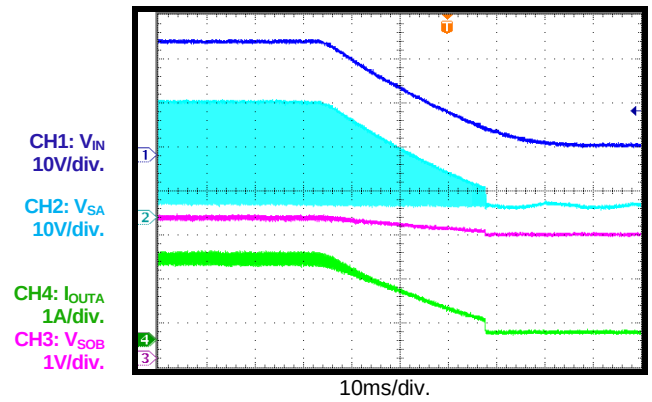
### Power Ramping Down
Duty = 10%



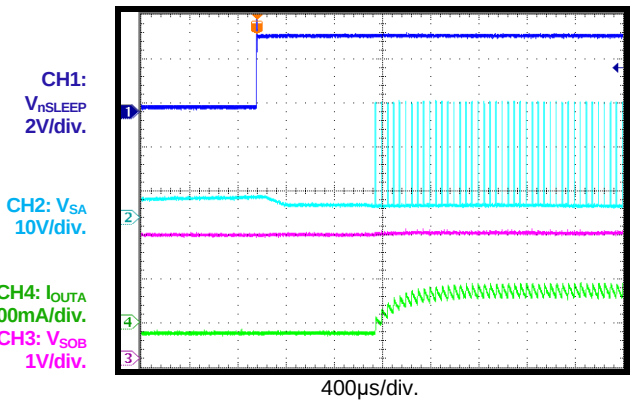

### Power Ramping Down
Duty = 50%



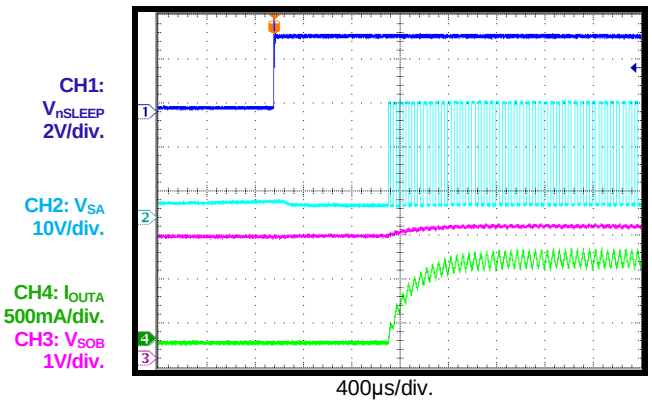

### Power Ramping Down
Duty = 90%



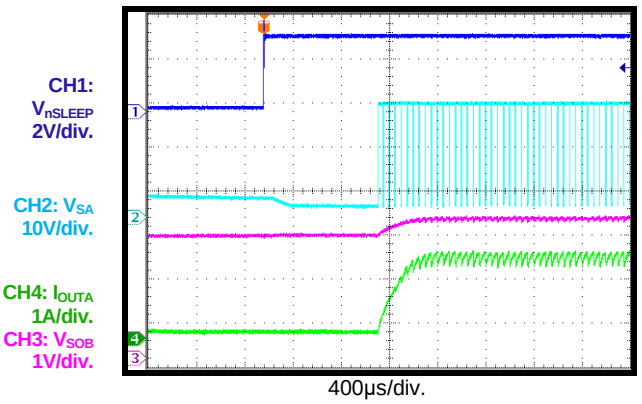

### Sleep Mode Recovery
Duty = 10%




### Sleep Mode Recovery
Duty = 50%



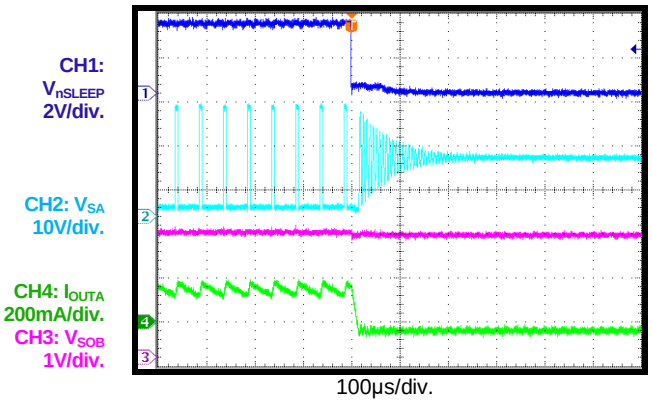

### Sleep Mode Recovery
Duty = 90%



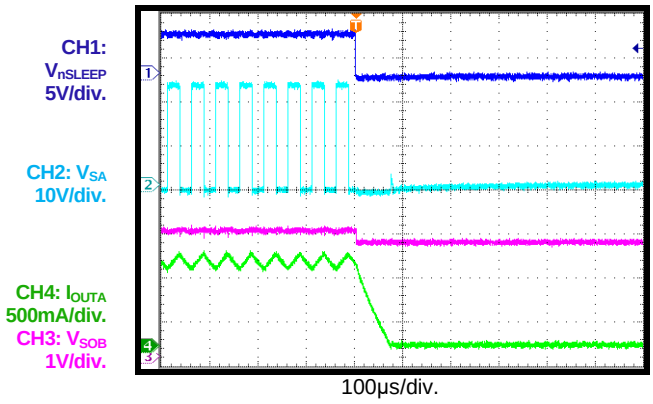
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, phase A switching with 20kHz frequency, phase B LS-FET on, phase C disabled, $V_{REF}$ = 5V, current-sense resistor divider = 5kΩ, $T_A$ = 25°C, resistor + inductor load is 5Ω + 1mH/phase with a star connection, unless otherwise noted.**

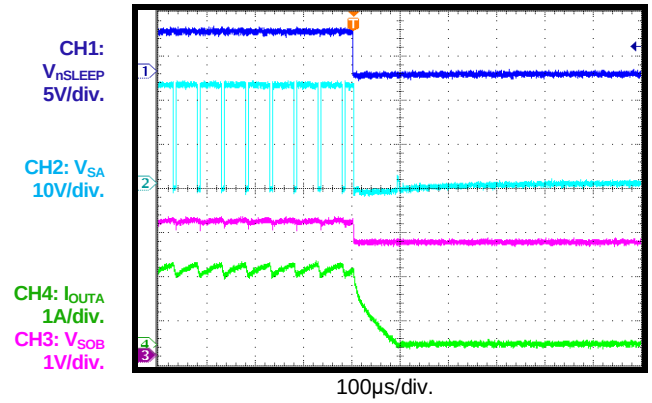
### Sleep Mode Entry
Duty = 10%




### Sleep Mode Entry
Duty = 50%




### Sleep Mode Entry
Duty = 90%



# FUNCTIONAL BLOCK DIAGRAM

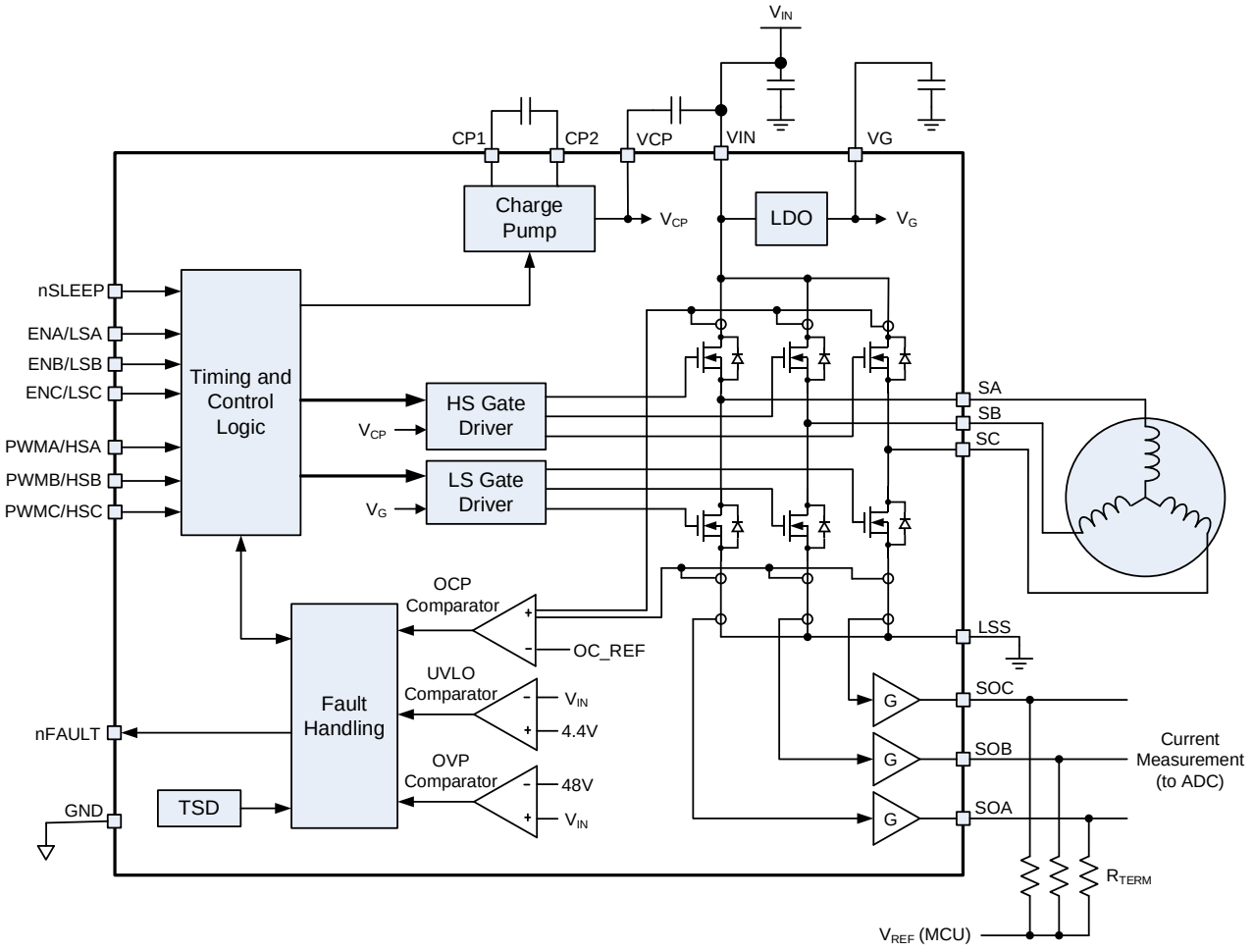



**Figure 1: Functional Block Diagram**

# OPERATION

## Input Logic

The MP6541 has three logic input pins (ENA, ENB, and ENC) that enable the corresponding outputs (SA, SB, SC). When ENx is low, the corresponding output is disabled (output is at high-impedance), and the pulse-width modulation (PWM) input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the output's state (see Table 1).

**Table 1: ENx and PWM Input Logic Truth Table**

| ENx | PWMx | Sx Output |
|---|---|---|
| H | H | VIN |
| H | L | GND |
| L | x (6) | High-impedance |

**Note:**

6) "x" means not applicable.

The MP6541A has separate inputs that are used to enable the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of each phase independently (see Table 2).

**Table 2: HS-FETx and LS-FETx Input Logic Truth Table**

| HS-FETx | LS-FETx | Sx Output |
|---|---|---|
| L | L | High-impedance |
| L | H | GND |
| H | L | VIN |
| H | H | High-impedance |

Note that the logic inputs have weak, internal pull-down resistors.

## nSLEEP Operation

Pull nSLEEP low to put the device into a low-power sleep state. In this state, all internal circuits are disabled and all inputs are ignored. To exit sleep mode, approximately 1ms must pass before the device responds to the inputs. nSLEEP has a weak pull-down resistor.

## Current-Sense Amplifiers

The internal current-sensing circuits detect the current flowing in each of the three outputs. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. It should be noted that only the current flowing in the LS-FET is sensed in both the forward and reverse directions.

To convert this current into a voltage (e.g. input to an analog-to-digital converter [ADC]), place a termination resistor ($R_{REF}$) between SOx and a reference voltage. When there is no current flowing, the resulting output is equal to the reference voltage ($V_{REF}$). When current is flowing, the output voltage ($V_{SOUT}$) can be above or below $V_{REF}$, and can be estimated using Equation (1):

$$V_{SOUT} = V_{REF} + (R_{REF} \times I_{LOAD}) / 11{,}000 \quad (1)$$

When using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground to terminate the outputs. The resulting ADC code is half-scale at zero current.

Figure 2 shows a simplified diagram of the current measurement circuit.

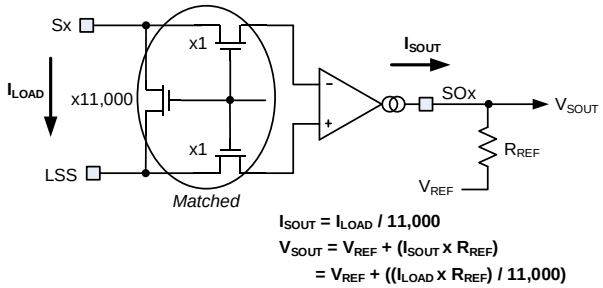



**Figure 2: Current Measurement Circuit**

## Automatic Synchronous Rectification

When driving a current through an inductive load with both of the output MOSFETs turned off, the recirculation current must continue flowing. Typically, this current passes through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6541 implements an automatic synchronous rectification feature.

When both the HS-FET and LS-FET are turned off and the voltage on an Sx output pin is pulled below GND, the LS-FET turns on until the current flowing through it reaches close to zero or until the HS-FET is commanded to turn on. Similarly, if Sx exceeds $V_{IN}$, the HS-FET turns on until the current reaches closes to zero or the LS-FET turns on.

### nFAULT Output

The MP6541 provides an nFAULT output pin, which is pulled active low if a fault condition occurs, such as over-current protection (OCP) or over-temperature protection (OTP). nFAULT is an open-drain output and must be pulled up by an external pull-up resistor.

### Input Under-Voltage Lockout (UVLO) Protection

If $V_{IN}$ falls below the under-voltage lockout (UVLO) threshold ($V_{UVLO}$), all circuitry in the device is disabled and the internal logic resets. Once $V_{IN}$ exceeds $V_{UVLO}$, the device automatically resumes normal operation.

### Over-Voltage Protection (OVP)

If $V_{IN}$ exceeds the over-voltage protection (OVP) threshold ($V_{OVP}$), all output MOSFETs are disabled and nFAULT is not pulled active low. Once $V_{IN}$ falls below $V_{OVP}$, the device automatically resumes normal operation.

### Thermal Shutdown

If the die temperature exceeds safe limits (typically 150°C), all output MOSFETs are disabled and nFAULT is pulled low. Once the die temperature falls to a safe level (typically 125°C), the device automatically resumes normal operation.

### Over-Current Protection (OCP)

The OCP circuit disables the gate driver to limit the current through each MOSFET. If the over-current (OC) limit threshold is reached and lasts longer than the OC deglitch time, then all six output MOSFETs are disabled (outputs have high impedance) and nFAULT is driven low. During this time, synchronous rectification is used to decay the current. The outputs are disabled for 2ms (typically) and are re-enabled automatically.

OC conditions on both high-side (HS) and low-side (LS) devices (e.g. a short to ground, supply, or across the motor winding) result in an OC shutdown.

Figure 3 shows a simplified diagram of the OCP circuit for one output.

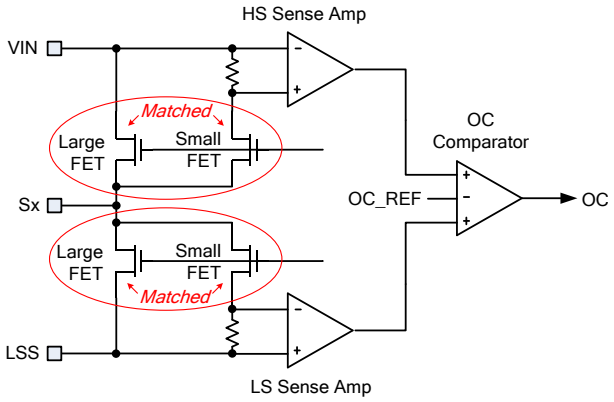



**Figure 3: OCP Measurement Circuit**

### Charge Pump and VG Regulator

An internal low-dropout (LDO) regulator generates a LS gate drive voltage of about 5.5V. A 4.7µF to 10µF bypass capacitor must be placed from VG to ground.

A charge pump is used to generate the gate drive for the HS-FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor rated for at least $V_{IN}$ between the CP1 and CP2 pins, and a 1µF ceramic capacitor rated for at least 10V between VIN and VCP.

# APPLICATION INFORMATION

## External Charge Pump Capacitors

Select the external charge pump capacitors using Table 3.

**Table 3: External Charge Pump Capacitor Selector**

| Specifications of Charge Pump and $V_G$ Capacitors | Min | Nom | Max | Unit |
|---|---|---|---|---|
| CP1 to CP2 capacitance | | 0.1 | | µF |
| CP1 to CP2 capacitor voltage | $V_{IN}$ | | | V |
| $V_{CP}$ to $V_{IN}$ capacitance | | 1 | | µF |
| $V_{CP}$ to $V_{IN}$ capacitor voltage | 10 | | | V |
| $V_G$ capacitance | 4.7 | | 10 | µF |
| $V_G$ capacitor voltage | 10 | | | V |

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and Figure 5 and follow the guidelines below:

1. Place the supply bypass capacitor and charge pump capacitor as close to the IC as possible, adjacent to the pins on the same PCB layer.
2. Use multiple vias to also connect the supply bypass and charge pump capacitors directly under the IC on the opposite side of the PCB.
3. Place as much copper as possible on the long pads.
4. Place large copper areas on the pads, as well as on the same outer copper layer as the device.
5. Place thermal vias inside the pad area to move heat to the copper layers.
6. If via-in-pad construction is not allowed, place multiple vias just outside the pad area.

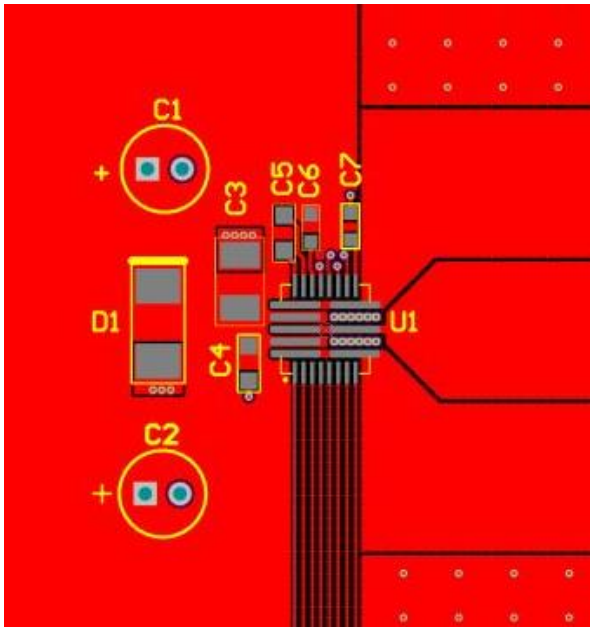



**Figure 4: Recommended PCB Layout**

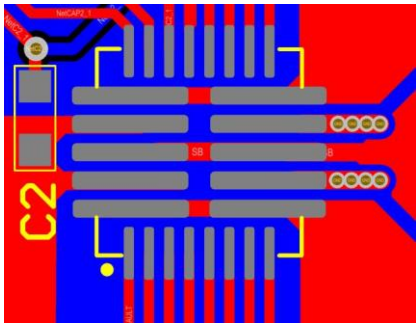



**Figure 5: Thermal Vias outside Pads**

## TYPICAL APPLICATION CIRCUIT

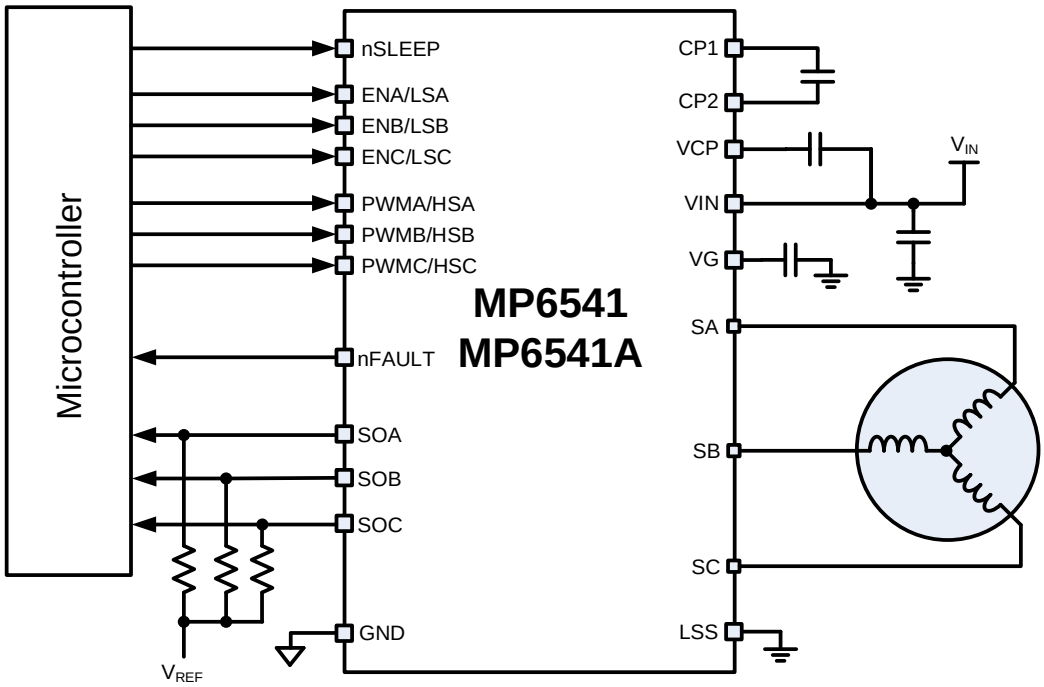
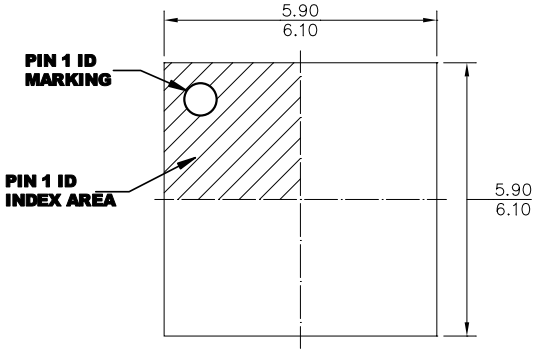


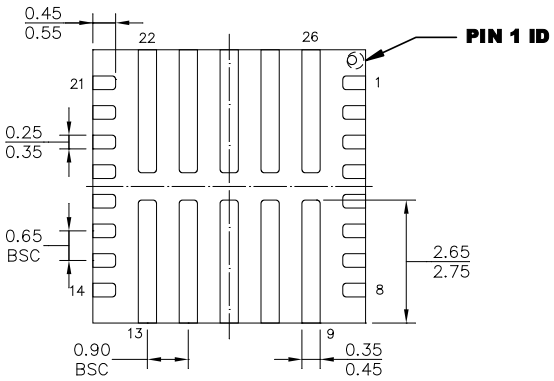

**Figure 4: Typical Application Circuit**

# PACKAGE INFORMATION

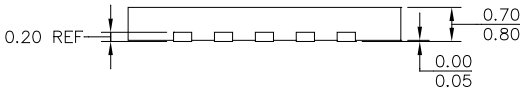
## TQFN-26 (6mmx6mm)



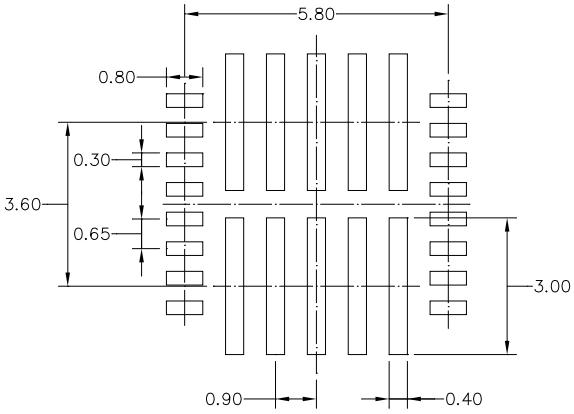

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**

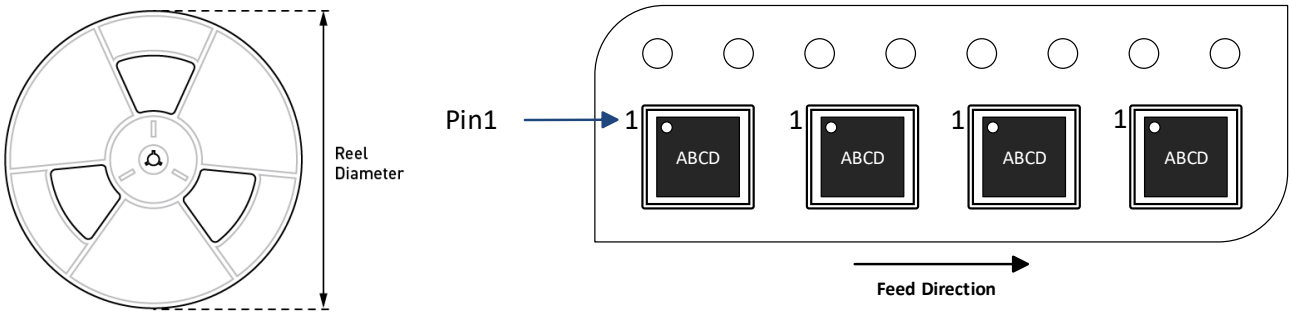



**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP6541GQKT-Z<br>MP6541AGQKT-Z | TQFN-26 (6mmx6mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 11/12/2021 | Initial Release | - |