MP6546

22V, 3A, Peak, 3-Phase BLDC Driver with 1MHz I²C Interface

DESCRIPTION

The MP6546 is a 3-phase brushless DC (BLDC) motor driver for gimbal applications. It has three half-bridge power stages, pre-drivers, field-oriented control (FOC) logic, and angle calculations. The MP6546 supports linear Hall angle inputs or an MPS magnetic angle sensor input. The MP6546 supports multi-slave mode and allows three-axis gimbals to be connected to a single I²C interface to reduce the microcontroller (MCU) load and system cost.

The MP6546 can deliver up to 3A of peak current. It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs (HS-FETs).

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), over-current protection (OCP), short-circuit protection (SCP), and over-voltage protection (OVP).

The MP6546 is available in a QFN-20 (3mmx4mm) package with an exposed thermal pad.

FEATURES

- 3.5V to 22V Operating Supply Voltage
- Three Half-Bridge Drivers
- Up to 1MHz Fast-Mode Plus for I²C
- Configurable Slave Addresses
- Supports Different Angle Sensor Inputs:
  - Linear Hall Sensor Input through HA/HB
  - Magnetic Angle Sensor through SPI/SSC Interface
- Integrated 12-Bit Analog-to-Digital Converter (ADC) for Hall Sensor
- D-Axis and Q-Axis Voltage Loop with Field-Oriented Control (FOC)
- Standby Mode to Save Quiescent Current
- Under-Voltage Lockout (UVLO), Thermal Shutdown (TSD), Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Voltage Protection (OVP)
- One-Time Programmable (OTP) Memory
- Available in a QFN-20 (3mmx4mm) Package

APPLICATIONS

- Gimbals
- Three-Phase Brushless DC (BLDC) Motors

TYPICAL APPLICATIONS

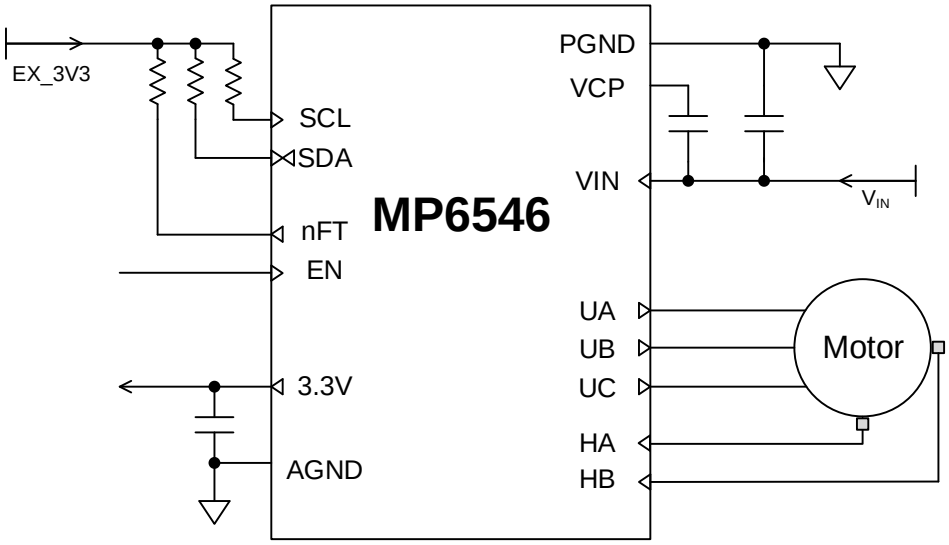


Figure 1: Application with Linear Hall Sensor Input

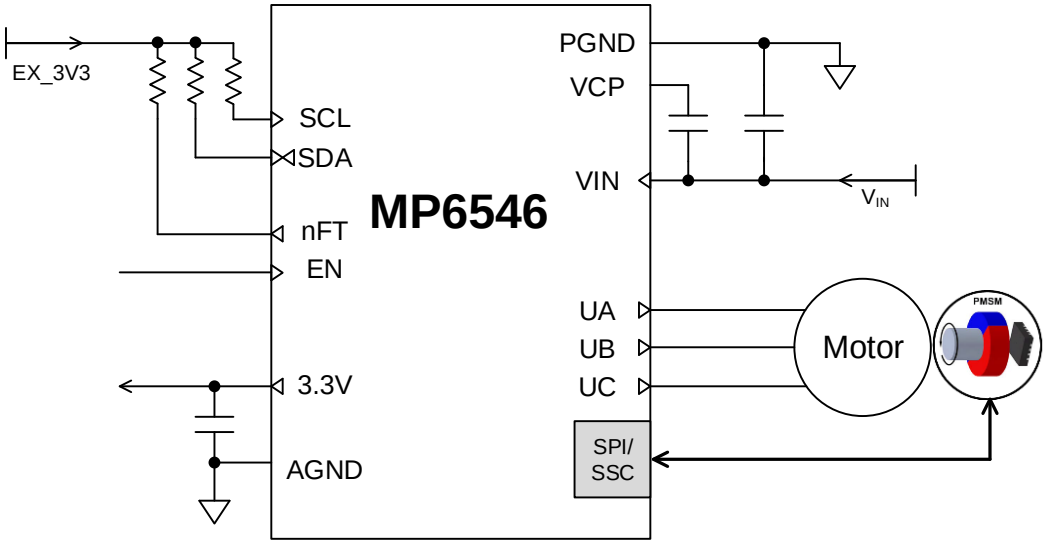


Figure 2: Application with Magnetic Angle Sensor Input

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6546GL-xxxx **	QFN-20 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6546GL-xxxx-Z).

** The default code for this part is “0000”.

TOP MARKING

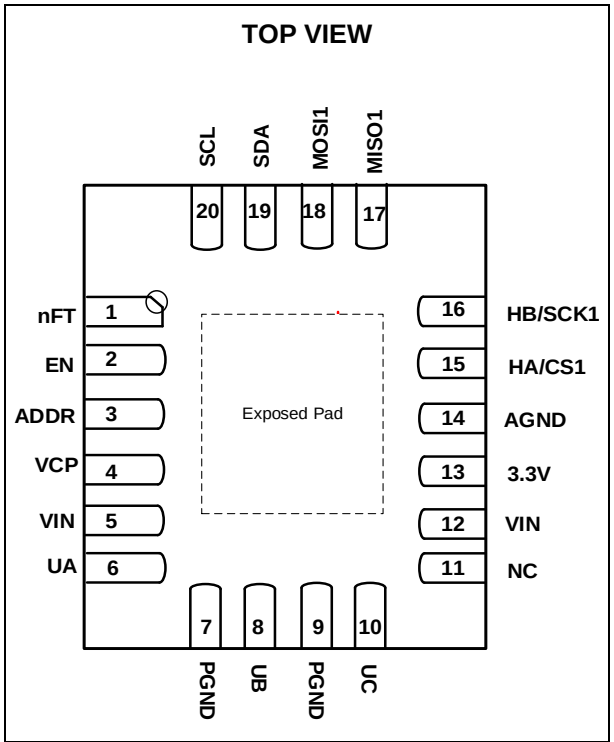
MPYW

6546

LLL

MP: MPS prefix
Y: Year code
W: Week code
6546: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	nFT	**Fault indication.** The nFT pin is an open-drain output that pulls to logic low when there is a fault condition.
2	EN	**IC enable input.** Pull the EN pin to logic high to enter operating mode. This pin is pulled down internally.
3	ADDR	**Slave address selection pin.**
4	VCP	**Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor from VCP to VIN.
5,12	VIN	**Input power.**
6	UA	**Phase A output.**
7,9	PGND	**Power ground.**
8	UB	**Phase B output.**
10	UC	**Phase C output.**
11	NC	**No connection.**
13	3.3V	**3.3V LDO output.** Connect a 4.7µF, 10V, X7R ceramic capacitor from 3.3V to ground.
14	AGND	**Analog ground.**
15	HA/CS1	**Multi-configuration pin.** In linear Hall sensor input mode, this pin is the Hall input A signal. In magnetic angle sensor input mode, this pin is the serial peripheral interface (SPI) chip selection output.
16	HB/SCK1	**Multi-configuration pin.** In linear Hall sensor input mode, this pin is the Hall input B signal. In magnetic angle sensor input mode, this pin is the SPI clock output pin.
17	MISO1	**SPI data input pin.**
18	MOSI1	**SPI data output pin.**
19	SDA	**I²C interface SDA pin.**
20	SCL	**I²C interface SCL pin.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +24V
V_{CP} .....-0.3V to V_{IN} + 5V
V_{UA}, V_{UB}, V_{UC} .....-0.3V to V_{IN} + 0.3V
All other pins .....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2) 2.6W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....3.5V to 22V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm).....48…....10...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, EN = 3.3V, T_J = -40°C to +125°C, unless otherwise noted.

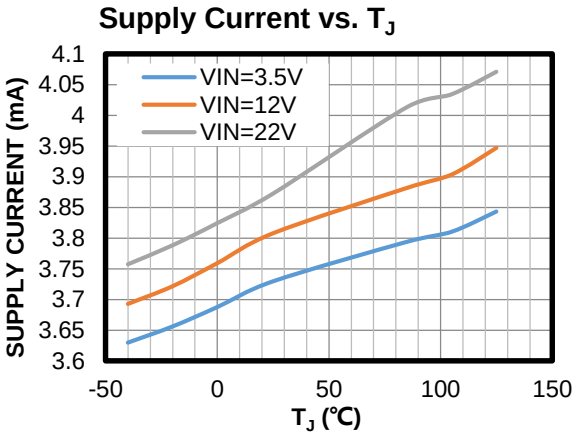
Parameters	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			3.2	3.4	V
Input UVLO hysteresis				0.26		V
Operating supply current	I_{IN}			3.8		mA
Standby current	I_{STB}	3.3V LDO shutdown		90		μA
Shutdown current		EN = low		0.8		μA
EN input high voltage	V_{EN}		1.5			V
EN input low voltage	V_{EN}				0.4	V
High-side (HS) switch on resistance	R_{HS_ON}	I_{OUT} = 1A		150		mΩ
Low-side (LS) switch on resistance	R_{LS_ON}	I_{OUT} = 1A		150		mΩ
Over-current protection (OCP)	I_{OCP}	OCP_SEL = 0		3		A
Short-circuit protection (SCP)	I_{SCP}	OCP_SEL = 0		4.5		A
OC retry time	t_{SCP}			150		ms
Max oscillator frequency	f_{CLK}	Full scale	-2%	15	+2%	MHz
PWM output frequency	f_{SW}			25		kHz
3.3V LDO output	V_{3P3}	I_{OUT} = 100mA	-5%	3.3	+5%	V
nFT pull-down resistance	R_{nFT}	I_{OUT} = 5mA		9		Ω
Charge pump voltage	V_{CP}			V_{IN} + 3.3		V
AD resolution (5)				10		bit
AD full-scale reference	V_{AD}		-0.8%	3.3	+0.8%	V
Thermal shutdown threshold (5)				160		°C
Thermal shutdown hysteresis (5)				40		°C
I²C Interface						
Input low voltage					0.3 x V_{3P3}	
Input high voltage			0.7 x V_{3P3}			V
Open-drain output low voltage	V_{OL_I2C}	3mA load			0.4	V
To I²C max clock frequency	f_{SCL}				1	MHz
SPI Interface						
Input low voltage (MISO1)					0.3 x V_{3P3}	V
Input high voltage (MISO1)			0.7 x V_{3P3}			V
Push-pull output low voltage (MOSI1, SCK1, CS1)	V_{OL_MISO}	1mA load			0.4	V
Push-pull output high voltage (MOSI1, SCK1, CS1)	V_{OL_MISO}	-1mA load	V_{3P3} - 0.4			V
SPI clock frequency (5)	f_{SCK}			2		MHz

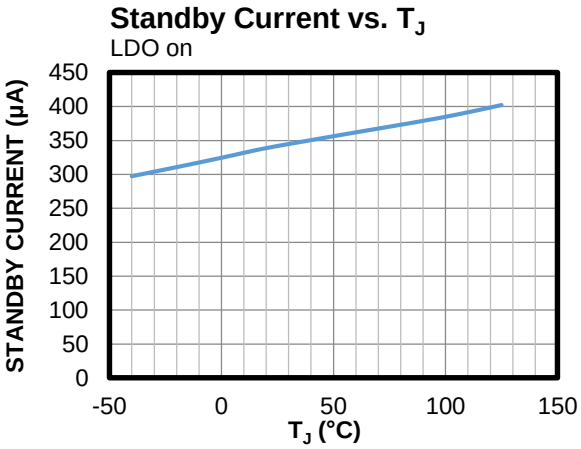
Note:

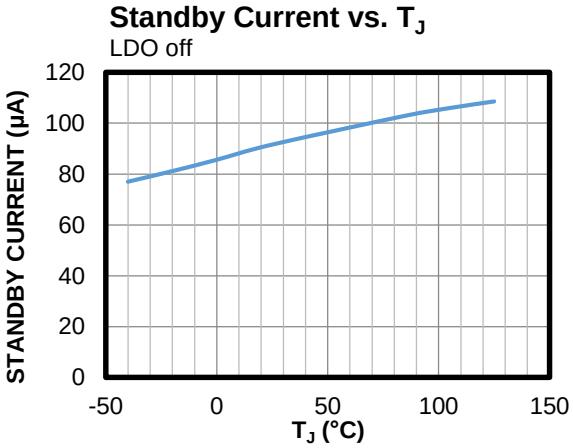
5) Guaranteed by design.

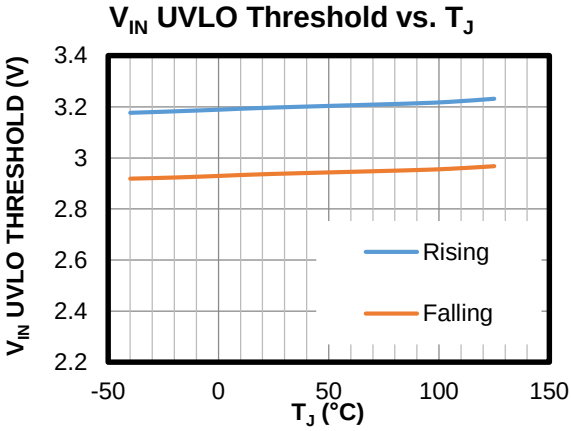
TYPICAL PERFORMANCE CHARACTERISTICS

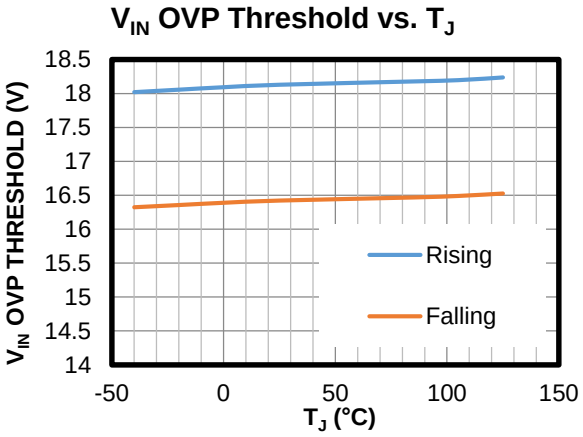
V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

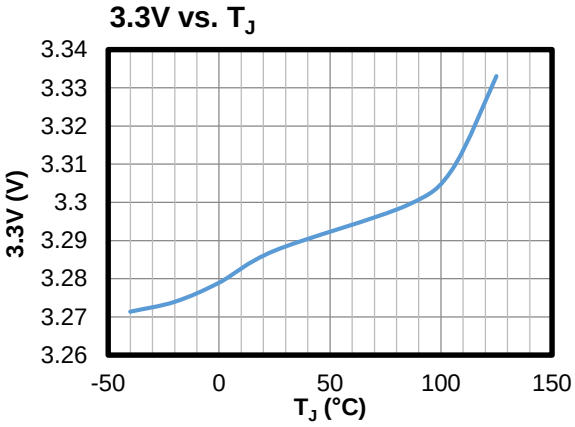








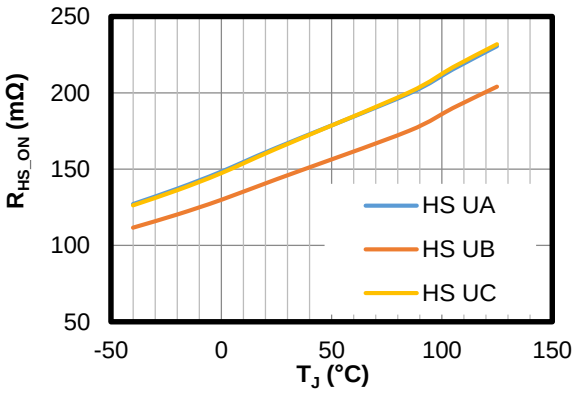




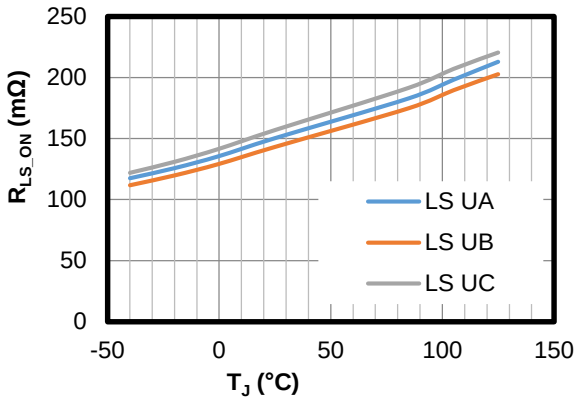
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

HS-FET On Resistance vs. T_J



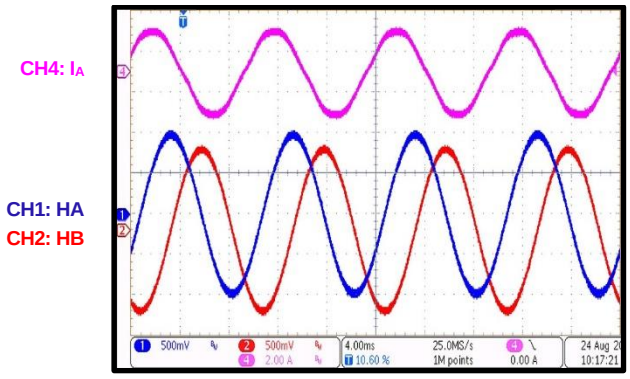
LS-FET On Resistance vs. T_J



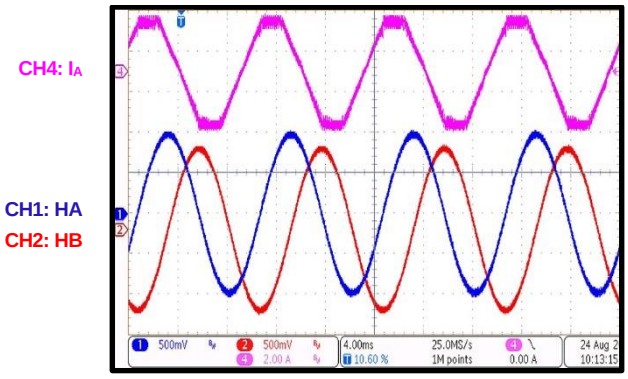
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, SIN/COS signal are added on HA and HB, test on the dummy load, unless otherwise noted.

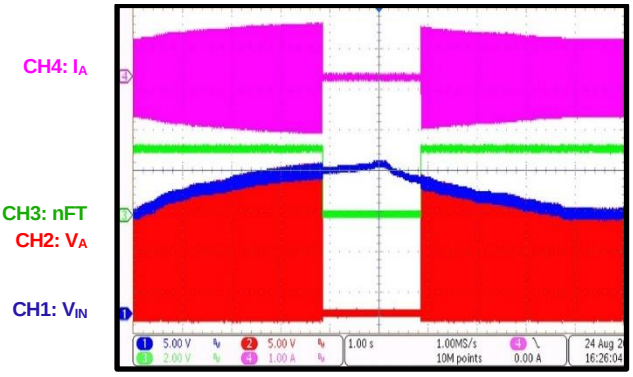
Steady State
PWM duty at 50%



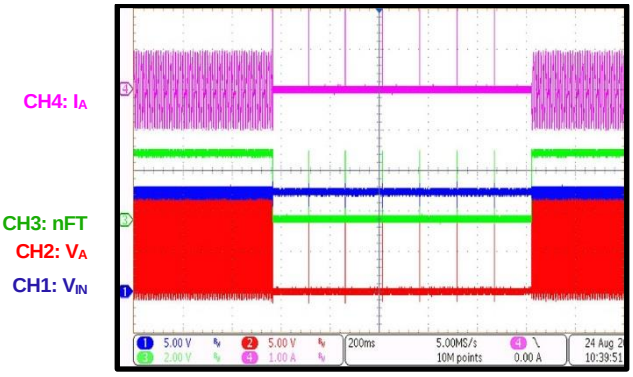
Steady State
PWM duty at 100%



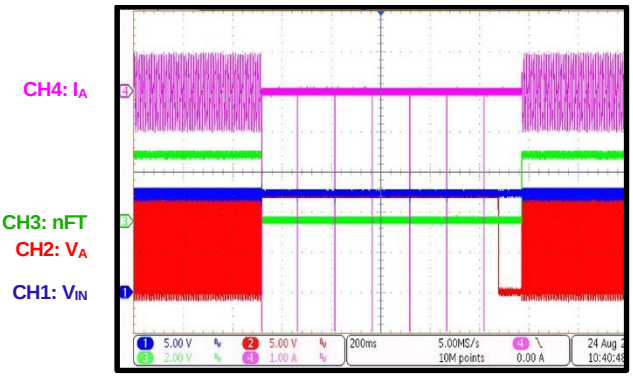
Over-Voltage Protection



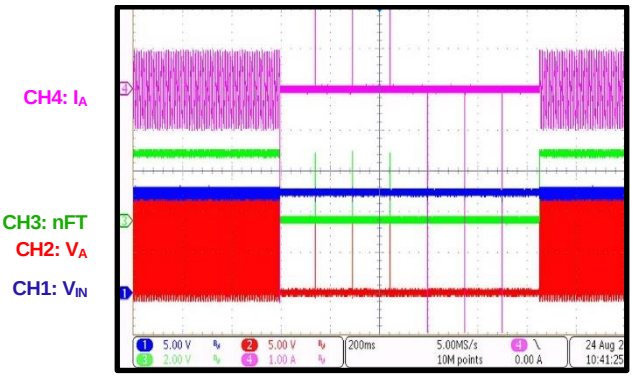
Short-Circuit Protection
Short UA and PGND



Short-Circuit Protection
Short UA and VIN



Short-Circuit Protection
Short UA and UB

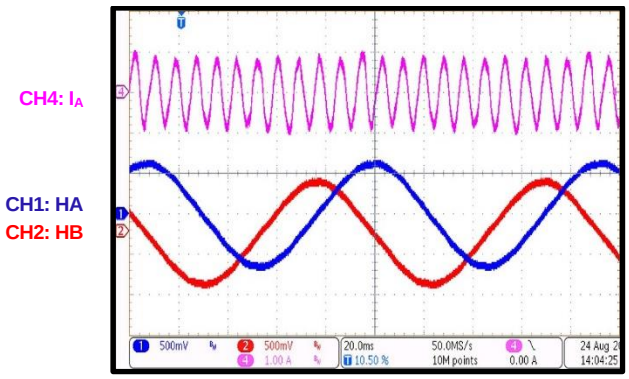


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, test on the gimbal motor unit, unless otherwise noted.

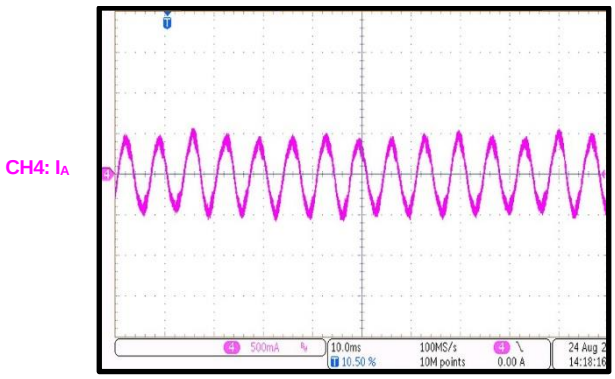
Steady State using Linear Hall Sensor

PWM duty cycle at 100%



Steady State using MagAlpha Sensor

PWM duty cycle at 100%



FUNCTIONAL BLOCK DIAGRAM

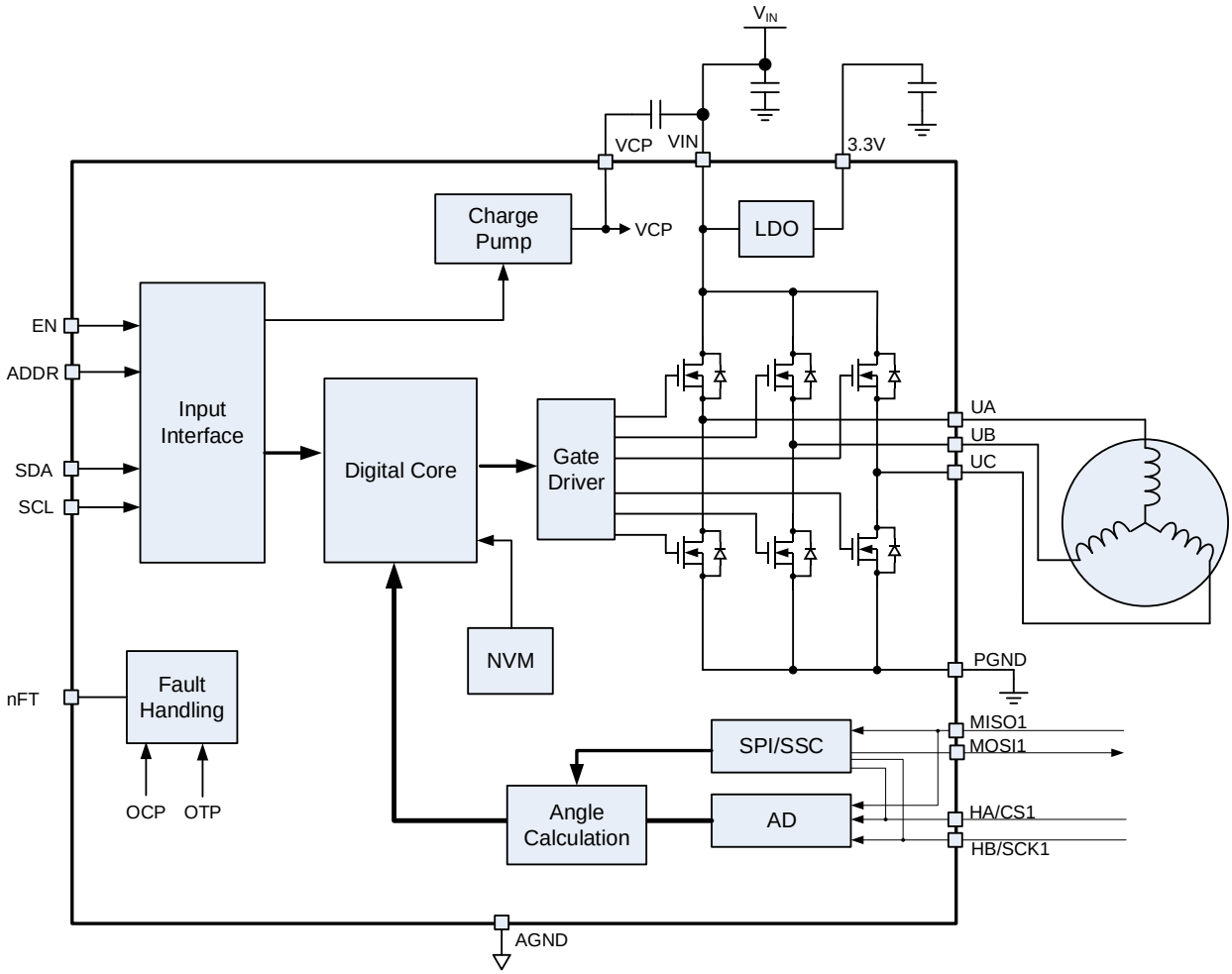


Figure 3: Functional Block Diagram

OPERATION

The MP6546 is a 3-phase brushless DC (BLDC) motor driver that can support both linear Hall sensor inputs and a magnetic sensor input. The device supports multi-slave mode and three-axis gimbals connected to a single I²C interface bus to reduce the microcontroller (MCU) load and system cost. Each slave unit calculates its own angle and controls the motor based on the UD[7:0] and UQ[7:0] bits from the system's MCU via the I²C interface.

External Angle Input Interface

The MP6546 supports both linear Hall inputs and a magnetic Hall sensor input for the field-oriented control (FOC) engine and system control. Use the AMOD bit in register 00h to select the input interface. The external sensor angle can be read via the ANGLE[14:0] bits in register 0Ch.

Magnetic Angle Sensor Input Mode

In magnetic angle sensor input mode, the MP6546 reads the external angle data input through the serial peripheral interface (SPI) or synchronous serial communication (SSC) interface (see Figure 4). Select the communication mode via the SPI_3 bit in register 00h. The baud rate of either interface can be set via the SPI_BAUD[2:0] bits in register 03h.

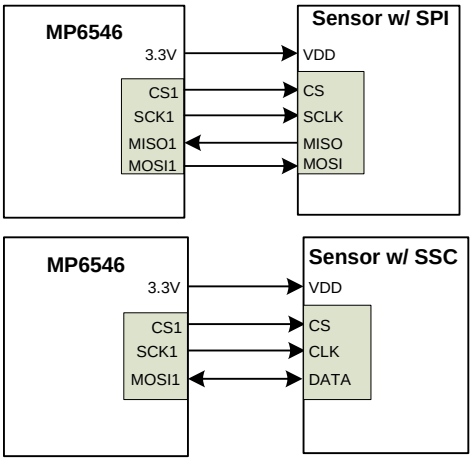


Figure 4: SPI and SSC Interface

The MP6546 supports the magnetic angle sensor ICs from MPS's MagAlpha family, though other angle sensors can be applied if the protocols are compatible. Follow the examples below to configure the MagAlpha family:

1. Read angle: Set SPI_REG_ADDR[4:0] to 0 and set CMD_CODE[2:0] to 0 by writing to register 11h. Then the sensor angle's value can be obtained via ANGLE[14:0].
2. Read register: Set SPI_REG_ADDR[4:0] to the sensor's register address, and set CMD_CODE[2:0] to 1 by writing to register 11h. Then the sensor's register value can be obtained via SPI_DATA[7:0] in register 11h.
3. Write register: Set SPI_REG_ADDR[4:0] to the sensor's register address, set SPI_DATA[7:0] to the sensor's register value, and set CMD_CODE[2:0] to 2.

Linear Hall Sensor Input

In linear Hall sensor input mode, the MP6546 reads the external angle data input through the HA and HB interface. The HA and HB signals go to the internal analog-to-digital converter (ADC), and the digital core calculates the angle based on these two signals (see Figure 5).

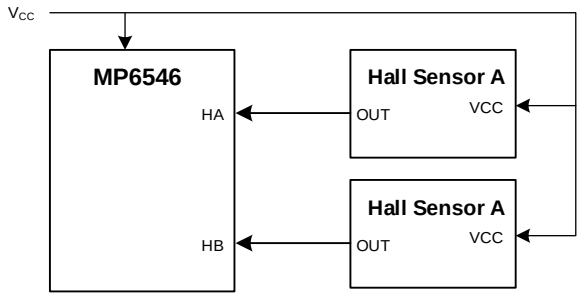


Figure 5: Linear Hall Sensor Interface

To use the linear Hall sensor, set AMOD to 1 to power up the ADC circuit. Then configure VA_BIAS[7:0] and VB_BIAS[7:0] (in register 01h) to compensate for the DC offset of the input SIN/COS signal (V_{OFFSET}). Vx_BIAS[7:0] can be calculated with Equation (1):

$$Vx\_BIAS[7:0] = \frac{V_{OFFSET} - 500}{6.445} \quad (1)$$

For example, if V_{OFFSET} is 1650mV, then register 01h should be set to 0xB2B2.

Internal Angle Processing

Theta Bias, Direction and Pole Pairs

The MP6546 supports a biased angle setting to align the sensor angle's zero position with phase A's axis. This bias can be set via THETA_BIAS[11:0] in register 02h.

The angle direction can be corrected by the THETA_DIR bit in register 00h if the desired rotation direction is opposite of the sensor angle.

The MP6546 supports up to 15 pairs of motor poles, which can be set via POLE_PAIR[3:0] in register 02h.

Theta Filter

The MP6546 supports two type of angle low-pass filters. The first filter is used for internal space vector PWM (SVPWM) control. Select the bandwidth frequency via FLT_N_SVM[2:0] in register 00h. The second filter is provided for the system's angle output. In this scenario, select the bandwidth frequency via FLT_N[1:0] in register 00h, and obtain the angle value by reading ANGLE[14:0].

INL Correction

The MP6546 supports an INL correction function to compensate for the angle error caused by the nonlinear factors. The INL error in one cycle is divided to 32 segments, which are configured by registers INL_00[5:0]~INL_1F[5:0] (registers 13h~1Eh). Each segment can cover an INL error of up to 22.4° (see Figure 6).

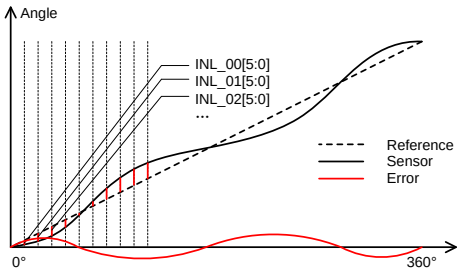


Figure 6: Sensor INL Calibration

INLxx[5:0] can be estimated with Equation (2):

$$INL\_xx[5:0]=\begin{cases}\dfrac{\theta_{INL}}{0.35°}, & \theta_{INL}\geq 0\\ \dfrac{\theta_{INL}}{0.35°}+2^{6}, & \theta_{INL}<0\end{cases} \quad (2)$$

Where θ_{INL} is INL error (in °), and INL_xx[5:0] is the correction value represented by a signed number of 6 bits.

For example, if θ_{INL} is -5°, then set INL_xx[5:0] to 0x32.

The INL compensation for the current position can be obtained via INL_COMP[7:0] in register 0Dh.

Drive Mode

The MP6546 supports two inverter drive modes: vector control mode and duty control mode. Select the control mode via the DRV_MOD bit in register 00h.

Vector Control Mode

In vector control mode, UD[9:0] (in register 08h) and UQ[9:0] (in register 09h) must be set, and the angle that is used for IPARK coordinate transformation can come from either the external sensor or ANGLE_T[11:0] in register 07h. Use the ALN_MOD bit in register 0Ah to select the angle source.

UD[9:0] and UQ[9:0] can be calculated with Equation (3) and Equation (4), respectively:

$$UD[9:0]=\begin{cases}\dfrac{512\sqrt{3}ud}{V_{IN}}, & ud\geq 0\\ \dfrac{512\sqrt{3}ud}{V_{IN}}+2^{10}, & ud<0\end{cases} \quad (3)$$

$$UQ[9:0]=\begin{cases}\dfrac{512\sqrt{3}uq}{V_{IN}}, & uq\geq 0\\ \dfrac{512\sqrt{3}uq}{V_{IN}}+2^{10}, & uq<0\end{cases} \quad (4)$$

Where UD is d-axis voltage, UQ is q-axis voltage, and V_{IN} is the bus input voltage.

Duty Control Mode

Set DRV_MOD in register 00h to 1 for duty control mode. In this mode, the duty of the inverter's three-phase output is determined via registers 07h, 08h, and 09h, respectively.

As PWMx[8:0] (where x = A, B, or C) changes from 0x100 to 0x1FF, the voltage duty changes from 100% to 0%. Reset the ninth bit of PWMx[8:0] (PWMx[8]) to shut down the output of

the corresponding channel. All these changes only take effect after register 09h is written to a certain value.

I²C Input Interface

To access the internal register and angle data, the MP6546 has fast-mode plus I²C mode, which can support a clock frequency up to 1MHz.

The slave address can be configured via two methods. The first method is to set ADDR[1:0] in register 00h to 0. In this scenario, the address is set by the ADDR pin. The low level represents 0x07h, the middle level represents 0x08h, and the high value represents 0x09h.

The second method is to set the address using the register. See the Register Description section on page 16 for more details.

The MP6546 supports multi-slave bus connections to support up to three slaves (see Figure 7). All slaves can monitor the SDA input data and receive data at the same time with the broadcasting address. With the mapped address, only one slave can transmit data through the SDA data pin, while the other two slaves release the bus.

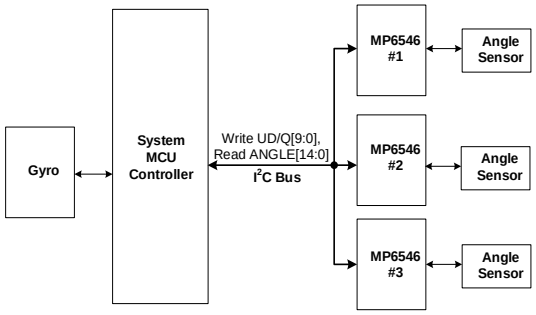


Figure 7: Multi-Slave Bus Connection

D/Q Reference Frame Voltage Control

The MP6546 provides D/Q reference frame rotor FOC voltage control. The voltage command for the D/Q reference comes from the main system MCU via the I²C interface. Then the UA/UB/UC output is modulated with the SVPWM output. This controls the three-axis motors via the system MCU.

Enable and Standby Operation

To reduce the operating current, the IC works in two modes for flexibility. These modes are described below.

1. By pulling the EN pin high: Set the STDBY_EN bit in register 00h then write to register 10h. Then the IC works in standby mode to reduce the quiescent current. A 3.3V low-dropout (LDO) regulator can be shut down or activated via the trimming bit TRIM_ENP in register 03h.

   Write to register 0Fh to force the IC to return to normal operation. The IC also resumes normal operation if a negative edge is detected on the SCL/SCK pin.

2. By pulling the EN pin low: The IC completely shuts down.

Over-Current Protection (OCP)

The MP6546 has a cycle-by-cycle current limit to clamp the peak current near a certain threshold. When the current flowing through the MOSFETs exceeds this threshold, all low-side MOSFETs (LS-FETs) turn on to reduce the phase current. This trigger threshold is selectable. The default threshold is a 3A peak current, and it scales down to 75% if the OCP_SEL bit in register 00h is set to high. The current-limit function can be disabled by setting OCP_EN in register 00h to 0.

Short-Circuit Protection (SCP)

The MP6546 provides short-circuit protection (SCP) to prevent IC damage caused by an over-current condition. When the current through the MOSFETs exceeds the threshold after the 1µs blanking time, all MOSFETs turn off. After about 150ms, the IC resumes normal operation. The default threshold is a 4.5A peak current, and it scales down to 75% if the OCP_SEL bit in register 00h is set to high. SCP can be disabled by setting SCP_EN in register 00h to 0.

Thermal Shutdown (TSD)

The MP6546's die also features thermal monitoring. If the die temperature exceeds 155°C, all MOSFETs turn off. Once the die temperature drops below 105°C, operation automatically resumes.

Over-Voltage Protection (OVP)

V_{IN} is detected to prevent MOSFET breakdown. If V_{IN} exceeds 18V, all MOSFETs turn off. Once V_{IN} drops below 16V, operation automatically resumes. Over-voltage protection (OVP) is

disabled by default. Set OVP_EN in register 00h to 1 to enable OVP.

Under-Voltage Lockout (UVLO)

When the voltage on the VIN pin (V_{IN}) falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled and the internal logic is reset. Operation resumes when V_{IN} exceeds the UVLO threshold.

Fault Output Indication

The MP6546 provides an nFT output pin that is driven active low in the event of a fault condition, such as SCP, thermal shutdown, or OVP. This pin is an open-drain output that must be pulled up by an external resistor. If an error is detected, the related register bit(s) is set to 1.

3.3V LDO Output

An internal LDO regulator generates a 3.3V voltage with a 100mA capacity, which could be used to power a small, low-power MCU.
A bypass capacitor between 4.7µF and 10µF must be connected from the 3.3V pin to the ground (see C4 in the Typical Application Circuits section on page 21).

Charge Pump

A charge pump generates the gate drive for the HS-FETs. The charge pump requires one external capacitor placed between VIN and VCP. A ceramic capacitor of 1µF rated at least 10V is recommended (see C3 in Typical Application Circuits on page 21).

REGISTER MAP (6)

Add.	Type	H/L	Default	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h	OTP	H	E0h	OCP_EN	SCP_EN	STDBY_EN	ADDR[1:0]		OCP_SEL	AMOD	THETA_DIR
		L	03h	OVP_EN	FLT_N_SVM[1:0]		DRV_MOD	SPI_3	FLT_N[2:0]		
01h	OTP	H	51h	VA_BIAS[7:0]							
		L	51h	VB_BIAS[7:0]							
02h	OTP	H	00h	THETA_BIAS[11:4]							
		L	07h	THETA_BIAS[3:0]				POLE_PAIR[3:0]			
03h	OTP	H	01h	SPI_BAUD[2:0]			RESERVED				TRIM_ENP
		L	00h	PCODE[7:0]							
07h	RAM	H	00h	RESERVED				ANGLE_T[11:8]			
		L	00h	ANGLE_T[7:0]							
08h	RAM	H	00h	RESERVED						UD[9:8]	
		L	00h	UD[7:0]							
09h	RAM	H	00h	RESERVED						UQ[9:8]	
		L	00h	UQ[7:0]							
0Ah	RAM	H	08h	RESERVED					ALN_MD	RESERVED	
		L	00h	RESERVED							
0Ch	RO	H	-	FAULT	ANGLE[14:8]						
		L	-	ANGLE[7:0]							
0Dh	RO	H	-	RESERVED				SCPF	TSDF	OVPF	OCPF
		L	-	INL_COMP[7:0]							
0Fh	CMD	H	-	NOR_MOD							
		L	-								
10h	CMD	H	-	STB_MOD							
		L	-								
11h	RAM	H	00h	CMD_CODE[2:0]			SPI_REG_ADDR[4:0]				
		L	00h	SPI_DATA[7:0]							
13h	RAM	H	00h	INL_02[3:0]				INL_01[5:2]			
		L	00h	INL_01[1:0]		INL_00[5:0]					
14h	RAM	H	00h	INL_05[1:0]		INL_04[5:0]					
		L	00h	INL_03[5:0]						INL_02[5:4]	
15h	RAM	H	00h	INL_07[5:0]						INL_06[5:4]	
		L	00h	INL_06[4:0]				INL_05[5:2]			
16h	RAM	H	00h	INL_0A[3:0]				INL_09[5:2]			
		L	00h	INL_09[1:0]		INL_08[5:0]					
17h	RAM	H	00h	INL_0D[1:0]		INL_0C[5:0]					
		L	00h	INL_0B[5:0]						INL_0A[5:4]	
18h	RAM	H	00h	INL_0F[5:0]						INL_0E[5:4]	
		L	00h	INL_0E[4:0]				INL_0D[5:2]			
19h	RAM	H	00h	INL_12[3:0]				INL_11[5:2]			
		L	00h	INL_11[1:0]		INL_10[5:0]					
1Ah	RAM	H	00h	INL_15[1:0]		INL_14[5:0]					
		L	00h	INL_13[5:0]						INL_12[5:4]	
1Bh	RAM	H	00h	INL_17[5:0]						INL_16[5:4]	
		L	00h	INL_16[4:0]				INL_15[5:2]			
1Ch	RAM	H	00h	INL_1A[3:0]				INL_19[5:2]			
		L	00h	INL_19[1:0]		INL_18[5:0]					
1Dh	RAM	H	00h	INL_1D[1:0]		INL_1C[5:0]					
		L	00h	INL_1B[5:0]						INL_1A[5:4]	
1Eh	RAM	H	00h	INL_1F[5:0]						INL_1E[5:4]	
		L	00h	INL_1E[4:0]				INL_1D[5:2]			

Note:

6) In the H/L column, “H” means bits[15:8], while “L” means bits[7:0].

REGISTER DESCRIPTION

CONTROL1 (00h)

The CONTROL1 command configures some basic settings.

Bits	Name	Description
15	OCP_EN	0: Disable over-current protection 1: Enable over-current protection
14	SCP_EN	0: Disable short-circuit protection 1: Enable short-circuit protection
13	STDBY_EN	0: Disable standby mode 1: Enable standby mode
12:11	ADDR[1:0]	00: The slave address is set by the ADDR pin 01: The slave address is 0x07h 10: The slave address is 0x08h 11: The slave address is 0x09h
10	OCP_SEL	1: The over-current protection threshold is 2.25A 0: The over-current protection threshold is 3A
9	AMOD	0: Magnetic hall sensor with SPI interface 1: Linear Hall sensor with HA/HB interface
8	THETA_DIR	0: Theta direction is consistent to the sensor 1: Theta direction is opposite to the sensor
7	OVP_EN	0: Disable over-voltage protection 1: Enable over-voltage protection
6:5	FLT_N_SVM[1:0]	Sets the bandwidth frequency (f_C) for SVPWM. 1: 600Hz 2: 300Hz 3: 150Hz 4: 75Hz
4	DRV_MOD	0: Vector control mode 1: Duty control mode
3	SPI_3	0: 4-wire SPI 1: 3-wire SPI (SSC)
2:0	FLT_N[2:0]	Sets the bandwidth frequency (f_C) for ANGLE[14:0]. 0: The filter does not work 1: 600Hz 2: 300Hz 3: 150Hz 4: 75Hz 5: 37Hz 6: 18Hz 7: 9Hz

ADC_BIAS (01h)

The ADC_BIAS command configures the voltage input bias in linear Hall mode.

Bits	Name	Description
15:8	VA_BIAS[7:0]	Set the Hall input A bias.
7:0	VB_BIAS[7:0]	Set the Hall input B bias.

THETA_BIAS (02h)

The THETA_BIAS command configures sensor angle bias.

Bits	Name	Description
15:4	THETA_BIAS[11:0]	Sets the mechanical theta bias.
3:0	POLE_PAIR[3:0]	Sets the motor pole pairs.

CONTROL2 (03h)

The CONTROL2 command configures some basic settings.

Bits	Name	Description
15:13	SPI_BAUD[2:0]	Set the baud rate of SPI. 0: SPI CLK = 7.5MHz 1: SPI CLK = 3.75MHz 2: SPI CLK = 2.5MHz 3: SPI CLK = 1.875MHz 4: SPI CLK = 1.5MHz 5: SPI CLK = 1.25MHz 6: SPI CLK = 1.07MHz 7: SPI CLK = 0.938MHz
12:9	RESERVED	Reserved.
8	TRIM_ENP	0: The 3.3V LDO is off in standby mode 1: The 3.3V LDO is on in standby mode
7:0	PCODE[7:0]	Production code number.

ANGLE_TEST (07h)

The ANGLE_TEST command configures the angle test value or output duty.

Bits	Name	Description
15:12	RESERVED	Reserved.
11:0	ANGLE_T[11:0]	If DRV_MOD = 0: Sets the align angle in vector control mode If DRV_MOD = 1: Sets phase A's duty in duty control mode

D_AXIS_VOLTAGE (09h)

The D_AXIS_VOLTAGE command configures the voltage vector or output duty.

Bits	Name	Description
15:10	RESERVED	Reserved.
9:0	UD[9:0]	If DRV_MOD = 0: Sets the d-axis voltage in vector control mode If DRV_MOD = 1: Sets phase B's duty in duty control mode

Q_AXIS_VOLTAGE (09h)

The Q_AXIS_VOLTAGE command configures the voltage vector or output duty.

Bits	Name	Description
15:10	RESERVED	Reserved.
9:0	UQ[9:0]	If DRV_MOD = 0: Sets the Q-axis voltage in vector control mode If DRV_MOD = 1: Sets phase C's duty in duty control mode

ALIGN_MOD (0Ah)

The ALIGN_MOD command configures the angle source used in vector control mode.

Bits	Name	Description
15:11	RESERVED	Reserved.
10	ALN_MD	0: The angle used in vector control mode is from an external sensor 1: The angle used in vector control mode is from register ANGLE_T[11:0]
9:0	RESERVED	Reserved.

ANGLE (0Ch)

The ANGLE command shows the mechanical angle from external sensor.

Bits	Name	Description
15	FAULT	Integrated error indication bit.
14:0	ANGLE[14:0]	The mechanical angle in one cycle.

FAULT_FLAG (0Dh)

The FAULT_FLAG command shows the status of each fault type.

Bits	Name	Description
15:12	RESERVED	Reserved.
11	SCPF	Short-circuit protection (SCP) flag.
10	TSDF	Thermal shutdown (TSD) flag.
9	OVPF	Over-voltage protection (OVP) flag.
8	OCPF	Over-current protection (OCP) flag.
7:0	INL_COMP[7:0]	INL compensation value at the current position.

NOR_MOD (0Fh)

The NOR_MOD command controls when to enter work mode.

Bits	Name	Description
15:0	NOR_MOD	Write to this register to enter work mode.

STB_MOD (10h)

The STB_MOD command controls when to enter standby mode.

Bits	Name	Description
15:0	STB_MOD	Write to this register to enter standby mode.

SPI_CMD (11h)

The SPI_CMD command configures SPI communication.

Bits	Name	Description
15:13	CMD_CODE[2:0]	0: Sensor angle read 1: Sensor register read 2: Sensor register write
12:8	SPI_REGADDR[4:0]	Set the sensor register address.
7:0	SPI_DATA[7:0]	Read/Write the sensor register value.

INL_DATA (13h~1Eh)

The INL_DATA command configures INL compensation for the sensor angle.

Bits	Name	Description
15:0	INL_xx[x:x]	Sets the INL correction value.

APPLICATION INFORMATION

Selecting an External Schottky Diode

In applications where thermal shutdown might be triggered, add a Schottky diode in parallel with the three-phase outputs to VIN (D1, D2, and D3 for phase A, phase B, and phase C, respectively) to improve the current capacity and temperature tolerance range.

In general, it is recommended to use a diode with a 30V reverse breakdown voltage, 1A forward continuous current, and SOT-123 package.

Selecting the Input Capacitor

The input capacitors (C1 and C2) can reduce the device's switching noise and the surge current drawn from the input supply. Use larger-value ceramic capacitors with X5R or X7R dielectrics for their low ESR and temperature coefficients.

In general, it is recommended to use two ceramic capacitors (each VIN pin requires a capacitor) of 10μF rated for at least 25V.

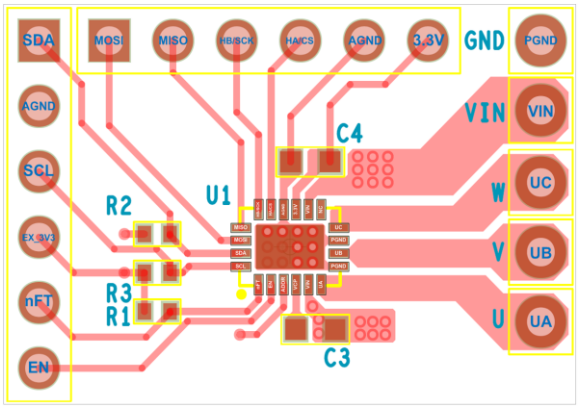
ADDR Pull-Up Power

The MP6546 checks the ADDR level status 100μs after start-up. If the pull-up power rises too slowly, an incorrect slave address might be set. It is recommended to pull the ADDR pin to the 3.3V pin if the address is set to 0x09h by the ADDR pin.

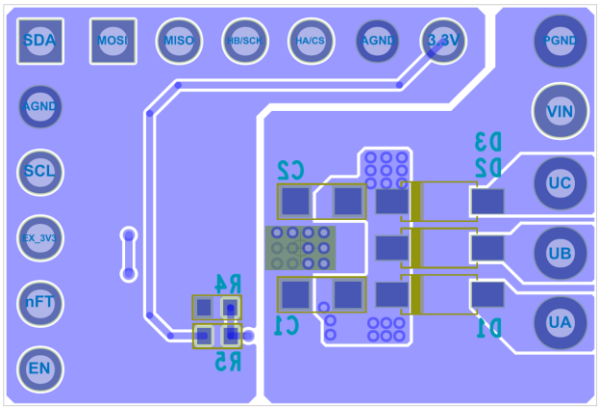
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, follow the guidelines below:

1. Use wider copper for the input, output, and GND-connecting wire to improve thermal performance.
2. Place GND vias near the input capacitor to improve thermal performance and reduce ground impedance.
3. Connect PGND and AGND as close to one another as possible.
4. Do not to introduce power circuit interference to the analog circuit.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

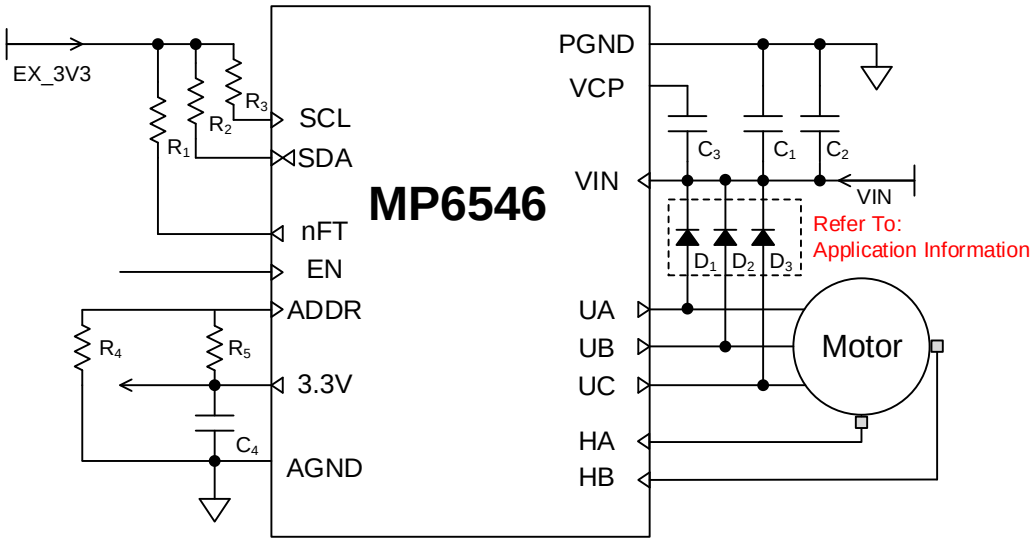


Figure 9: Application with Linear Hall Sensor Input

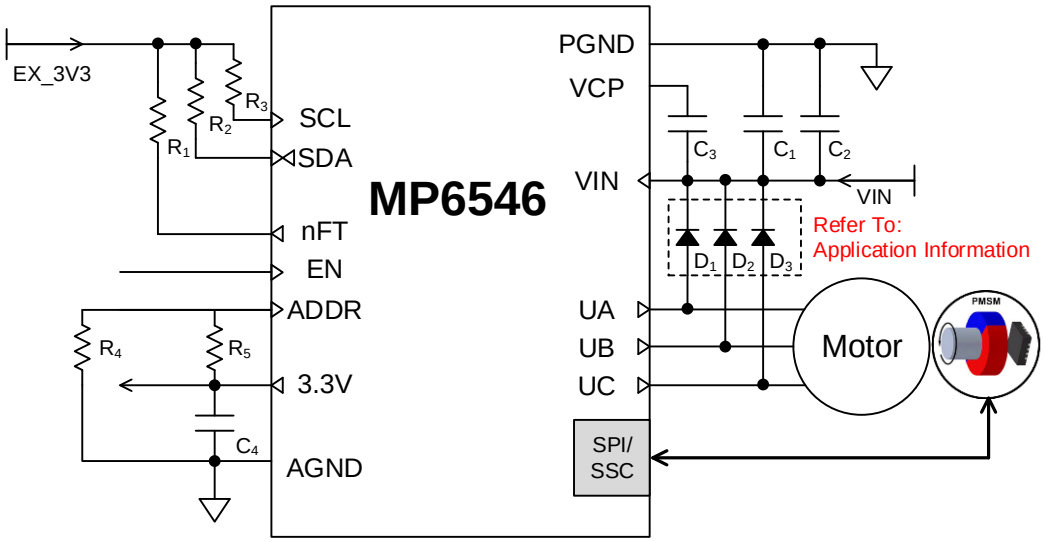
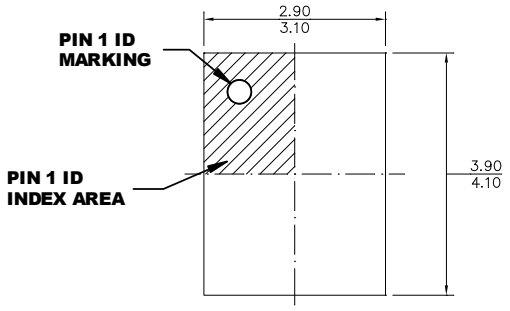


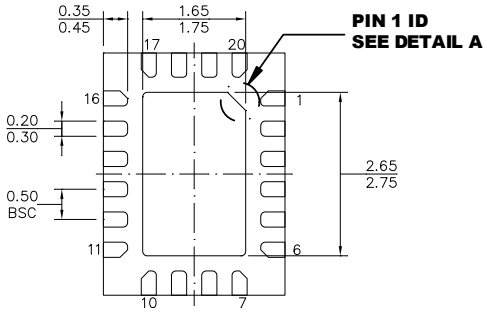
Figure 10: Application with Magnetic Angle Sensor Input

PACKAGE INFORMATION

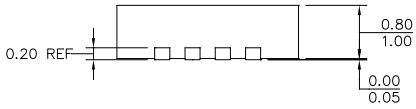
QFN-20 (3mmx4mm)



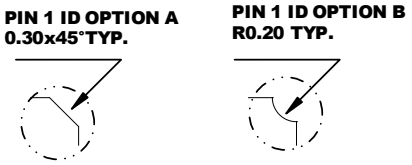
TOP VIEW



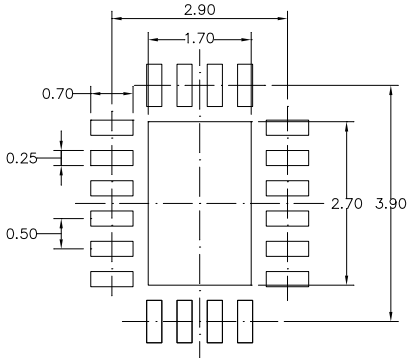
BOTTOM VIEW



SIDE VIEW



DETAIL A

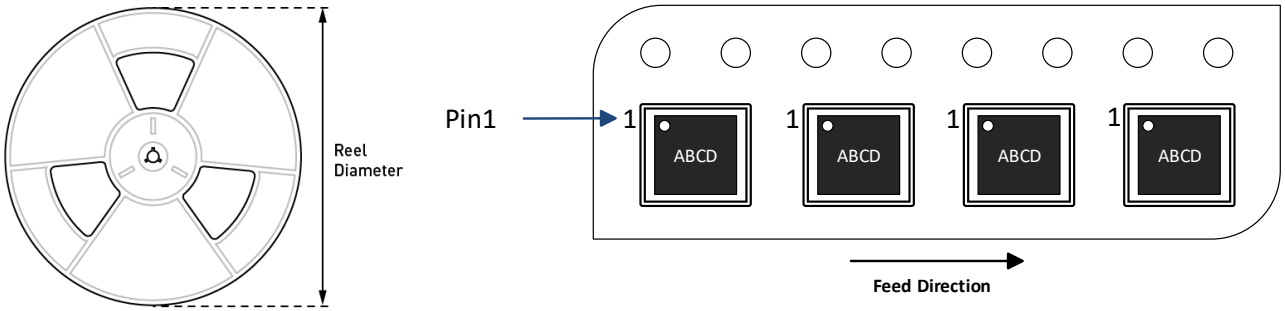


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6546GL-xxxx-Z	QFN-20 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/20/2023	Initial Release	-