MP6612/MP6612D

40V, 5A, H-Bridge DC Motor Driver with Current Sense

DESCRIPTION

The MP6612 and MP6612D are H-bridge motor drivers used for driving reversible motors, which can drive a DC motor, or the winding of a stepper motor or other loads. The H-bridge consists of four N-channel power MOSFETs and an internal charge pump to generate the required gate-drive voltages.

For the MP6612, control of the outputs is accomplished through the IN1 and IN2 pins. For the MP6612D, control of the outputs is accomplished through the DIR and ENBL pins. Otherwise, both parts are identical. References to the MP6612 in this document also apply to the MP6612D unless otherwise noted.

The MP6612 operates on a motor power-supply voltage from 4V to 40V, which can supply an output current (I_{OUT}) up to 5A according to the logic control. Very low standby quiescent current (I_Q) can be achieved when disable the device.

An internal current-sense (CS) circuit provides an output with a voltage proportional to the load current (I_{LOAD}). In addition, the MP6612 provides cycle-by-cycle current regulation and limiting. These features do not require the use of a low-ohmic shunt resistor.

Fault indication and internal shutdown functions are available for over-current protection (OCP), over-voltage protection (OVP), under-voltage lockout (UVLO), and over-temperature protection (OTP).

The MP6612 and MP6612D require a minimal number of readily available, standard external components, and are available in TSSOP-20 with an exposed thermal pad package.

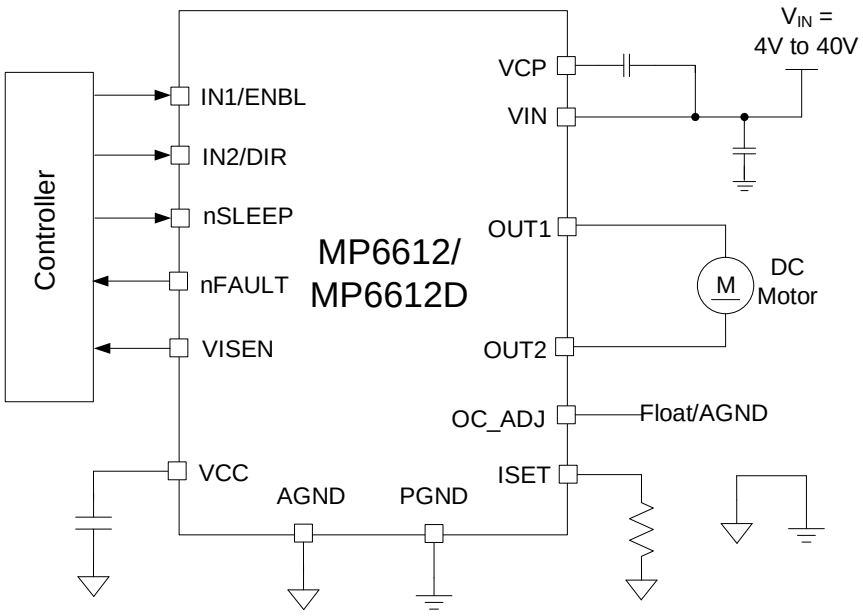
FEATURES

- Wide 4V to 40V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver Supports 100% Duty Cycle with Internal Charge Pump
- Current Sense: 10% Accuracy
- 5A Continuous Driver Current
- Low On Resistance ($R_{DS(ON)}$):
  - 70mΩ High-Side MOSFET (HS-FET)
  - 45mΩ Low-Side MOSFET (LS-FET)
- Cycle-by-Cycle Current Regulation and Limiting
- MP6612: IN1 and IN2 Logic Inputs, MP6612D: ENBL and DIR Logic Inputs
- Low Quiescent Current (I_Q) Brake Mode with Two LS-FETs On
- Configurable Current Limit
- Fault Indication for Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP)
- Available in a TSSOP-20EP Package

APPLICATIONS

- Brushed DC Motor Drivers
- Solenoid Drivers
- Door Locks and Latches

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6612GF*	TSSOP-20EP	*See Below*	2a
MP6612DGF**	TSSOP-20EP	*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MP6612GF-Z).

** For Tape & Reel, add suffix -Z (e.g. MP6612DGF-Z).

TOP MARKING (MP6612GF)

MPSYYWW
MP6612
LLLLLLLLL

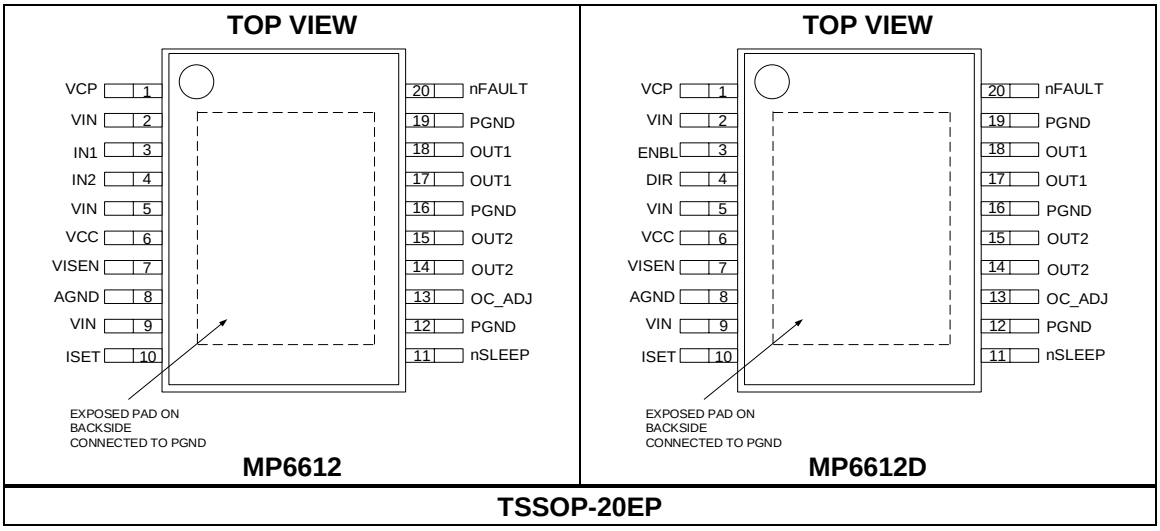
MPS: MPS prefix
YY: Year code
WW: Week code
MP6612: Part number
LLLLLLLLL: Lot number

TOP MARKING (MP6612DGF)

MPSYYWW
MP6612D
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6612D: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



TSSOP-20EP

PIN FUNCTIONS

Pin #	MP6612	MP6612D	Description
1	VCP		**Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor to the VIN pin.
2, 5, 9	VIN		**Input supply voltage.** An input capacitor (C_{IN}) is required to prevent large voltage spikes from appearing at the input.
3	IN1	-	**Input 1.** IN1 is pulled down internally via an internal resistor.
	-	ENBL	**H-bridge enable input.** ENBL is pulled down internally via an internal resistor.
4	IN2	-	**Input 2.** IN2 is pulled down internally via an internal resistor.
	-	DIR	**H-bridge phase input (motor direction).** DIR is pulled down internally via an internal resistor.
6	VCC		**5V LDO output for internal driver and logic.**
7	VISEN		**Current-sense output terminal.**
8	AGND		**Analog ground.** Connect AGND to PGND.
10	ISET		**Current configuration resistor.** Connect a resistor to AGND to set the current limit and the VISEN pin's output voltage. If current limiting is not desired, connect the ISET pin directly to AGND.
11	nSLEEP		**Sleep mode input.** Pull this pin logic high to enable the MP6612; pull it logic low to enter low-power sleep mode. nSLEEP is pulled down internally via an internal resistor.
12, 16, 19	PGND		**Power ground.**
13	OC_ADJ		**Over-current threshold programming pin.** Leave this pin floating or connect it to AGND.
14, 15	OUT2		**Output terminal 2.** Connect OUT2 to the motor winding.
17, 18	OUT1		**Output terminal 1.** Connect OUT1 to the motor winding.
20	nFAULT		**Fault indication.** This pin is an open-drain output. If a fault occurs, it is pulled logic low.
Exposed pad	GND		**Exposed thermal pad.** Connect GND to PGND.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +45V
VCP voltage (V_{CP}).....V_{IN} to V_{IN} + 6.5V
V_{OUTX} .....-0.3V to V_{IN} + 0.3V
PGND to AGND.....-0.3V to +0.3V
All other pins to AGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TSSOP-20EP..... 3.125W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM)..... 1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 40V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4)	***θ_{JA}***	***θ_{JC}***
TSSOP-20EP.....	.....40.....	8…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

4V < V_{IN} < 40V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage (V_{IN})						
VIN operating range	V_{IN}		4		40	V
Turn-on threshold	V_{IN_ON}	V_{IN} rising edge		3	3.8	V
Turn-on hysteretic voltage	V_{IN_HY}			0.3		V
IC Supply						
Shutdown current	I_{SD}	nSLEEP = low			1	µA
Quiescent current	I_Q	Low-I_Q brake mode, OC_ADJ = GND		50	70	µA
		Low-I_Q brake mode, OC_ADJ = floating		35	50	µA
VCC regulator voltage	V_{CC}	V_{IN} > 5.2V, 10mA load	4.75	5	5.25	V
VCC regulator dropout voltage	V_{CCD}	V_{IN} ≤ 5.2V, 10mA load		325		mV
Input Logic (IN1/ENBL, IN2/DIR, nSLEEP)						
Input high voltage	V_{IH}		1.5			V
Input low voltage	V_{IL}				0.4	V
Input high current	I_{IH}	V_{IH} = 5V			50	µA
Input low current	I_{IL}	V_{IL} = 0V	-5		+5	µA
Input pull-down resistance	R_{PD}	IN1/ENBL, IN2/DIR		200		kΩ
		nSLEEP		500		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Switching Frequency (f_{SW})						
Externally applied PWM frequency	f_{PWM}				100	kHz
Power MOSFET						
Output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_A = 25°C	50	70	90	mΩ
		I_{OUT} = 1A, T_J = -40°C to +125°C			180	mΩ
	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_A = 25°C	30	45	65	mΩ
		I_{OUT} = 1A, T_J = -40°C to +125°C			130	mΩ
Minimum on time	t_{MON}			200		ns
Output enable time	t1			70	300	ns
Output disable time	t2			70	300	ns
Delay time	t3			70	300	ns
	t4			70	300	ns
Output rise time	t_{RISE}	R_L = 40Ω		40	150	ns
Output fall time	t_{FALL}	R_L = 40Ω		10	150	ns
IC start-up delay	t_{DELAY}	Enable to switching			500	µs

ELECTRICAL CHARACTERISTICS *(continued)*

4V < V_{IN} < 40V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protections						
Over-current protection (OCP) threshold	I_{OCP}	OC_ADJ = floating	10.5	15	19	A
		OC_ADJ = GND	14.5	20	25.5	A
OCP retry time	t_{OCR}			4		ms
Input over-voltage (OV) threshold	V_{IN_OVP}		45	46.5	48	V
Thermal shutdown	T_{SD}			165		°C
Thermal shutdown hysteresis	T_{SD_HY}			20		°C
Current Control						
Off Time	t_{ITRIP}	After $V_{ITRIP-R}$ is reached		11		µs
ISET current	I_{ISET}		95	100	105	µA/A
Current trip voltage (rising)	$V_{ITRIP-R}$	At the ISET pin	1.44	1.5	1.56	V
Current trip voltage (falling)	$V_{ITRIP-F}$	At the ISET pin	1.15	1.2	1.25	V
VISEN Output						
Output voltage accuracy	ΔV_{VISEN}	V_{ISET} > 0.4V	-5		+5	%

TIMING CHARACTERISTICS DIAGRAM

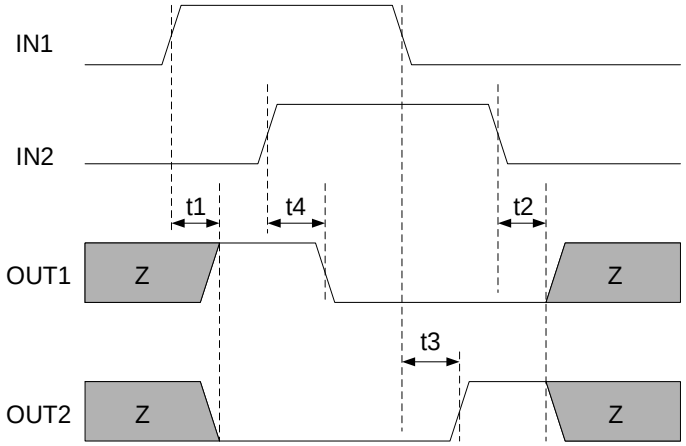
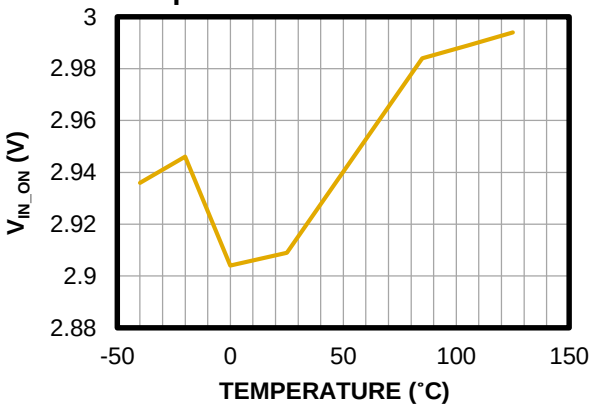


Figure 1: Input/Output Timing Characteristics

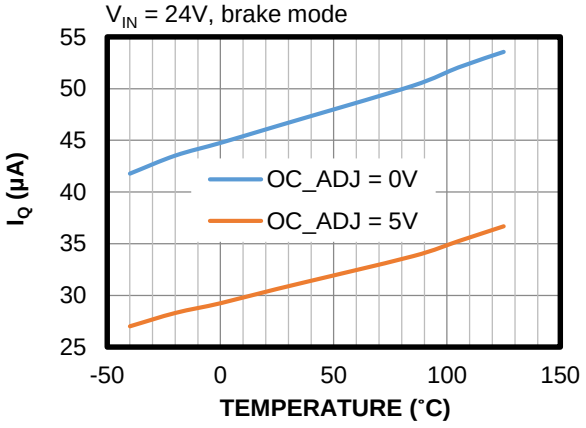
TYPICAL CHARACTERISTICS

Turn-On Threshold vs. Temperature



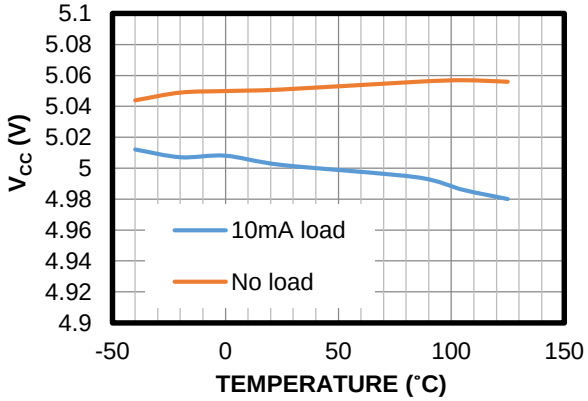
Quiescent Current vs. Temperature

V_{IN} = 24V, brake mode



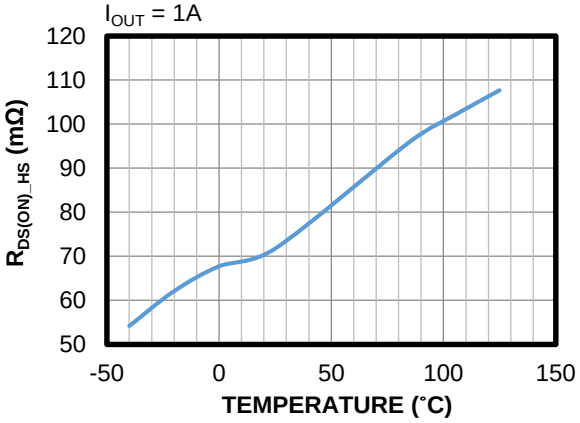
VCC Voltage vs. Temperature

V_{IN} = 24V



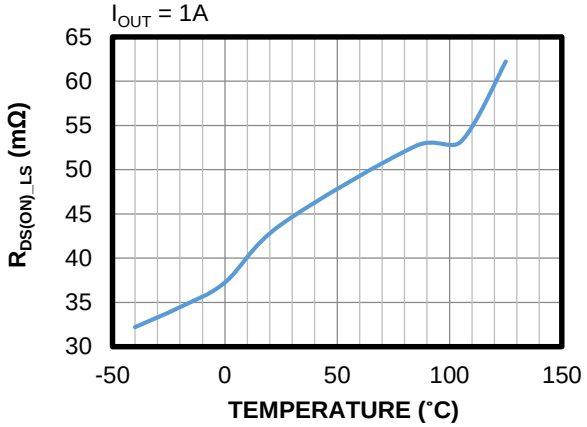
HS-FET On Resistance vs. Temperature

I_{OUT} = 1A

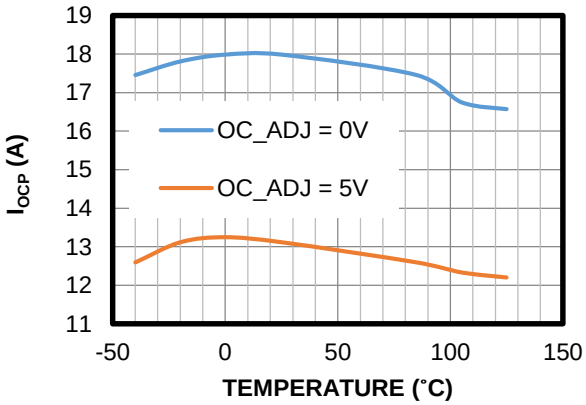


LS-FET On Resistance vs. Temperature

I_{OUT} = 1A



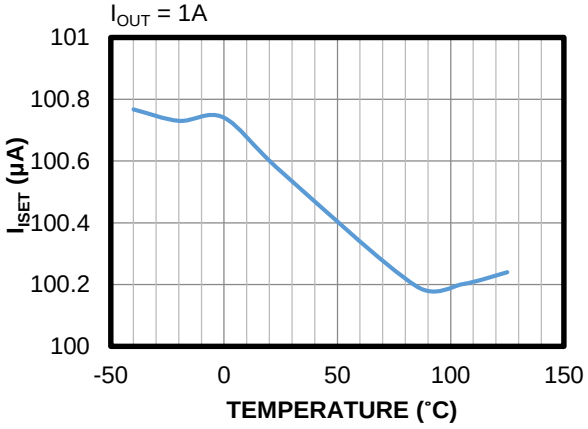
OCP Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

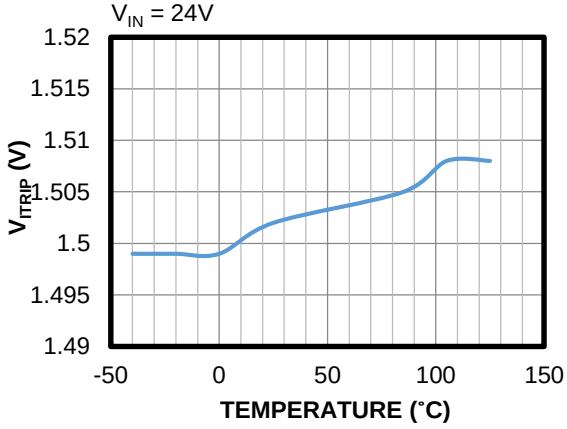
ISET Current vs. Temperature

I_{OUT} = 1A



Current Trip Voltage vs. Temperature

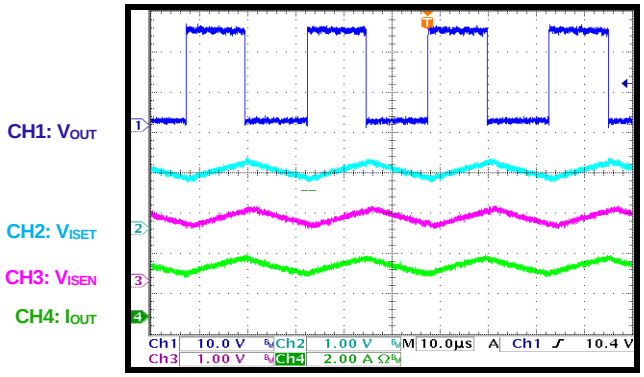
V_{IN} = 24V



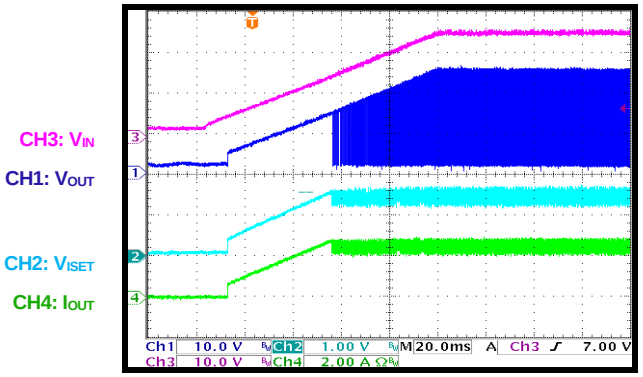
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, IN1 = 5V, IN2 = 0V, I_{OUT} = 3A, T_A = 25°C, resistor + inductor load: 4Ω + 0.2mH between OUT1 and OUT2, unless otherwise noted.

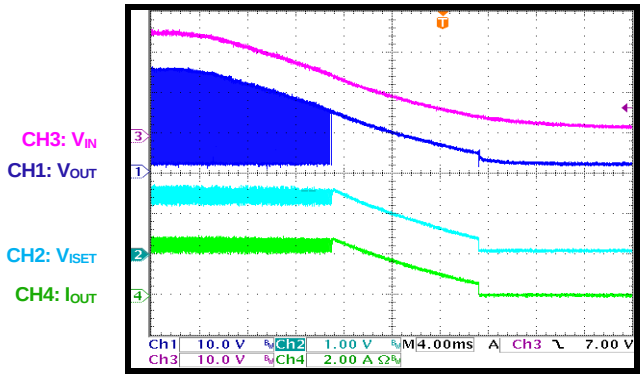
Steady State



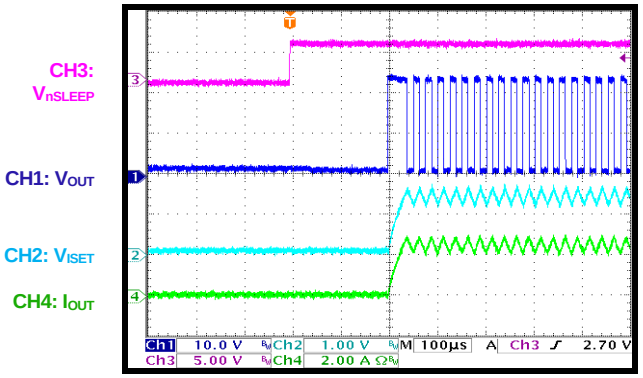
Input Power Start-Up



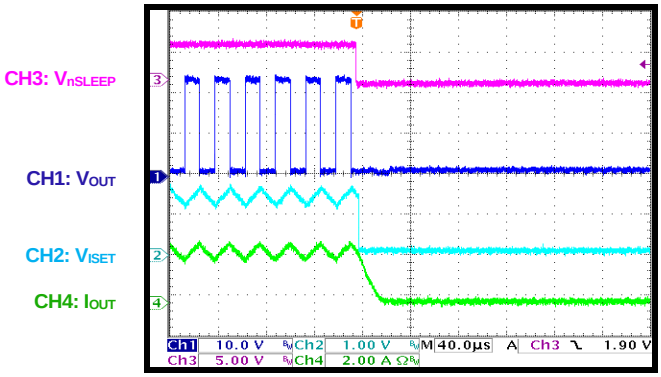
Input Power Shutdown



Sleep Start-Up



Sleep Shutdown



FUNCTIONAL BLOCK DIAGRAM

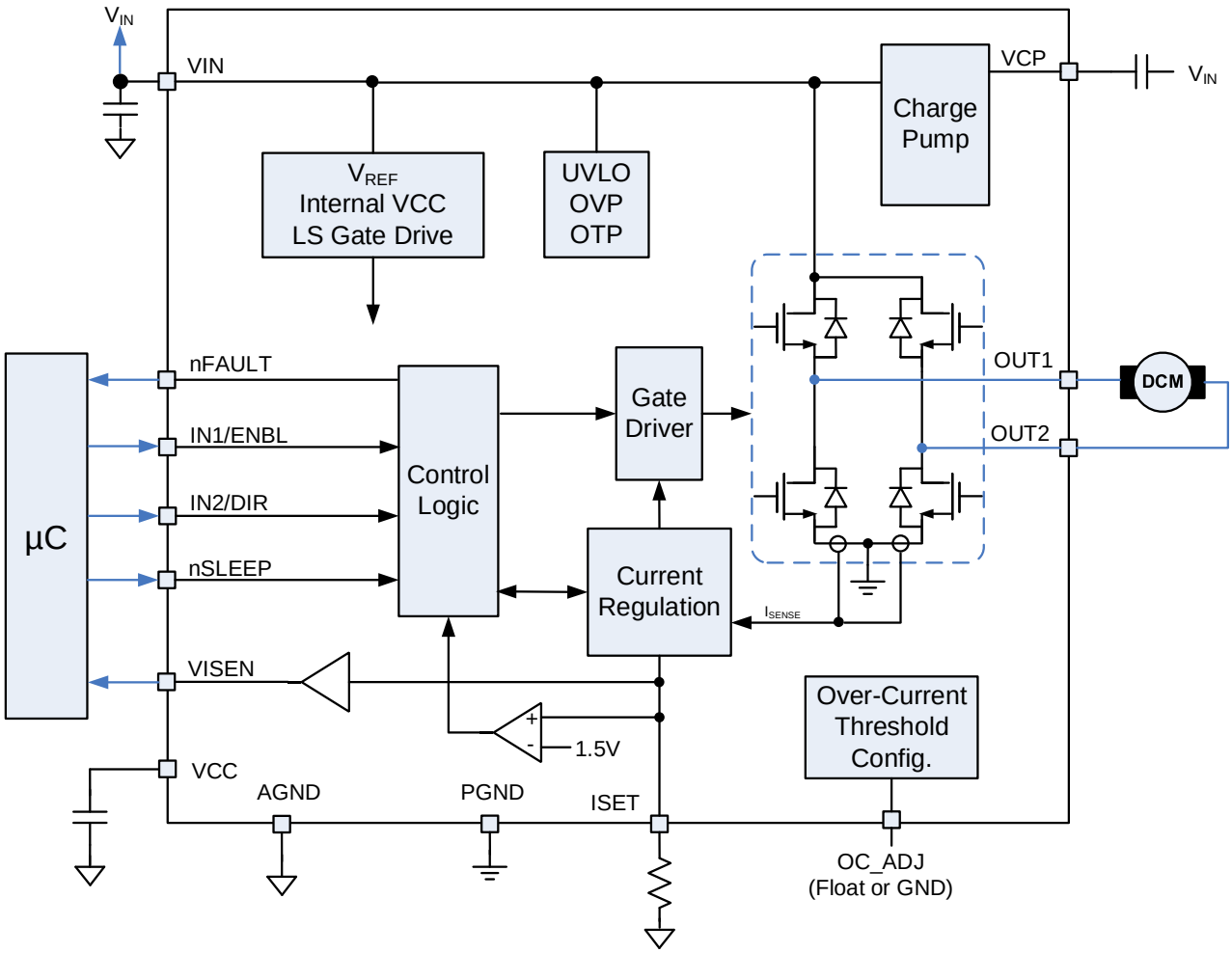


Figure 2: Functional Block Diagram

OPERATION

Bridge Control

The MP6612 is controlled using a pulse-width modulation (PWM) input interface, which is compatible with industry-standard devices. For the MP6612, control of the outputs is accomplished through the IN1 and IN2 pins. Drive both IN1 and IN2 high for about 1ms to force the part to enter low quiescent current (I_Q) brake mode. In this mode, only few internal circuits continue operating to maintain the load brake. Current sense (CS), current limiting, and current regulation functions are disabled, as well as most diagnostic and protection functions. Only output short-to-V_{IN} protection remains enabled, so the part consumes a very small current.

Table 1 shows the control logic for the MP6612.

Table 1: Input Logic Truth Table for MP6612

IN1	IN2	OUT1	OUT2	Function (DC Motor)
L	L	Z	Z	Coast
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

For the MP6612D, control of the outputs is accomplished through the DIR and ENBL pins. Drive ENBL low for about 1ms to force the part to enter low-I_Q brake mode.

Table 2 shows the control logic for the MP6612D.

Table 2: Input Logic Truth Table for MP6612D

ENBL	DIR	OUT1	OUT2	Function (DC Motor)
H	L	L	H	Reverse
H	H	H	L	Forward
L	X	L	L	Brake

Current Sensing

The current flowing in the two low-side MOSFETs (LS-FETs) is sensed with an internal CS circuit. A voltage proportional to the output current (I_{OUT}) is sourced on the VISEN pin.

The VISEN output voltage scaling is set by a resistor (R_{ISET}) connected between the ISET pin and ground. For 1A of I_{OUT}, 100μA of current is sourced into the resistor connected to ISET. For example, if a 5kΩ resistor is used, the output voltage on the VISEN pin is 0.5V/A of I_{OUT}. Current is sensed any time one of the LS-FETs is turned on, including in slow decay (brake) mode.

The load current applied to the VISEN pin ($I_{VISEN-LOAD}$) should be kept below 2mA, with no more than 500pF of capacitance.

Current Limiting and Regulation

The current in the outputs is regulated using constant-off-time PWM control circuitry (see Figure 3).

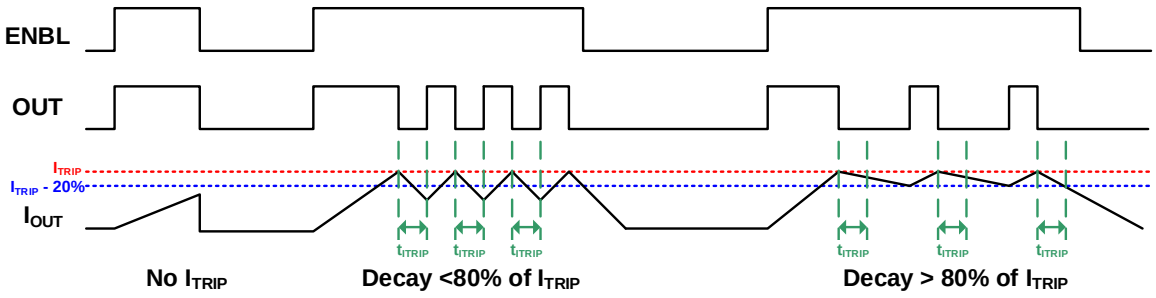


Figure 3: Current Limit Operation

The current limiting and regulation process is described below:

- Initially, a diagonal pair of MOSFETs turns on and drives current through the load.
- I_{OUT} increases, which is sensed by the internal CS circuit.
- If I_{OUT} reaches the current trip voltage threshold ($V_{ITRIP-R}$), the H-bridge switches to slow decay mode, with the two LS-FETs turned on.
- After a fixed off time (t_{ITRIP}), if I_{OUT} drops below 80% of $V_{ITRIP-R}$, the diagonal pair of MOSFETs are re-enabled and the cycle repeats.

- If I_{OUT} remains above 80% of VITRIP-R, the off time (t_{OFF}) is extended until I_{OUT} drops below 80% of $V_{ITRIP-R}$.

$V_{ITRIP-R}$ is reached when the ISET pin reaches 1.5V. As an example, with a 5kΩ resistor connected from ISET to ground, the ISET voltage (V_{ISET}) is 0.5V/A of I_{OUT}. Therefore, when the current reaches 3A, V_{ISET} reaches 1.5V and a current trip occurs.

For DC motors, current regulation is used to limit the motor's start-up and stall currents. Speed control is typically performed by providing an external PWM signal to the input pins.

If the current regulation feature is not needed, it can be disabled by connecting the ISET pin directly to GND.

During current regulation, the nFAULT pin is not active.

Blanking Time

There is often a current spike during the MOSFET turn-on time due to the body diode's reverse-recovery current or the shunt capacitance of the load. This current spike requires filtering to prevent the MOSFET from erroneously shutting down. An internal fixed blanking time (t_{MON}) blanks the CS comparator's output when the MOSFET turns on. This blanking time also sets the MOSFET's minimum on time.

nSLEEP Operation

Drive nSLEEP low to put the device into a low-power sleep state. In this state, the H-bridge outputs are turned off, all related internal circuits — including the gate drive charge pump — are disabled, and all inputs are ignored. When waking up from sleep mode, there is a delay time (t_{DELAY}) before the outputs begin operating.

Protection Circuits

The MP6612 is fully protected against over-current (OC), over-temperature (OT), under-voltage (UV), and over-voltage (OV) events.

Over-Current Protection (OCP)

The MP6612 features internal short-circuit protection (SCP). The currents in both the high-side MOSFETs (HS-FETs) and LS-FETs are measured. If the current exceeds the over-current protection (OCP) threshold (I_{OCP}), all MOSFETs in the H-bridge are turned off. After approximately 4ms, the bridge is re-enabled automatically.

I_{OCP} is specified by OC_ADJ (see Table 3).

Table 3: Over-Current Threshold

OC_ADJ	Min OC Threshold
Float	10.5A
GND	14.5A

Over-Temperature Protection (OTP)

Thermal monitoring is also integrated into the MP6612. If the die temperature exceeds safe limits, all MOSFETs turn off and the nFAULT pin is driven low. Once the die temperature has fallen to a safe level, operation automatically resumes.

Under-Voltage Lockout (UVLO)

If at any time V_{IN} falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled and the internal logic is reset. Once V_{IN} rises above the UVLO threshold, the MP6612 restarts and resumes normal operation.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the input over-voltage threshold (V_{IN_OVP}), the device is disabled. Once V_{IN} drops to a safe level, the MP6612 restarts resumes normal operation.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the supply bypass capacitor and charge pump capacitor as close to the IC as possible. Each VIN pin should have a bypass capacitor.
2. Connect OUT1 (pins 17 and 18) and OUT2 (pins 14 and 15) to the pads of the chip.
3. Use large copper areas for PGND, VIN, OUT to improve thermal performance.
4. The thermal pad should be soldered directly to copper on the PCB.
5. Use thermal vias to transfer heat to other layers of the PCB. Add as many vias as possible to improve thermal dissipation.

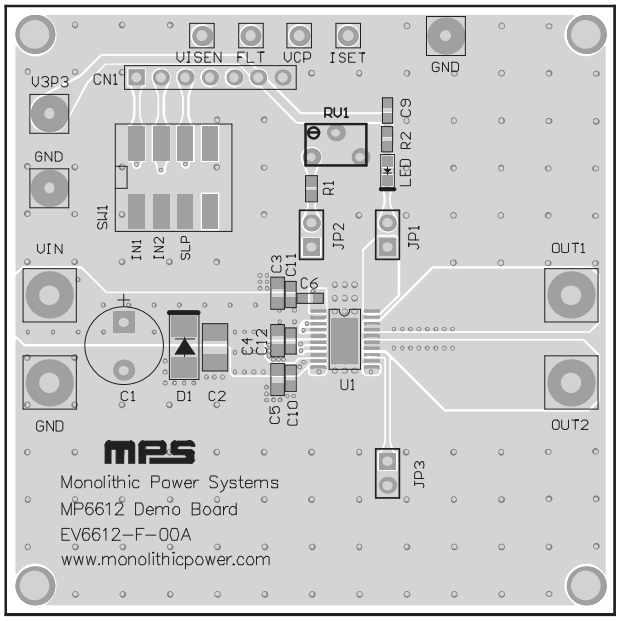


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

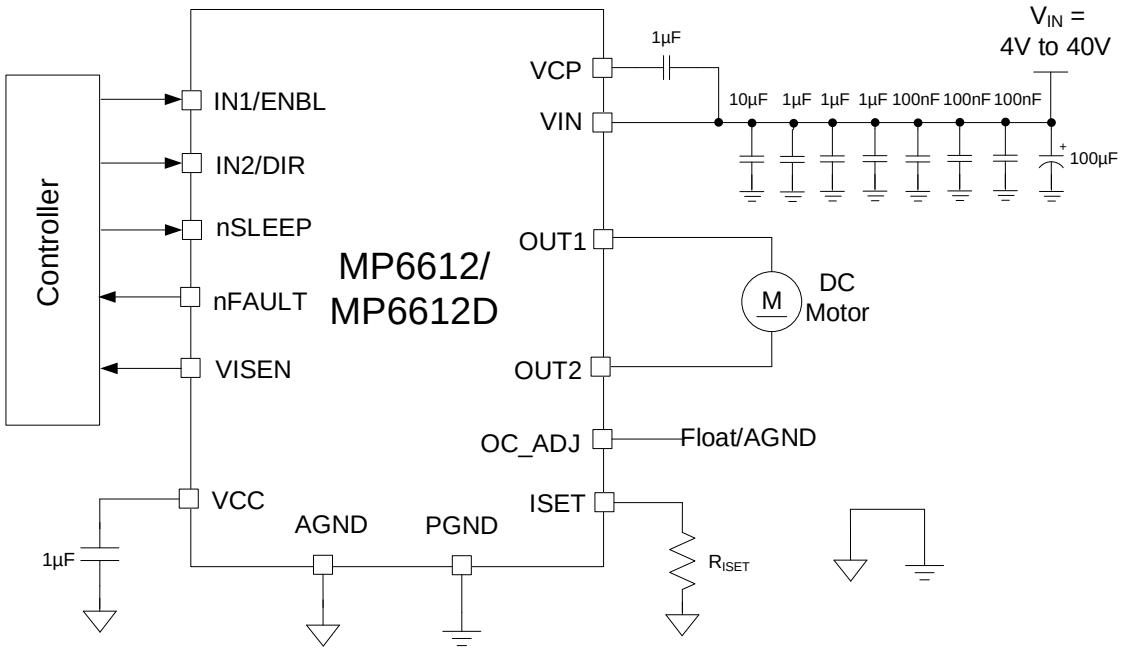
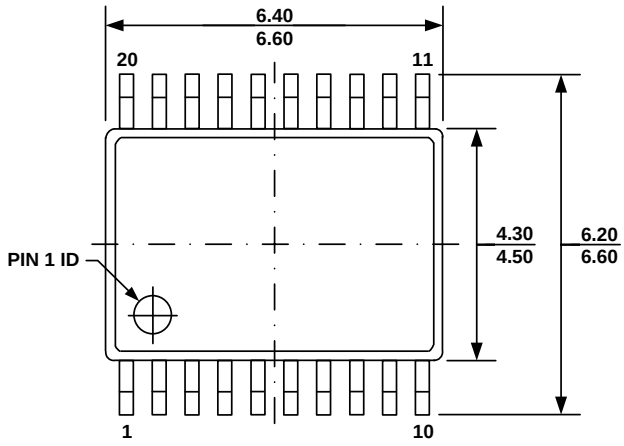


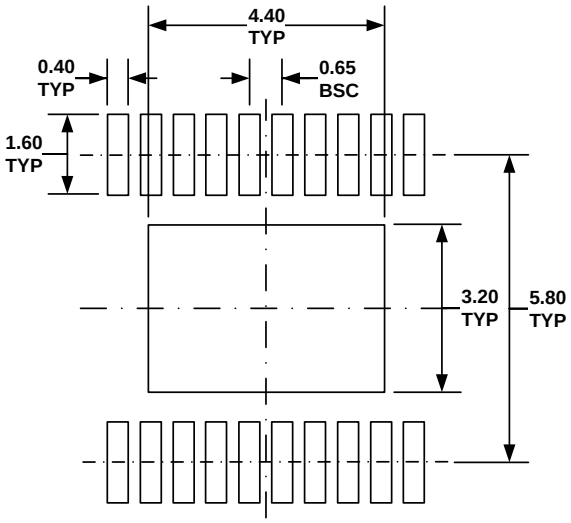
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

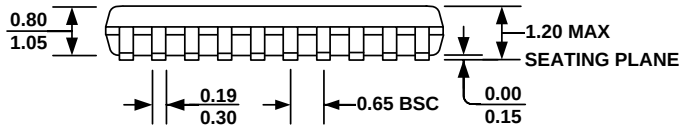
TSSOP-20EP



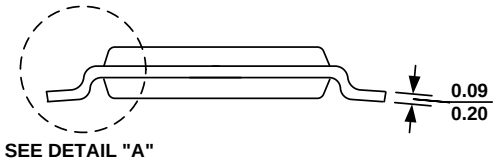
TOP VIEW



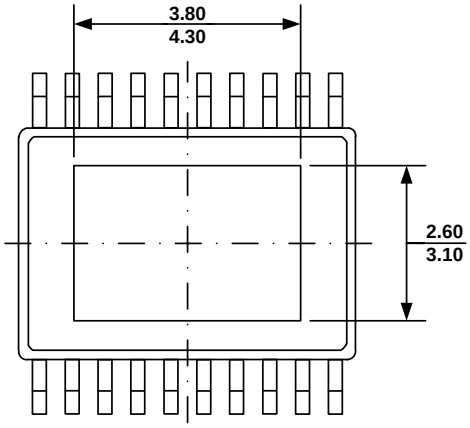
RECOMMENDED LAND PATTERN



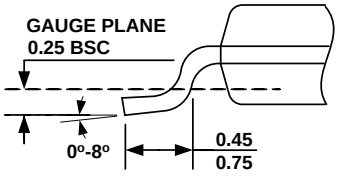
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

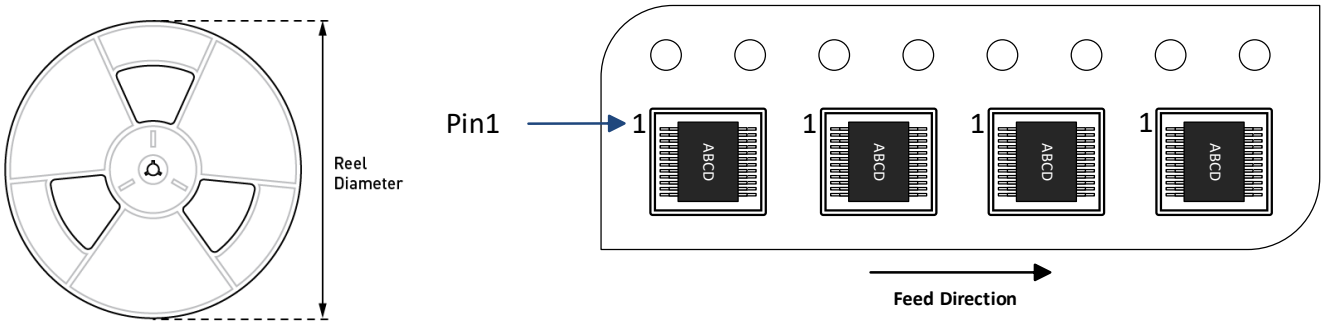


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6612GF-Z*	TSSOP-20EP	2500	75	N/A	13in	16mm	8mm
MP6612DGF-Z**	TSSOP-20EP						

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/14/2023	Initial Release	-