The Future of Analog IC Technology

MP6616

2A Single Phase BLDC Driver with Integrated Hall Sensor

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP6616 is a single-phase brushless DC motor driver with integrated power MOSFETs and Hall Effect Sensor. It drives single-phase brushless DC motor motors, with up to 2A operation output current. The input voltage ranges from 3.3V to 18V.

The MP6616 controls the motor speed through the PWM signal on PWM pin with close loop control, built-in programmable speed curve function. It features programmable soft on/off phase transition and Hall angle trimming over full speed range which can flexibly optimize low speed and high speed performance.

The MP6616 also has the rotational speed detector feature. The rotational speed detector (the FG pin) is the output of an open drain collector. It outputs a high or low voltage relative to the internal Hall comparator's output. In addition direction control is also achieved through DIR pin input.

Rich protection includes input over-voltage protection, under-voltage Lockout, locked-rotor protection, over-current protection, and thermal shutdown protection.

The MP6616 is available in a QFN10-2x3mm package.

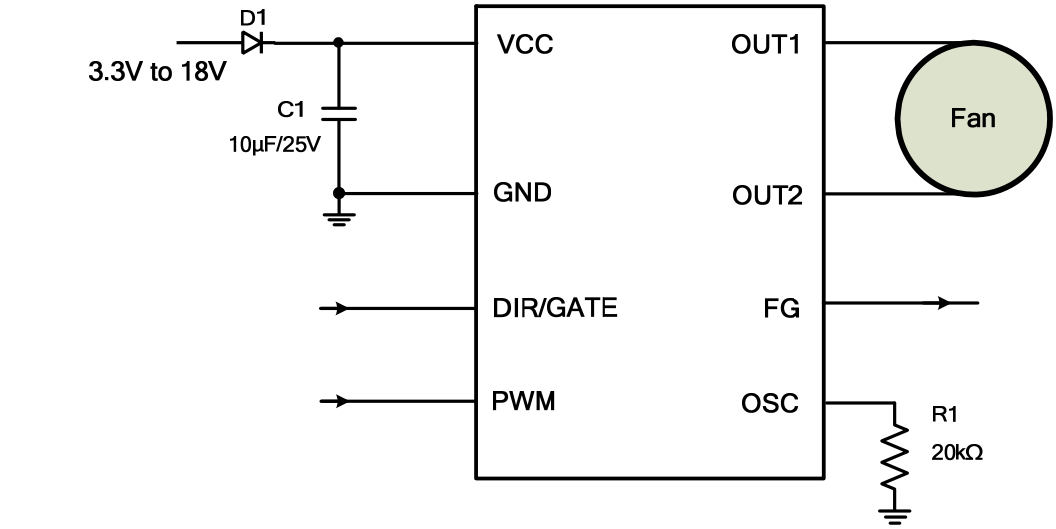
FEATURES

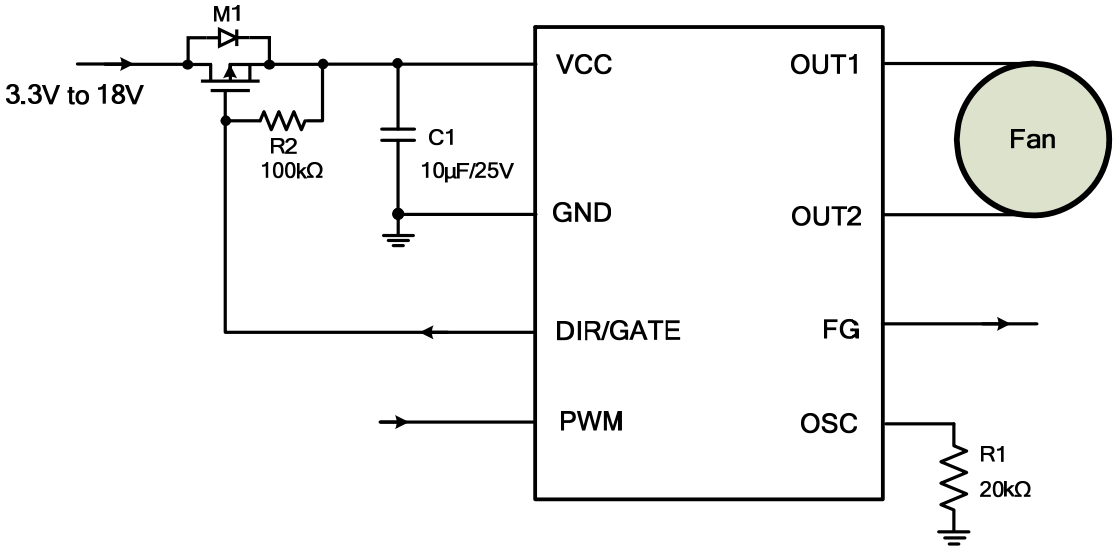
- On chip hall sensor (2mT min. sensitivity)
- Wide 3.3V to 18V operating input range
- 2A continuous driver current
- Integrated power MOSFETs: total 100mΩ (HS+LS)
- Programmable speed curve
- Max. 40000 rpm programmable speed
- Programmable min. speed and PWM in duty
- Close-loop control or mix mode selectable
- High speed accuracy @close-loop mode
- Programmable soft on/off phase transition angle, max. 45^{o}
- Programmable Hall trimming angle, max. $\pm 45^{o}$
- 4-step programmable current limit, max. 4A
- Rotor-lock protection
- 2KHz to 100KHz PWM input range
- 2.4s to 19.2s programmable soft start time
- Fixed 27KHz output switching frequency
- Input-line reverse connection protection gate signal
- Rotor lock protection and auto. recovery
- Thermal protection and auto. recovery
- Built-in input OVP, UVLO and automatic recovery
- Available in a QFN10-2x3mm Package

APPLICATIONS

- Personal Computers or CPU Fan
- 1U&2U Server Fan

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6616GD	QFN-10 (2mmx3mm)	*See Below*

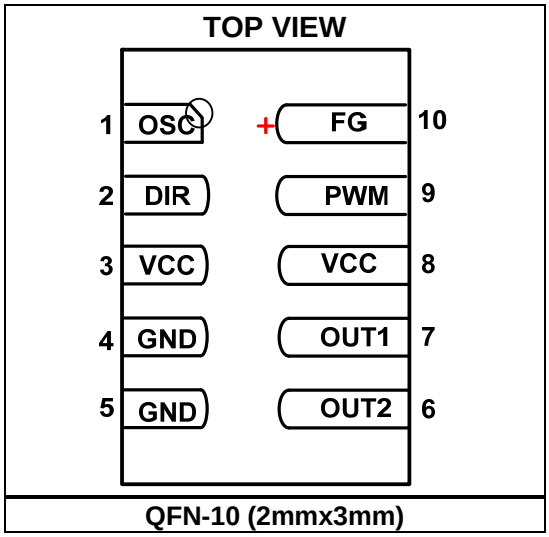
* For Tape & Reel, add suffix –Z (e.g. MP6616GD–Z)

TOP MARKING

BEPY
LLL

BEP: product code of MP6616GD
Y: year code
LLL: lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{CC} .....–0.7V to +25V
FG, PWM, $V_{OUT1/2}$.....–0.3V to V_{CC}+0.3V
All Other Pins.....–0.3V to +6.5 V
Continuous Power Dissipation (T_A = +25°C) (2) ..
FCQFN10 ..... 1.9W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -60°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} .....3.3V to 18V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (2mmx3mm)	65	12 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_J = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol		Min	Typ	Max	Units
Input UVLO Rising Threshold	V_{UVLO}			3		V
Input UVLO Hysteresis				0.15		V
Operating Supply Current	I_{CC}			5		mA
PWM Input High Voltage	V_{PWMH}		1.5			V
PWM Input Low Voltage	V_{PWML}				0.4	V
PWM Input Internal Pull-high Resistance				100		kΩ
HS Switch-On Resistance	R_{HSON}	I_O=100mA		50		mΩ
LS Switch-On Resistance	R_{LSON}	I_O=100mA		50		mΩ
Cycle-Cycle Current Limit	I_{OCP}	Full scale	-20%	4	+20%	A
Short Circuit Current Limit	I_{LMT}	Full scale	-20%	6.5	+20%	A
PWM Output Frequency	fs	R_{OSC}=20kΩ	-1%	27	+1%	kHz
FG Output Low-level Voltage	VFG_L	IFG/RD=3mA, V_{PULL}=5V			0.35	V
Soft Turn On Angle at 100% PWM Out Duty	θ_{son}	SON=11111		45		deg
Soft Turn Off Angle at 100% PWM Out Duty	θ_{soff}	SON=11111		45		deg
Rotor-Lock Detection Time	T_{RD}			0.6		s
Minimum Recommended Magnetic Field					±2	mT
Thermal Shutdown Threshold(5)			150	160	180	°C
Thermal Shutdown Hysteresis(5)				40		°C

Note:

5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VCC} = 12V, T_A = 25°C, unless otherwise noted.

TBD

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{VCC} = 12V, T_A = 25°C, unless otherwise noted.

TBD

PIN FUNCTIONS

QFN Pin #	Name	Description
1	OSC	Internal Oscillator Setting Pin. Connect a 1% accuracy resistor between this pin to ground.
2	DIR/GATE	Programmable for: • Rotational Direction Control pin. • PMOS Gate Signal for Reverse Connection MOSFET.
3,8	VCC	Input Power Pin.
4,5	GND	Ground.
6	OUT2	Motor Driver Output 2. It is low state during the Hall High Logic.
7	OUT1	Motor Driver Output 1. It is low state during the Hall Low Logic.
9	PWM	PWM Input Pin for Speed Control. 2KHz to 100kHz PWM is recommended in normal operation. I^2C Interface Data (SDA) Pin in Test Mode.
10	FGRD	Selectable for Speed Indication or Rotor Lock Indication. I^2C Interface Clock (SCL) Pin in Test Mode.

OPERATION

The MP6616 is a single-phase brushless DC motor driver with integrated power MOSFETs and Hall Effect sensor. The MP6616 controls the motor speed through the PWM signal on PWM pin with close/open loop control, built-in programmable speed curve function. It features programmable soft on/off phase transition and Hall angle trimming over full speed range which can flexibly optimize low speed and high speed performance.

The MP6616 also has the rotational speed detector feature. The rotational speed detector (the FG pin) is the output of an open drain collector. It outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection includes input over-voltage protection, under-voltage Lockout, locked-rotor protection, over-current protection, and thermal shutdown protection.

Speed Control

The PWM signal on PWM Pin accepts wide input frequency range (2kHz to 100kHz). IC adjusts motor speed by detecting the PWM signal duty cycle. Close loop and mix mode are supported.

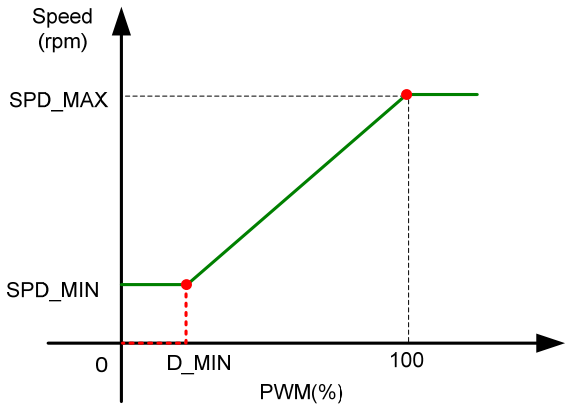
- Close Loop Mode (**DIN_OPEN = 0xFF**)

In this mode, IC internally detects the hall signal speed and feedbacks to the control loop which adjusts the output PWM duty in close loop. By doing this, the motor speed follows the reference exactly. The speed reference vs. PWM input duty is set shown as below.

The max. speed (rpm) is set by **SPD_MAX** register corresponding to 100% duty cycle. The min. speed (rpm) is set by **SPD_MIN** register corresponding to the value set by register **DIN_MIN**. When PWM input duty is lower than the duty set by **DIN_MIN**, the fan speed supports two modes,

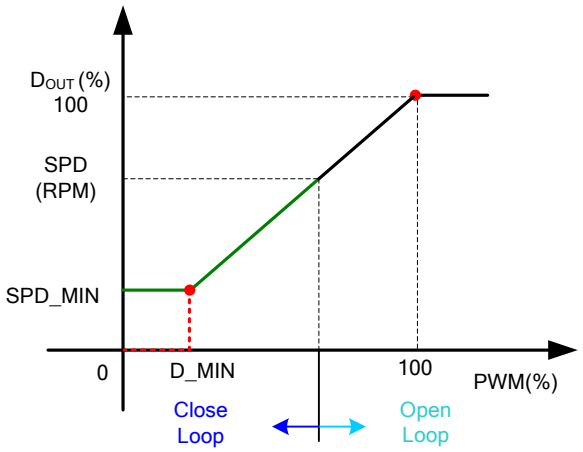
1) The speed keeps the value set by **SPD_MIN** when **SPD_ZERO** is set to 0.

2) The speed keeps 0 when **SPD_ZERO** is set to 1.



- Mixed Mode

The register **DIN_OPEN** set the boundary of open-loop control and close loop control, when the PWM duty cycle is lower than DIN_OPEN, IC works in close loop, when PWM duty cycle is larger than **DIN_OPEN**, the motor speed transfers to open loop control mode.



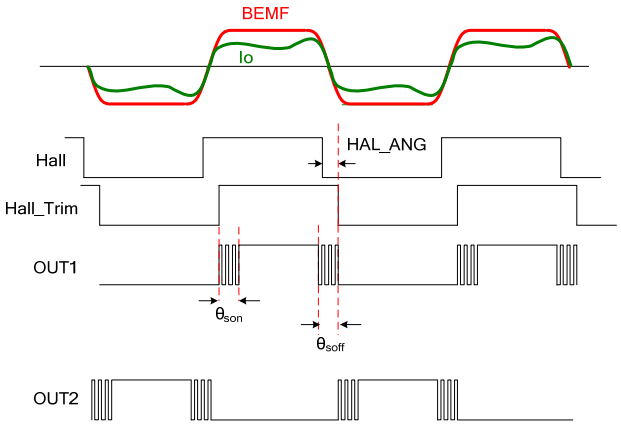
OUT1/2 Normal Operation

In normal operation, MP6616 controls H-bridge MOSFETs switching according to below timing figure to reduce speed variation and increase system efficiency.

All operation sequence is based on the Hall signal coming from the embedded hall sensor. Hall_Trim is the trimming signal, max. 45° phase shift, which is generated based on Hall signal. When Hall_Trim signal is high, OUT2 keeps constant low while OUT1 is switching phase. When Hall_Trim signal is low, OUT1

keeps constant low while OUT2 is switching phase. In addition, the phase shift angle is separately setting dependent on PWM input duty cycle.

- The trimming angle is dependent on **HAL_ANG1** when input duty is lower than the value (**DIN_HAL_L/64**) set by **DIN_HAL_L.**
- The trimming angle is dependent on **HAL_ANG2** when input duty is between the value (**DIN_HAL_L/64**) set by **DIN_HAL_L** and the value (**DIN_HAL_H**/64) set by **DIN_HAL_H**.
- The trimming angle is dependent on **HAL_ANG3** when input duty is higher than the value (**DIN_HAL_H/64**) set by **DIN_HAL_H.**
- The phase shift leading/lag direction is set by **HAL_FLAG**



Soft Turn-on Section:

During this time, the switching phase duty cycle gradually increases from 0 to steady duty. transition phase time is 45° which is set by **SON_ANG**. The resolution is 1.45°.

Soft Turn-off Section:

During this time, the switching phase duty cycle gradually decreases from steady duty to 0, max. transition phase time is 45° which is set by **SOFF_ANG**. The resolution is 1.45°.

Soft Start Time

To reduce the input inrush current during startup, MP6616 provides programmable soft start time of speed reference by setting register bits **TIME_SS**. From 2.4s to 19.2s programmable time is supported.

Notice that, the **TIME_SS** is ramp-up-down time of the speed reference in close-loop mode.

Reverse Current Detection

To avoid current stored in motor charging back to input side, IC has reverse current detection function. During soft off time, when negative current is detected, both high side and low side MOS of switching phase is turned off. This function can be enabled or disabled by setting **RVSI_EN** bit.

Direction Control

The motor rotational direction is controlled by DIR pin, pull DIR high, motor is in reverse rotation, pull DIR pin low, motor is in forward rotation.

DO NOT change rotational direction while motor is rotating. Waiting motor stop rotating before change the direction.

Close Loop Integrator Gain

In close loop mode, the close loop integrator gain is dependent on **KI_TIMER**[1:0] and **ERR_GAIN**[1:0].

KI_TIMER[1:0] Setting:

- **KI_TIMER = 00:** the integrator refresh timer is 9.3ms;
- **KI_TIMER = 01:** the integrator refresh timer is1.2ms;
- **KI_TIMER = 10:** the integrator refresh timer is 150us;
- **KI_TIMER = 11:** the integrator refresh timer is 19us;

ERR_GAIN[1:0] Setting:

- **ERR_GAIN = 00:** the integrator gain co-efficient is 1/8;
- **ERR_GAIN = 01:** the integrator gain co-efficient is 1/4;
- **ERR_GAIN = 10:** the integrator gain co-efficient is 1/2;
- **ERR_GAIN = 11:** the integrator gain co-efficient is 1.

The higher timer frequency or gain-coefficient leads to the higher loop response when the loop is steady.

Oscillator Frequency Setting

To provide accurate clock timing for speed control, a high accuracy resistor with 20kΩ value needs to connected between OSC pin and ground. The internal high frequency oscillator is fixed to 7MHz and switching frequency is around 27KHz.

Digital Oscillator Frequency

The oscillator f_{osc_d} used for digital block including all hall angle calculation and close loop calculation is selected through **SPD_SEL** bits. Higher frequency leads to higher calculation resolution but causes higher min. speed.

SPD_SEL = 0:

Digital oscillator is 7MHz/64, min. supported speed is 100 r/min.

SPD_SEL = 1:

Digital oscillator is 7MHz/16, min. supported speed is 400 r/min.

SPD_SEL = 2:

Digital oscillator is 7MHz/8, min. supported speed is 800 r/min.

SPD_SEL = 3:

Digital oscillator is 7MHz/4, min. supported speed is 1600 r/min.

Cycle-Cycle Over Current Protection (OCP)

During normal switching, if the current flowing through the highs side MOSFET of the H-bridge exceeds the threshold setting by register bits **OCP_SEL** after around 1us blanking time, the high side MOSFET turns off immediately. It resumes to normal switching in the next switching cycle. The over load current limit threshold has 4 programmed values up to 4A.

Speed Detection

The FG signal on FGRD pin outputs internal hall change signal for speed indication. Different FG signal frequency is provided including 1X, 1/2X and 1/4X hall frequency. This is selected by setting **FGRD_SEL** bit to 00/01/10.

FGRD is an open drain collector and needs to be pulled high when normal operation.

Rotor Dead Lock Protection (RD)

In motor rotor lock cases, MP6616 shuts down all power MOSFETs if hall signal edge is not changed during 0.6s detection time, all MOSFETs of H-bridge are turned off and auto restarts after the recovery time set by register bits **LOCK_SEL**. By setting **FGRD_SEL** bit to 11, the signal on FGRD pin is selected to rotor lock indication. During rotor lock fault status, the signal keeps high by setting **RD_H_L** bit to 1 while the signal keeps low by setting **RD_H_L** bit to 0.

Over-Voltage Protection (OVP)

If VCC pin voltage exceeds over-voltage threshold 16V, IC turns off high-side bridge MOSFETs and turns on low-side bridge MOSFETs. Then IC resumes to normal operation after VCC drops blow 15V.

Thermal Shutdown (TSD)

Thermal monitoring of MP6616 die is also provided. If the die temperature rises above 160°C, the MOSFETs of switching half-bridge turn off. Once the die temperature has drops lower than 120°C, operation automatically resumes.

Under-Voltage Lockout (UVLO)

When the voltage on VCC pin falls below the under-voltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when VCC rises above the UVLO threshold.

Pre-Startup Timer

With VCC powered, IC first increases output duty cycle gradually before the speed is taken over PWM duty cycle, triggered by timer set by DUTY_SLOPE[1:0] bits. This is used to avoid startup current when fan is in stand-still and to provide robust startup mode.

- DUTY_SLOPE = 0: Timer period is 18.6ms.
- DUTY_SLOPE = 1: Timer period is 9.3ms.
- DUTY_SLOPE = 2: Timer period is 4.6ms.

- DUTY_SLOPE = 3: Timer period is 2.3ms

Higher timer period leads to lower soft pre-start current but causes longer pre-startup time.

Debug Mode

The register can be programmed in debug mode. In debug mode, PWM and FGRD pin can be used as I^2C interface to read/write internal register. IC exits debug mode and returns to normal PWM/FG mode when either below condition is met.

- IC exits debug mode by write **DEBUG** to 1 through I2C.
- Reset power supply VCC.

Suggest to use MPS GUI software for easy debugging.

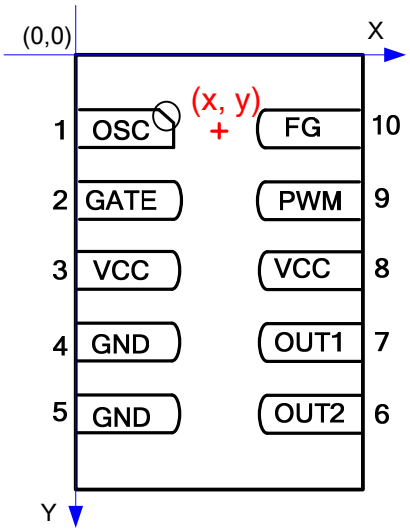
OTP Program

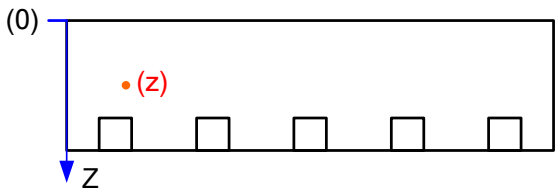
MP6616 provides two times non-volatile memory programming for parameters store. After design finalized, the OTP programming is done as below sequence,

1. Writing 1 to **OTP_EN** register bit in debug mode.
2. Then writing 1 to **PG_EN** register bit in debug mode.

Embedded Hall Position

The embedded hall position of MP6616 is as follow





Here, x=1003±40μm, y=620±40μm, z=370±40μm.

I²C Chip Address:

After the START condition, the I²C-compatible master sends a seven-bit address followed by an eighth read (Read: 1) or write (Write: 0) bit. The following bit indicates the register address to/from which the data will be written/read. The I2C address is 0x17

0	0	1	0	1	1	1	R/W

The I²C Compatible Device Address

Register Mapping:

Add	D7	D6	D5	D4	D3	D2	D1	D0
00H	NA	SPD_SEL[1:0]		Reserved				
01H	SPD_MAX[7:0]							
02H	SPD_MAX[15:8]							
03H	SPD_MIN[7:0]							
04H	DIN_MIN[7:0]							
05H	DIN_OPEN[7:0]							
06H	TIME_SS[2:0]			RVSI_EN	KI_TIMER[1:0]		ERR_GAIN[1:0]	
07H	SPD_ZERO	OCP_SEL[1:0]		SON_ANG [4:0]				
08H	RD_H_L	LOCK_SEL[1:0]		SOFF_ANG [4:0]				
09H	DEBUG	OTP_EN	HAL_FLAG	HAL_ANG1[4:0]				
0AH	PINMOD[1:0]		Reserved	HAL_ANG2[4:0]				
0BH	DUTY_SLOPE[1:0]		Reserved	HAL_ANG3[4:0]				
0CH	FGRD_SEL[1:0]		DIN_HAL_L[5:0]					
0DH	PG_EN	TRIM_EN	DIN_HAL_H[5:0]					
0FH	OTP_PAGE[1:0]		Reserved					

BLOCK DIAGRAM

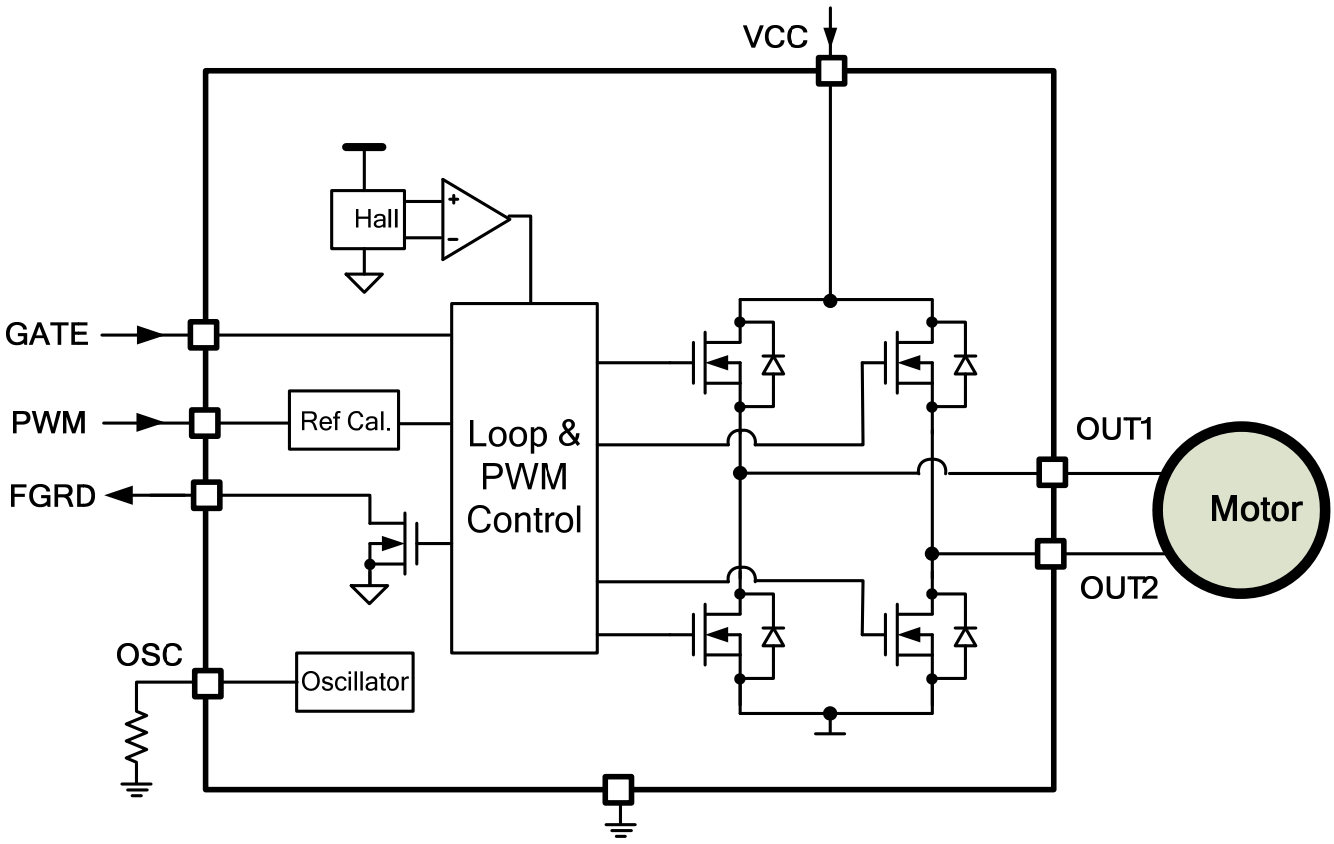
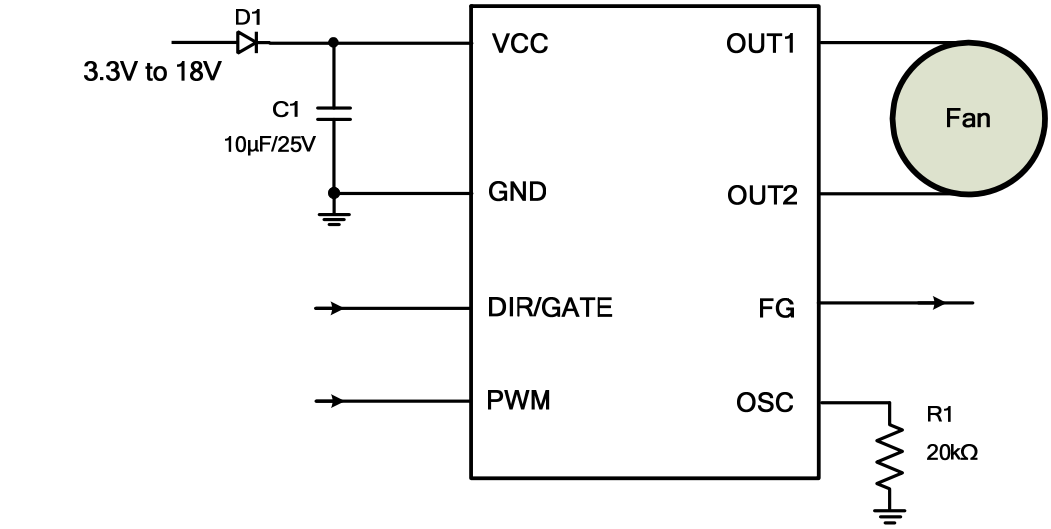
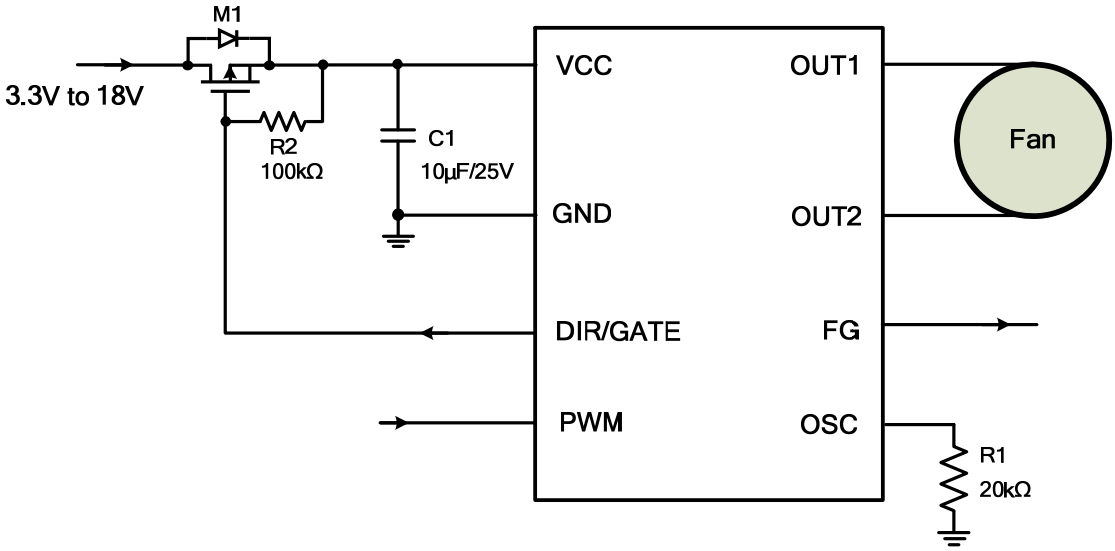


Figure 1: Functional Block Diagram

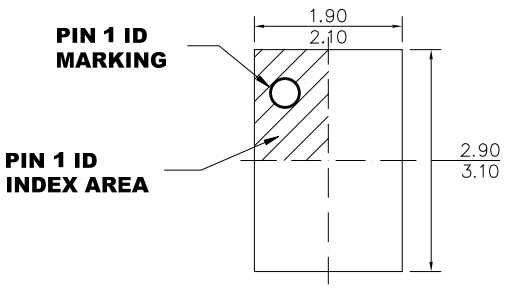
TYPICAL APPLICATION



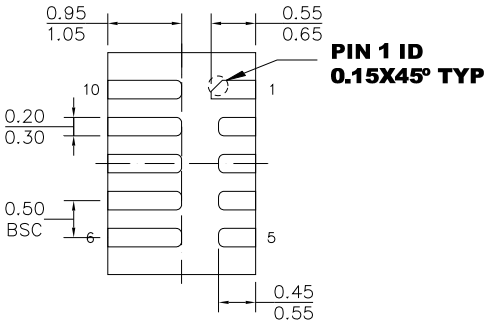


PACKAGE INFORMATION

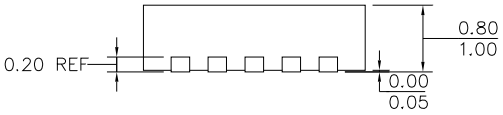
QFN-10 (2mmx3mm)



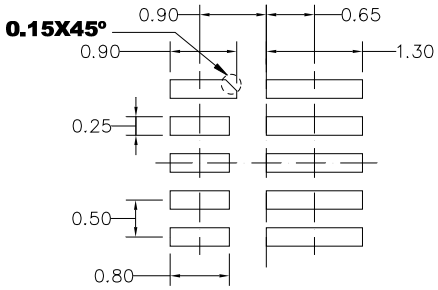
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.