MP6652A

18V, Single-Phase BLDC Fan Driver with Embeded Hall Sensor and MOSFETs

DESCRIPTION

The MP6652A is a single-phase brushless DC (BLDC) fan driver with integrated power MOSFETs and a Hall-effect sensor. It supports up to 1A of peak current across a wide 3V to 18V input voltage (V_{IN}) range.

The fan speed is controlled by a pulse-width modulation (PWM) signal applied on the PWM pin. The MP6652A's configurable speed curve makes this device well-suited for cooling fan applications that require flexible speed curve control.

The FG/RD pin is an open-drain output that can be configured for speed detection (FG) or locked rotor protection (RD). The FG/RD pin must be pulled up externally.

Rich protections are implemented for robust operation. These protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked rotor protection, thermal shutdown, and over-current protection (OCP).

The MP6652A is available in a TSOT23-6-SL and a TSOT23-6-R packages.

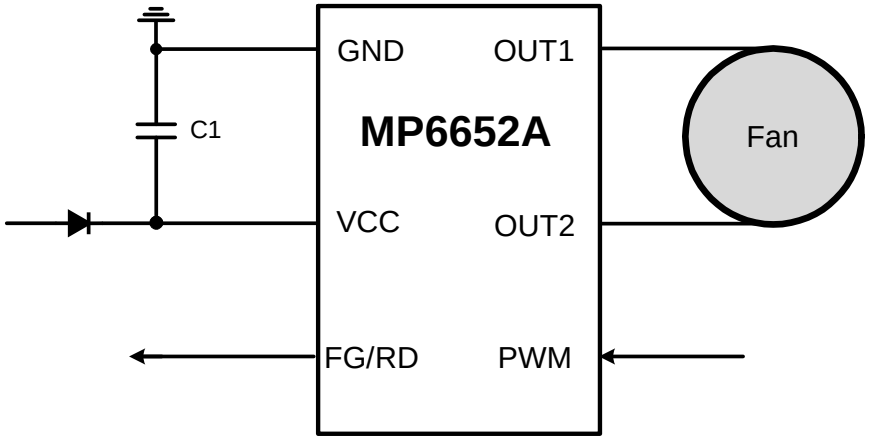
FEATURES

- On-Chip Hall Sensor
- Wide 3V to 18V Operating Input Voltage (V_{IN}) Range
- Up to 1A Peak Current Limit
- Integrated Power MOSFETs: Total 850mΩ for High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)
- Configurable Speed Curve
- 1kHz to 100kHz PWM Input Frequency Range
- Soft-On/Off Phase Commutation
- Configurable Output Indictation on FG/RD:
  - Rotational Speed Indicator (FG)
  - Locked Rotor Protection Fault (RD)
- Fixed 27kHz Output Switching Frequency (f_{SW})
- Configurable Speed Reference Soft-Start Time
- 1x, 0.5x, or 2x Original FG Frequency Output
- Recoverable Locked Rotor Protection
- Recoverable Thermal Protection
- Recoverable Input Over-Voltage Protection (OVP)
- Available in TSOT23-6-SL and TSOT23-6-R Packages

APPLICATIONS

- Cooling Fans
- GPU Cooling Fans
- CPU Fans for Personal Computers or Servers
- Other Brushless Cooling Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Tape & Reel	Top Marking	MSL Rating
MP6652AGJS-xxxx**	TSOT23-6-SL	Normal	*See Below*	1
MP6652AGJR-xxxx**	TSOT23-6-R	Reverse	*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MP6652AGJS-xxxx-Z).

** "-xxxx" is the configuration code identifier. The four digits of the suffix ("-xxxx") can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the default "-0000" code.

TOP MARKING (MP6652AGJS-xxxx)

BUXY
LLL

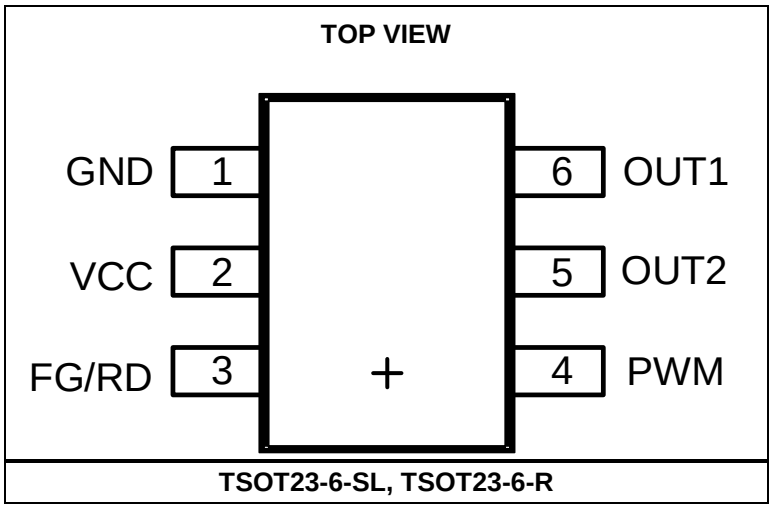
BUX: Product code
Y: Year code
LLL: Lot number

TOP MARKING (MP6652AGJR-xxxx)

| BUXY

BUX: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.** The VCC pin must be bypassed locally.
3	FG/RD	**Rotational speed detection (default) or dead lock indication (RD signal).** The FG/RD pin is an open-drain output. Pull FG/RD high externally.
4	PWM	**PWM input for speed control.** A 1kHz to 100kHz pulse-width modulation (PWM) input is recommended during normal operation.
5	OUT2	**Motor driver output switching node 2.**
6	OUT1	**Motor driver output switching node 1.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, $V_{OUT1/2}$ ..... -0.3V to +25V
FG/RD, PWM.....-0.3V to V_{CC} + 0.3V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2)
.....1.25W
Junction temperature ..... 150°C
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 18V
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{VCC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol		Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			2.76		V
Input UVLO hysteresis				0.25		V
Operating supply current	I_{CC}			4		mA
PWM input high voltage	V_{PWMH}		2			V
PWM input low voltage	V_{PWML}				0.4	V
PWM input internal pull-up resistance				100		kΩ
High-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)}$	I_{OUT} = 100mA		0.85		Ω
Over-current protection (OCP) threshold	I_{OCP}			1		A
Input over-voltage protection (OVP) threshold	V_{OVP}		18	19.1	20.2	V
Input OVP hysteresis	V_{OVP_HYS}			1.3		V
PWM output frequency (switching frequency)	f_{SW}	T_J = 25°C	24.2	27	29.8	kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA, V_{PULL} = 5V			0.35	V
Soft turn-on angle	θ_{SON}	SON = 0x0F		46.8		deg
Soft turn-off angle	θ_{SOFF}	SOFF = 0x0F		46.5		deg
Hall offset angle	θ_E	HAL_ANG = 0x07		22.5		deg
Locked rotor detection time (5)	t_{RD}			0.6		s
Locked rotor off time (5)	t_{RD_OFF}	LOCK_SEL = 00		3.6		s
Minimum recommended magnetic field			-1		+1	mT
Thermal shutdown threshold (5)				165		°C
Thermal shutdown hysteresis (5)				25		°C

Note:

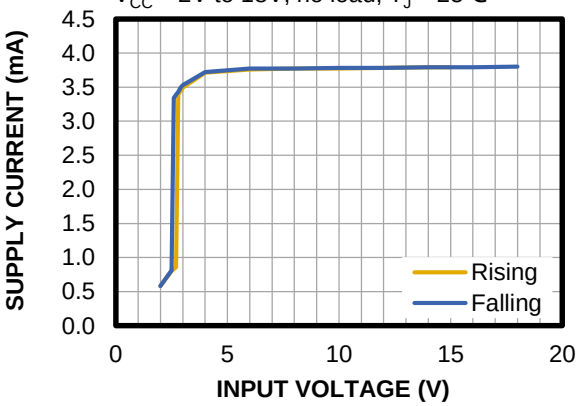
5) Guaranteed by design

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_A = -40°C to 125°C, unless otherwise noted.

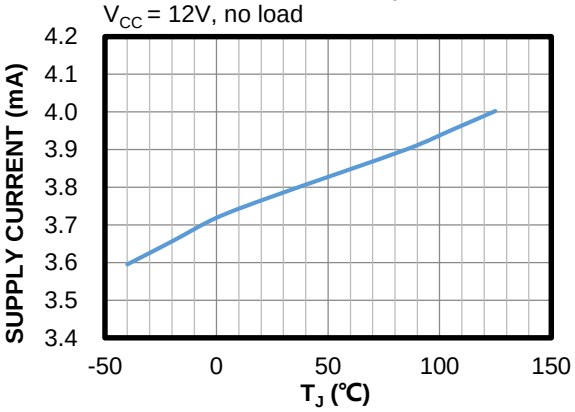
Supply Current vs. Input Voltage

V_{CC} = 2V to 18V, no load, T_J = 25℃

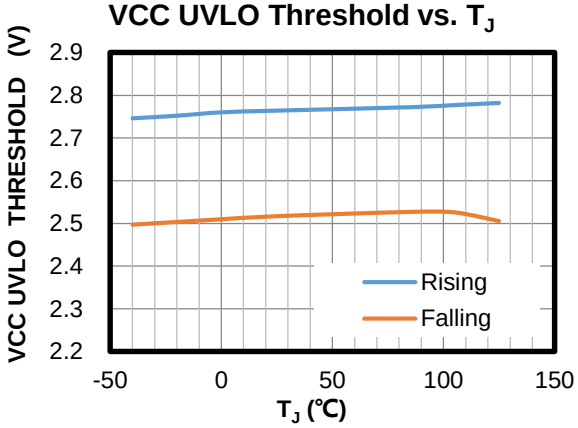


Supply Current vs. T_J

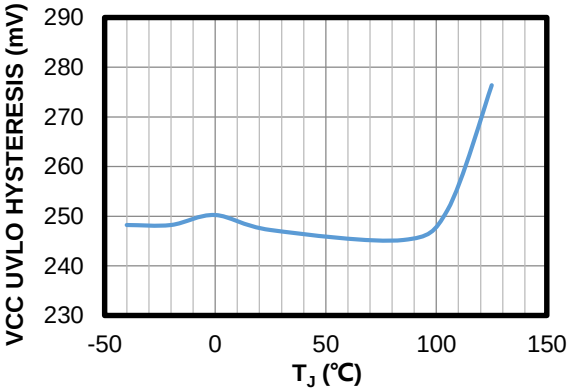
V_{CC} = 12V, no load



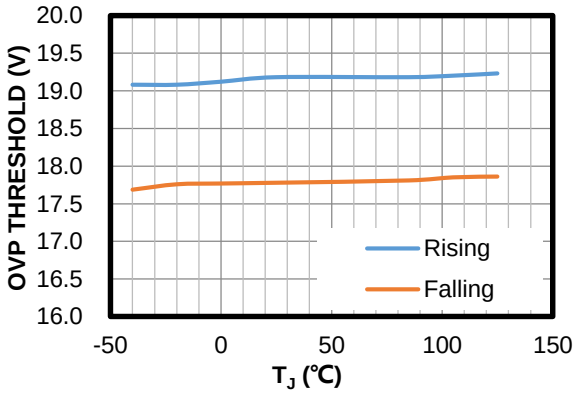
VCC UVLO Threshold vs. T_J



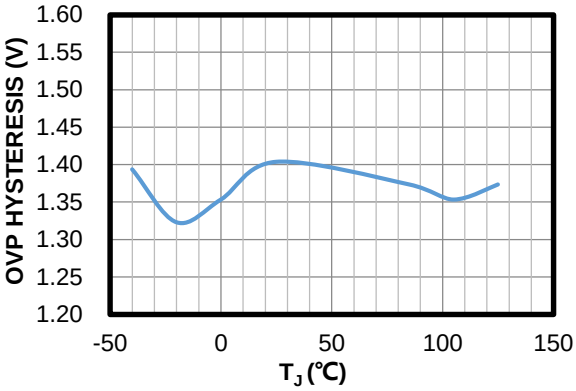
VCC UVLO Hysteresis vs. T_J



OVP Threshold vs. T_J



OVP Hysteresis vs. T_J

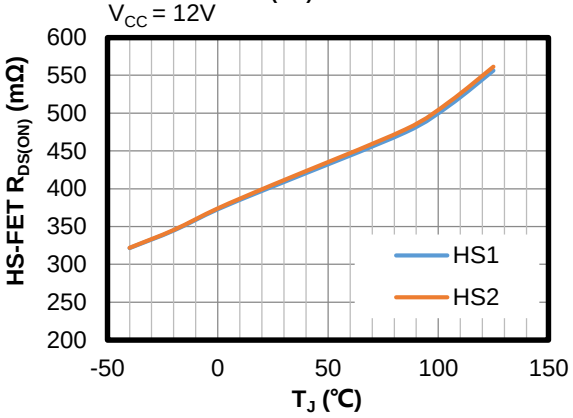


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = -40°C to 125°C, unless otherwise noted.

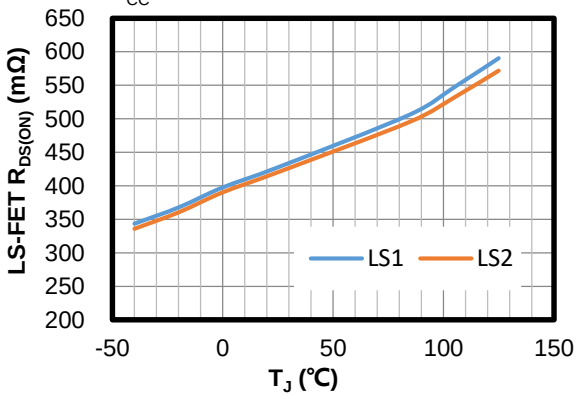
HS-FET $R_{DS(ON)}$ vs. T_J

V_{CC} = 12V



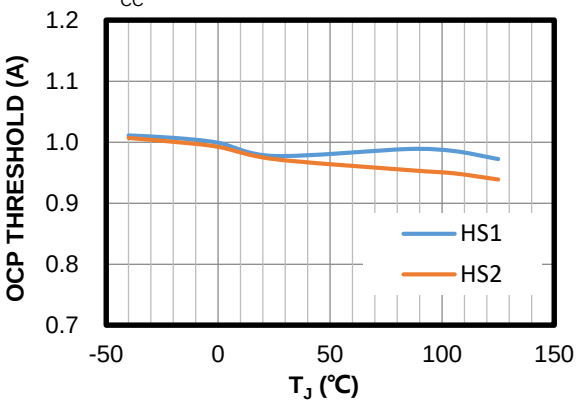
LS-FET $R_{DS(ON)}$ vs. T_J

V_{CC} = 12V



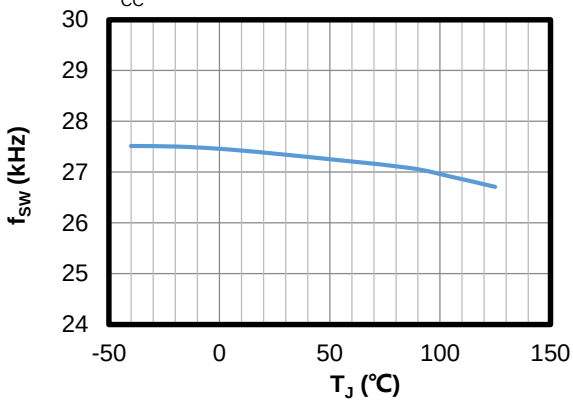
OCP Threshold vs. T_J

V_{CC} = 12V



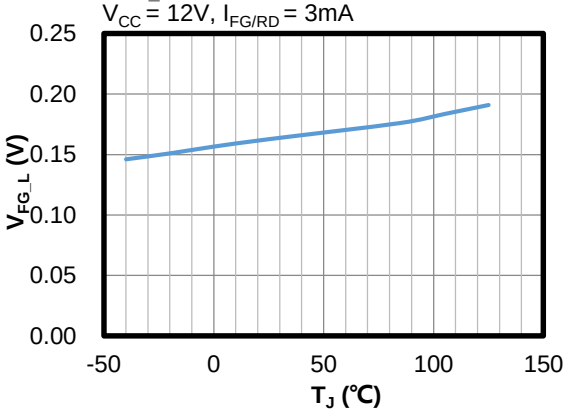
Switching Frequency vs T_J

V_{CC} = 12V



V_{FG_L} vs. T_J

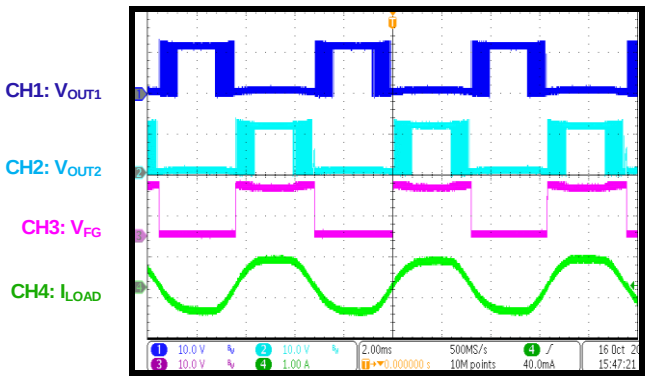
V_{CC} = 12V, $I_{FG/RD}$ = 3mA



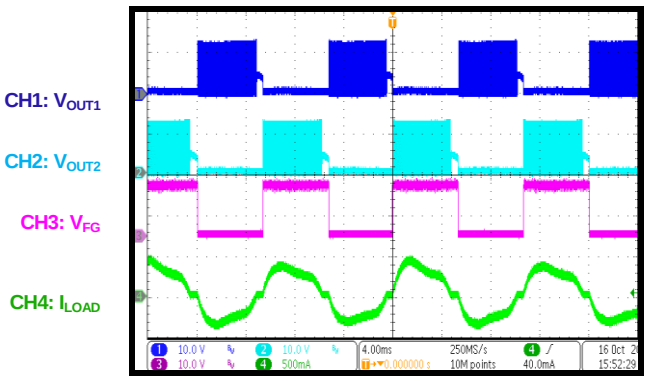
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 8025 Axial Fan, 450mA, 5000rpm, T_A = 25°C, unless otherwise noted.

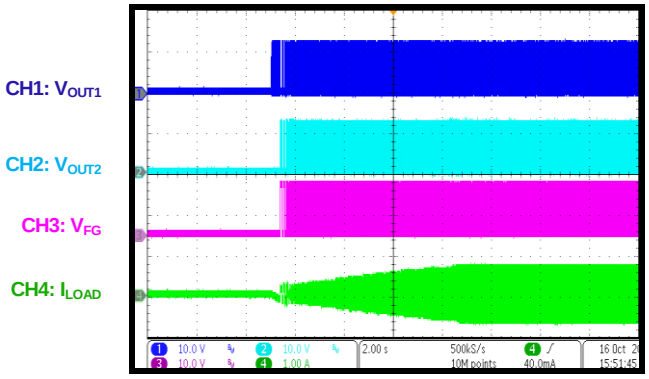
Steady State
PWM duty cycle = 100%



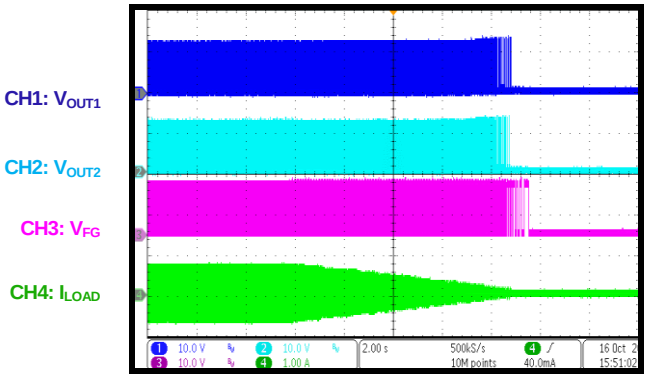
Steady State
PWM duty cycle = 50%



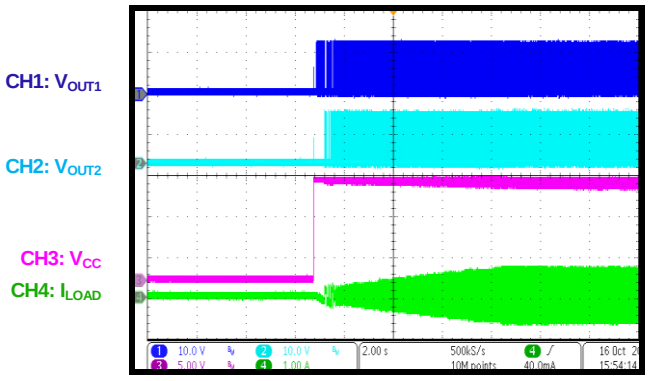
PWM On
PWM duty cycle = 0% to 100%



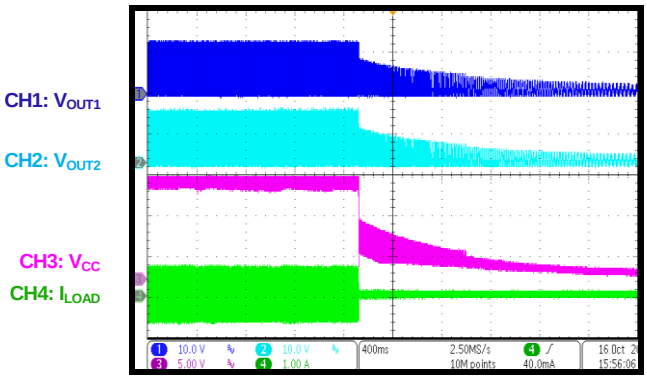
PWM Off
PWM duty cycle = 100% to 0%



Start-Up through VCC
VCC power plugged in



Shutdown through VCC
VCC power plugged out

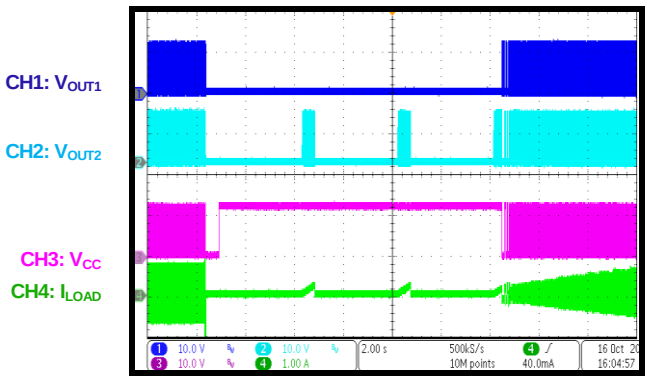


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 8025 Axial Fan, 450mA, 5000rpm, T_A = 25°C, unless otherwise noted.

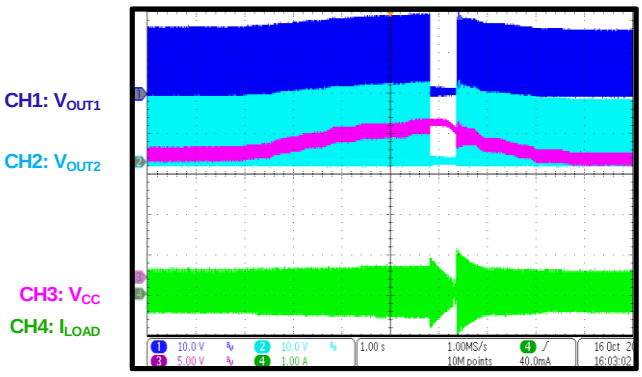
Locked Rotor Protection

Lock rotor then release



Over-Voltage Protection (OVP)

V_{CC} ramps up, then ramps down



FUNCTIONAL BLOCK DIAGRAM

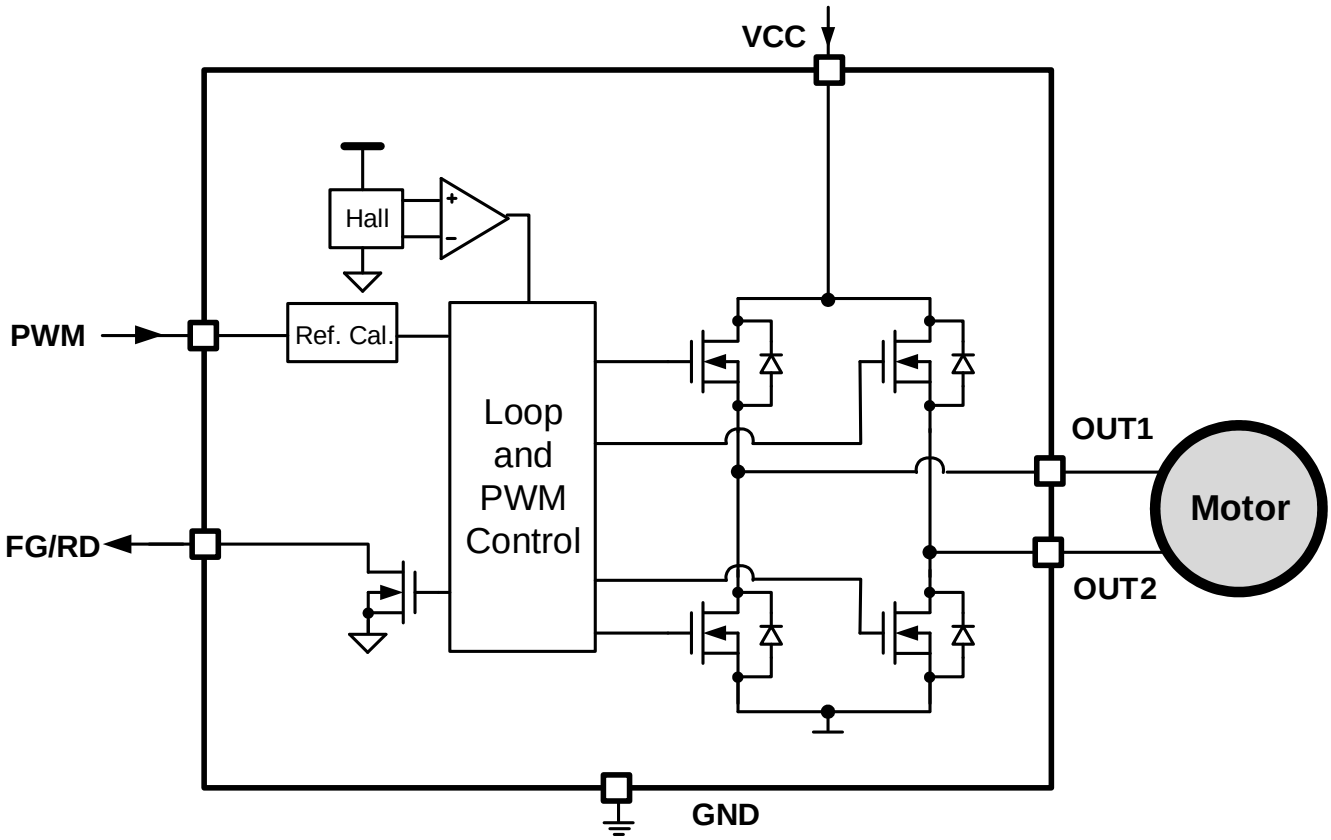


Figure 1: Functional Block Diagram

OPERATION

Speed Control

The PWM signal on the PWM pin accepts a wide input frequency range (1kHz to 100kHz). The device adjusts the motor speed by detecting the PWM signal duty cycle.

When the PWM duty cycle exceeds the value set by DIN_MIN plus a hysteresis, the OUT1 and OUT2 pins' output duty cycles follow the PWM's input duty cycle. The minimum output duty cycle is set by DOUT_MIN and SPD_ZERO.

If SPD_ZERO = 1, the MP6652A stops switching when the input duty cycle is below the value set by DIN_MIN (see Figure 1).

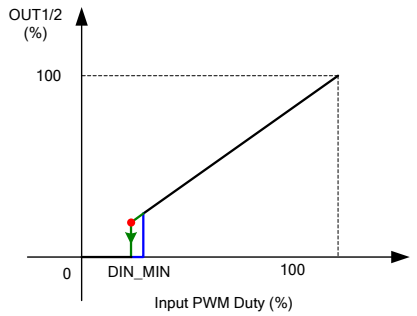


Figure 2: Speed Curve (SPD_ZERO = 1)

If SPD_ZERO = 0, the minimum output duty cycle is limited by DOUT_MIN (see Figure 3).

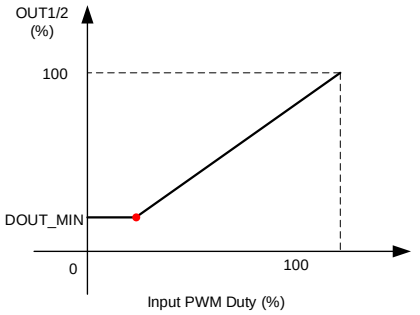


Figure 3: Speed Curve (SPD_ZERO = 0)

OUT1/2 Normal Operation

During normal operation, the MP6652A controls the H-bridge MOSFET switching according to a timing sequence. All operation sequences are based on the Hall signal coming from the embedded Hall sensor. H_{A_IN} is the original signal from the embedded Hall sensor, and H_{A_OUT} is generated based on H_{A_IN} with a Hall offset angle (see Figure 4).

H_{A_OUT} is the control signal for phase commutation.

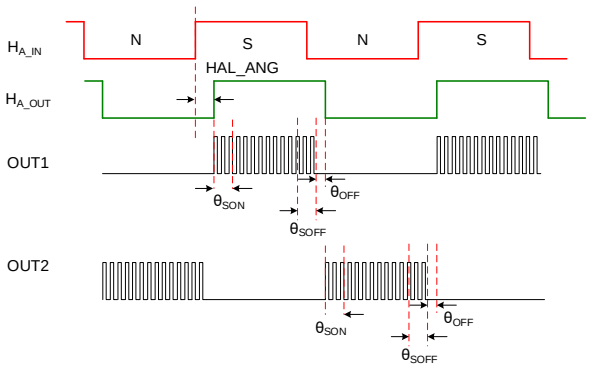


Figure 4: Operation with Hall Trimming Angle

If the H_{A_OUT} signal is high, OUT2 remains low while OUT1 switches phases. If the H_{A_OUT} signal is low, OUT1 remains low while OUT2 switches phases.

- The phase shift between H_{A_IN} and H_{A_OUT} is set via the HAL_ANG bits.
- The phase shift's leading/lag is set via the HAL_FLG bit.

Soft-On Commutation Section

During soft-on commutation, the switching phase's output duty cycle gradually increases from 0% duty cycle to the target duty cycle (see θ_{SON} in Figure 4).

The soft-on commutation angle is set by the SON_ANG register. The maximum soft-on commutation angle is 90°. The resolution is 2.8°.

Soft-Off Commutation

During soft-off commutation, the switching phase's output duty cycle gradually decreases from the steady duty cycle to 0% duty cycle (see θ_{SOFF} in Figure 4).

The soft-off commutation angle is set by the SOFF_ANG register. The maximum soft-off commutation angle is 90°. The resolution is 2.8°.

Configurable Speed Curve

The MP6652A provides 8 points (register addresses 01h~08h) to configure the speed curve. These registers set the output duty cycle, which correspond to PWM's input duty cycle every 12.5% (from 12.5% to 100%).

These 8 registers set the output duty cycle, but they can be used to configure the speed curve (see Figure 5).

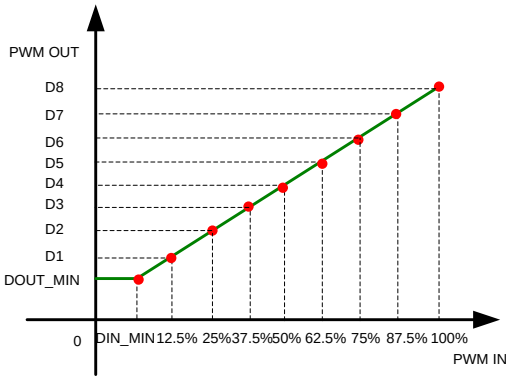


Figure 5: Speed Curve Configurations

Soft-Start Time

To reduce the input inrush current during speed transitions, the MP6652A provides a configurable soft-start time for the speed reference via the TSS bits. The soft-start time can be set between 2.4s and 9.6s.

Rotor Speed Indication (FG)

The FG/RD pin can be set for speed indication (FG) or rotor lock indication (RD), depending on the FGRD bits.

- FGRD = 00: FG/RD is 1x the original Hall frequency
- FGRD = 01, FG/RD is 0.5x the original Hall frequency
- FGRD = 10, FG/RD is 2x the original Hall frequency
- FGRD = 11, FG/RD is set as the rotor lock indicator

Protection Behavior

The MP6652A has rich and robust protections including over-voltage voltage (OVP), under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown (TSD).

Neighbor Pin Short Protection (SCP)

The MP6652A provides internal overload mode and short-circuit protection (SCP) by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the SCP threshold, all of the MOSFETs turn off after a blanking time.

Over-Current Protection (OCP)

If the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the OCP threshold after a blanking time during normal switching, the HS-FET turns off immediately and LS-FET turn on. It resumes switching in the next switching cycle.

Thermal Shutdown (TSD)

The MP6552A provides thermal monitoring If the die temperature exceeds the thermal protection threshold, the IC enters a protection mode. Operation automatically resumes once the die temperature drops to a safe level.

Under-Voltage Lockout (UVLO)

If the voltage on the VCC pin drops below the UVLO threshold at any moment, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{CC} rises above its UVLO threshold.

Locked Rotor (Dead Lock) Protection (RD)

If the FGRD bit is set to 11, the FG/RD pin outputs a dead lock indication signal when locked rotor protection is triggered.

If the MP6652A cannot detect a Hall signal edge during the 0.6s detection time, locked rotor protection is triggered, and both low-side MOSFETs (LS-FETs) of the H-bridge turn on The FG/RD pin's output depends on the RD_H_L bit.

The IC attempts to automatically restart after the lock retry time set via the LOCK_SEL bits. The locked rotor indication signal is released after 3 Hall signal edges are detected.

Over-Voltage Protection (OVP)

If V_{CC} exceeds the OVP threshold (about 19V), the device turns off the HS-FETs. The device resumes normal operation once V_{CC} drops below 18V.

Online Design Mode

To configure the internal register, the MP6652A has an online design mode. In online design mode, the internal registers can be read and written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM). Refer to the related GUI software for more details on changing parameters and configuring the memory.

REGISTER MAP

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00 (OTP/REG)	DOUT_MIN[7:0]							
0x01 (OTP/REG)	D1[7:0]							
0x02 (OTP/REG)	D2[7:0]							
0x03 (OTP/REG)	D3[7:0]							
0x04 (OTP/REG)	D4[7:0]							
0x05 (OTP/REG)	D5 [7:0]							
0x06 (OTP/REG)	D6[7:0]							
0x07 (OTP/REG)	D7[7:0]							
0x08 (OTP/REG)	D8[7:0]							
0x09 (OTP/REG)	RESERVED	DIN_MIN[6:0]						
0x0A (OTP/REG)	RESERVED	SPD_SEL[1:0]		SON_ANG[4:0]				
0x0B (OTP/REG)	RESERVED	TPRE[1:0]		SOFF_ANG[4:0]				
0x0C (OTP/REG)	LOCK_DIS	RESERVED	RD_HL	HAL_FLAG	HAL_ANG[3:0]			
0x0D (OTP/REG)	LOCK_SEL[1:0]		OCP_SEL[1:0]		RESERVED			TADV_EN
0x0E (OTP/REG)	ZCD_POS	TADV[1:0]		OVP	T_SS[1:0]		FGRD[1:0]	
0x0F (OTP/REG)	DUTY_ST[1:0]		SPD_ZERO	SCP_DIS	OCP_DIS	BRK_SLOW	DN_SCALE[1:0]	
0x14 (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			

Register: 0x00

Bits	Bit Name	Access	Default	Description
7:0	DOUT_MIN[7:0]	OTP/REG	0x20	Sets the minimum output duty cycle limit. The minimum output duty cycle = DOUT_MIN[7:0] / 256. The default is 12.5%. If SPD_ZERO = 1, then the device stops switching once the input PWM duty cycle drops below the duty cycle set by DIN_MIN. If SPD_ZERO = 0, then the device keeps the minimum output duty once the input PWM duty cycle drops below the duty cycle set by DIN_MIN.

Register: 0x01

Bits	Bit Name	Access	Default	Description
7:0	D1[7:0]	OTP/REG	0x20	Sets the output duty cycle when the input duty cycle = 12.5%. The output duty cycle = D1[7:0] / 256. The default is 12.5%.

Register: 0x02

Bits	Bit Name	Access	Default	Description
7:0	D2[7:0]	OTP/REG	0x40	Sets the output duty cycle when the input duty cycle = 25%. The output duty cycle = D2[7:0] / 256. The default is 25%.

Register: 0x03

Bits	Bit Name	Access	Default	Description
7:0	D3[7:0]	OTP/REG	0x60	Sets the output duty cycle when the input duty cycle = 37.5%. The output duty cycle = D3[7:0] / 256. The default is 37.5%.

Register: 0x04

Bits	Bit Name	Access	Default	Description
7:0	D4[7:0]	OTP/REG	0x80	Sets the output duty cycle when the input duty cycle = 50%. The output duty cycle = D4[7:0] / 256. The default is 50%.

Register: 0x05

Bits	Bit Name	Access	Default	Description
7:0	D5[7:0]	OTP/REG	0xA0	Sets the output duty cycle when the input duty cycle = 62.5%. The output duty cycle = D5[7:0] / 256. The default is 62.5%.

Register: 0x06

Bits	Bit Name	Access	Default	Description
7:0	D6[7:0]	OTP/REG	0xC0	Sets the output duty cycle when the input duty cycle = 75%. The output duty cycle = D6[7:0] / 256. The default is 75%.

Register: 0x07

Bits	Bit Name	Access	Default	Description
7:0	D7[7:0]	OTP/REG	0xE0	Sets the output duty cycle when the input duty cycle = 87.5%. The output duty cycle = D7[7:0] / 256. The default is 87.5%.

Register: 0x08

Bits	Bit Name	Access	Default	Description
7:0	D8[7:0]	OTP/REG	0xFF	Sets the output duty cycle when the input duty cycle = 100%. The output duty cycle = D8[7:0] / 256. The default is 100%.

Register: 0x09

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:0	DIN_MIN[6:0]	OTP/REG	0x20	Sets the starting duty cycle. The starting duty cycle = DIN_MIN[6:0] / 256. The default is 12.5%.

Register: 0x0A

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:5	SPD_SEL[1:0]	OTP/REG	01	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds. 00: 100rpm 01: 400rpm (default) 10: 800rpm 11: 1600rpm
4:0	SON_ANG[4:0]	OTP/REG	10000	Sets the soft-on commutation angle. 00000: 2.8° 00001: 5.6° …. 11111: 90° The soft-on angle can be calculated with the following equation: Soft-on angle = (SON_ANG[4:0] + 1) x 2.8° With 2.8° per step.

Register: 0x0B

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.

6:5	T_PRE[1:0]	OTP/REG	00	Sets the pre start-up timer. 00: 18.6ms/step (default) 01: 9.3ms/step 10: 4.6ms/step 11: 2.3ms/step
4:0	SOFF_ANG[4:0]	OTP/REG	10000	Sets the soft-off commutation angle. 00000: 2.8° 00001: 5.6° … 11111: 90° The soft-off angle can be calculated with the following equation: Soft-off angle = (SOFF_ANG[4:0] + 1) x 2.8° With 2.8° per step.

Register: 0x0C

Bits	Bit Name	Access	Default	Description
7	LOCK_DIS	OTP/REG	0	Enables locked rotor protection. 0: Enabled (default) 1: Disabled
6	RESERVED	N/A	1	Reserved.
5	RD_HL	OTP/REG	0	Selects the RD output polarity bit when locked rotor protection is triggered. 0: Low output when locked rotor protection is triggered (default) 1: High output when locked rotor protection is triggered
4	HAL_FLAG	OTP/REG	0	Sets whether the Hall offset angle lags or leads. 0: Lag (default) 1: Lead
3:0	HAL_ANG[3:0]	OTP/REG	0000	Sets the Hall offset angle. 0000: 2.8° (default) 0001: 5.6° … 1111: 45° The Hall offset angle can be calculated with the following equation: Hall offset angle = (HAL_ANG[3:0] + 1) x 2.8° With 2.8° per step.

Register: 0x0D

Bits	Bit Name	Access	Default	Description
7:6	LOCK_SEL[1:0]	OTP/REG	00	Selects the lock protection retry time. 00: 3.6s (default) 01: 4.8s 10: 6s 11: 8.5s
5:4	OCP_SEL[1:0]	OTP/REG	11	Selects the current limit threshold. 00: 0.35A 01: 0.5A 10: 0.75A 11: 1A (default)

3:1	RESERVED	N/A	011	Reserved.
0	TADV_EN	OTP/REG	1	Enables the advanced off time. 0: Disabled 1: Enabled (default)

Register: 0x0E

Bits	Bit Name	Access	Default	Description
7	ZCD_POS	OTP/REG	0	Selects the angle position zero-current detection (ZCD). 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°.
6:5	TADV[1:0]	OTP/REG	00	Sets the advanced off time. 00: Auto (default) 01: 5.6° 01: 11.2° 11: 22.5°
4	OVP	OTP/REG	0	Enables over-voltage protection (OVP) 0: Enabled (default) 1: Disabled
3:2	T_SS[1:0]	OTP/REG	00	Sets the soft transition time. This is the time that it takes for the output duty to transition from 0 to 100%. 00: 2.4s (default) 01: 4.8s 10: 7.2s 11: 9.6s
1:0	FGRD[1:0]	OTP/REG	00	Selects the FG/RD pin output. 00: 1x (default) 01: 0.5x 10: 2x 11: RD

Register: 0x0F

Bits	Bit Name	Access	Default	Description
7:6	DUTY_ST[1:0]	OTP/REG	01	Sets the initial output duty cycle at start-up. 00: 0% 01: 12.5% (default) 10: 18.5% 11: 25%
5	SPD_ZERO	OTP/REG	1	Enables zero speed. 0: Keep the minimum output duty cycle if the input PWM duty cycle drops below DIN_MIN 1: Stop switching if the input PWM duty cycle drops below DIN_MIN (default)
4	SCP_DIS	OTP/REG	0	Enables short-circuit protection (SCP). 0: Enabled (default) 1: Disabled
3	OCP_DIS	OTP/REG	0	Enables over-current protection (OCP). 0: Enabled (default) 1: Disabled

2	BRK_SLOW	OTP/REG	0	Sets the threshold at which the fan speed drops below its speed threshold, then the IC initiates a PWM cycle immediately after start-up. 0: 800rpm (default) 1: 400rpm
1:0	DN_SCALE[1:0]	OTP/REG	00	Sets the PWM output duty ramp-down scale as the output duty cycle drops from 100% to 0%. 00: 1 x T_SS[1:0] (default) 01: 2 x T_SS[1:0] 10: 3 x T_SS[1:0] 11: 4 x T_SS[1:0]

Register: 0x14

Bits	Bit Name	Access	Default	Description
7:6	RESERVED	N/A	00	Reserved.
5:4	OTP_PAGE[1:0]	REG	00	Indicates the OTP page (read-only). 00: No OTP page is configured (default) 01: The first OTP page is configured 10: The second OTP page is configured
3:0	RESERVED	N/A	0000	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor as close to the VCC and GND pins as possible. This keeps the input voltage (V_{IN}) stable and reduces V_{IN} noise. The input capacitor impedance should be low at the switching frequency (f_{SW}).

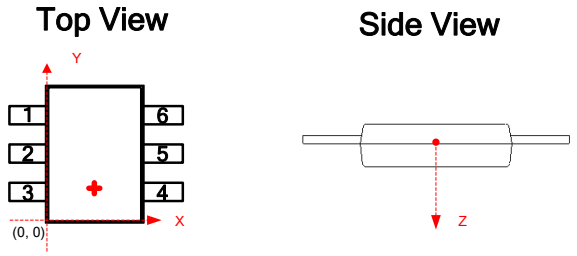
Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The capacitance of the ceramic capacitor drops when the voltage across the capacitor rises; the ceramic capacitor can lose more than 50% of its capacitance when the voltage across the capacitor is close to its rated voltage.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

For certain applications, it is recommended to use an additional, large electrolytic capacitor to absorb motor energy.

Hall Sensor Position

The Hall sensor cell is located in the lower-left corner of the package (see Figure 6).



(X, Y, Z) = (800µm, 783µm, 80µm)

Figure 6: Hall Sensor Position

Selecting the Reverse Blocking Diode

To avoid damage if the fan experiences a reverse plug-in, a reverse blocking diode is required. The reverse blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's maximum reverse voltage must exceed 30V, and its forward current rating must exceed the input current (I_{IN}).

ESD Enhanced Circuit

Some fan products must pass system-level ESD testing. System-level ESD follows the IEC61000-4-2 standard. There are differences between human body mode (HBM) ESD and system-level ESD (IEC 61000-4-2). Figure 7 shows the equivalent circuit of a HBM ESD circuit.

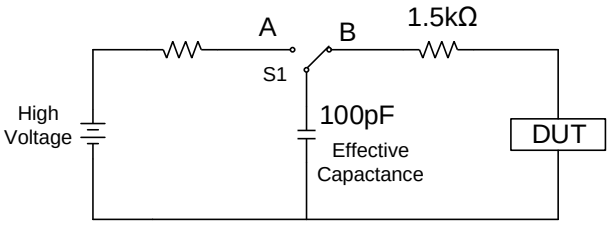


Figure 7: Equivalent Circuit of HBM ESD Circuit

Figure 8 shows the equivalent circuit of a system-level ESD circuit.

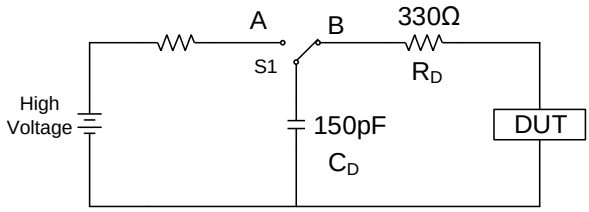


Figure 8: Equivalent Circuit of System Level ESD

Compared to the HBM ESD ratings, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistance of the IEC level ESD is much smaller.

There are two different modes for IEC61000-4-2 ESD testing: air discharge and contact discharge. Contact discharge is the first choice for testing.

The MP6652A can pass IEC61000-4-2 4kV contact ESD testing without any additional components.

If a higher level is required, then an external circuit may be required to enhance the ESD capability (see Figure 9).

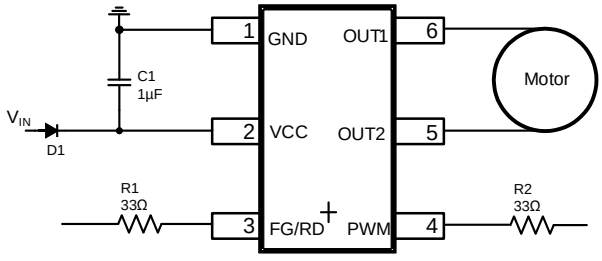


Figure 9: Enhanced ESD using a Resistor

Figure 10 on page 19 shows an external ESD-enhanced circuit using a Zener/ESD diode.

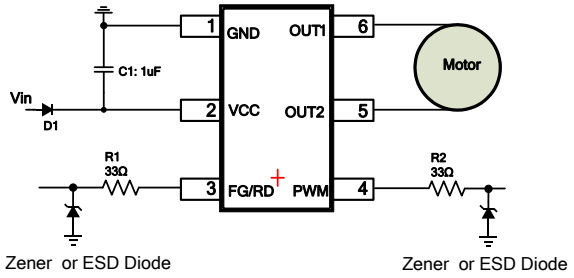


Figure 10: Enhanced ESD using a Zener Diode or ESD Diode

Input Clamping Circuit

To avoid high voltage spikes caused by the energy stored in the motor, a voltage-clamping circuit may be required (especially for applications with a high current or a large inertia). A 15V/SOD-123 package TVS diode or Zener diode is sufficient for most 12V input applications.

Input Snubber

Due to the input capacitor energy charge/discharge during phase commutation, I_{IN} has switching cycle ringing. If necessary, place an RC snubber (a 2Ω resistor in series with a 1μF capacitor) in parallel with the input capacitor. This effectively prevents switching cycle ringing.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 11 and follow the guidelines below:

1. Place the input capacitor as close as possible to the VCC and GND pins. See the Selecting the Input Capacitor section on page 20 for more details.

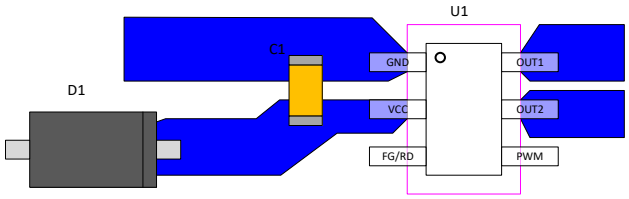


Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

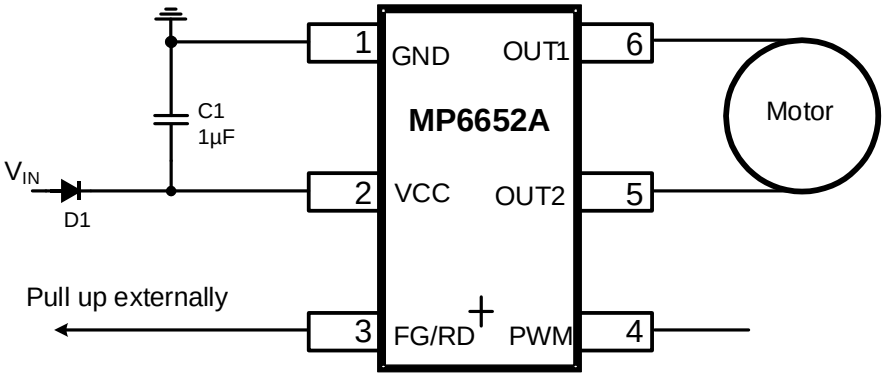


Figure 12: Typical Application Circuit for Normal Applications

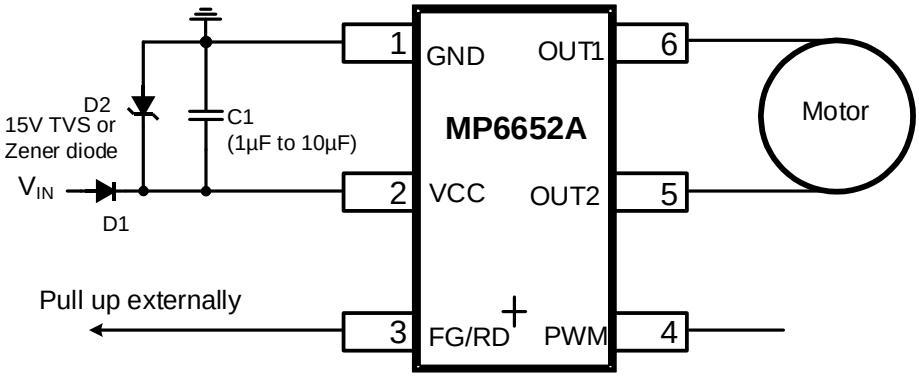
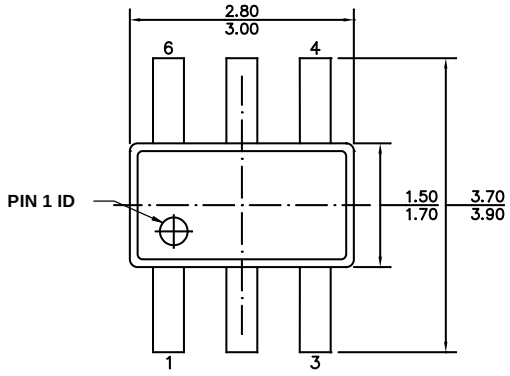


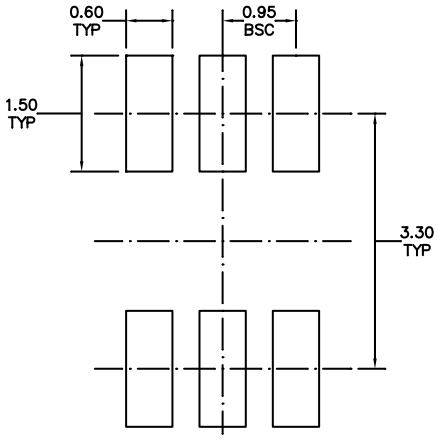
Figure 13: Typical Application Circuit for High-Current, High-Inertia Fan

PACKAGE INFORMATION

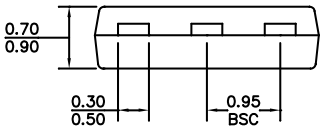
TSOT23-6-SL



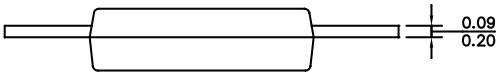
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



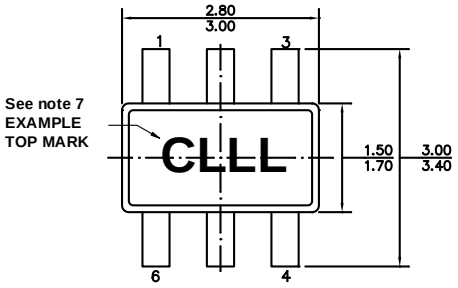
SIDE VIEW

NOTE:

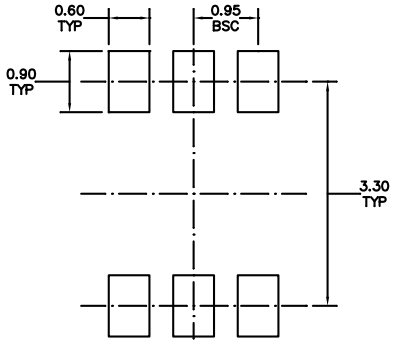
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

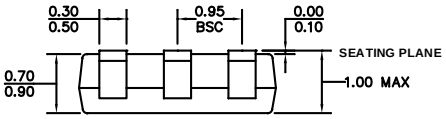
TSOT23-6-R



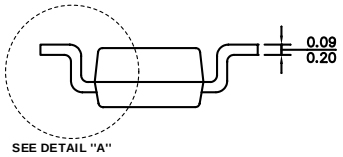
TOP VIEW



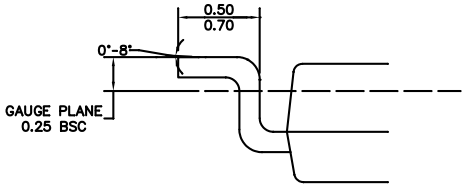
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



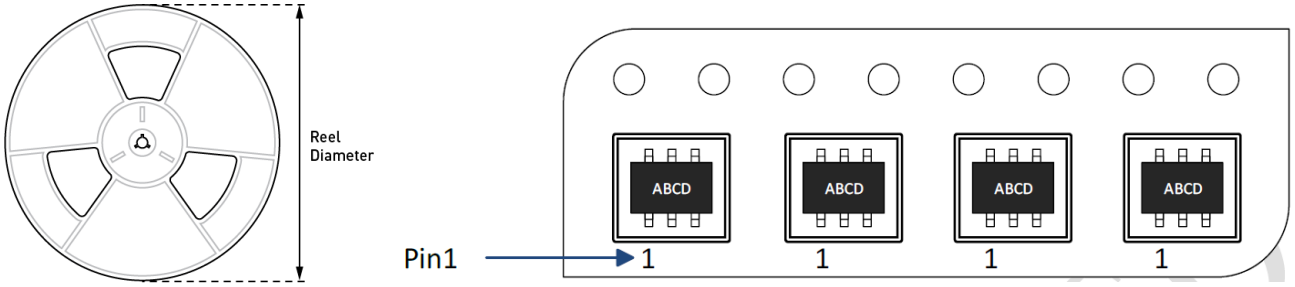
DETAIL "A"

NOTE:

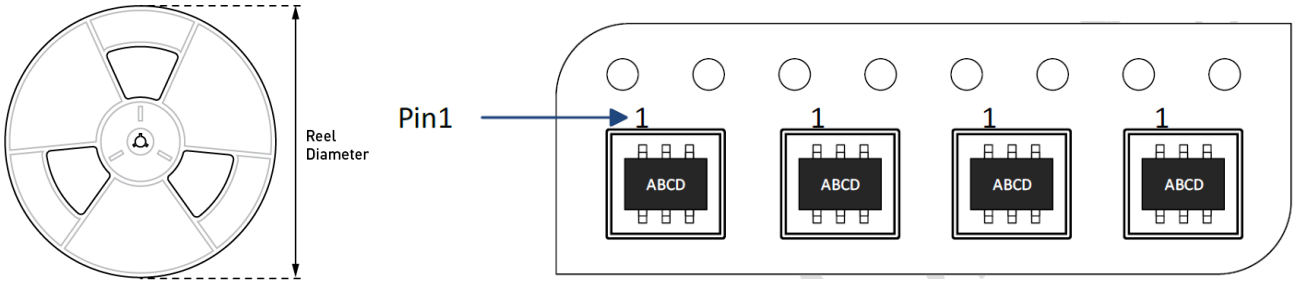
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS UPPER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION

TSOT23-6-SL



TSOT23-6-R



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6652AGJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MP6652AGJR-xxxx-Z	TSOT23-6-R	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/24/2022	Initial Release	-