MP6653

32V, Single-Phase BLDC Motor Driver with Embedded Hall Sensor

DESCRIPTION

The MP6653 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and an embedded Hall sensor. It can drive a single-phase BLDC motor, with up to 1.2A of peak output current (I_{OUT}) across a 5.5V to 32V input voltage (V_{IN}) range.

The MP6653 controls the motor speed through the pulse-width modulation (PWM) signal or DC voltage on the PWM pin. The device features soft commutation and a Hall offset angle that can be flexibly configured to optimize performance.

The MP6653 also has rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6653 is available in TSOT23-6-SL and TSOT23-6-L packages.

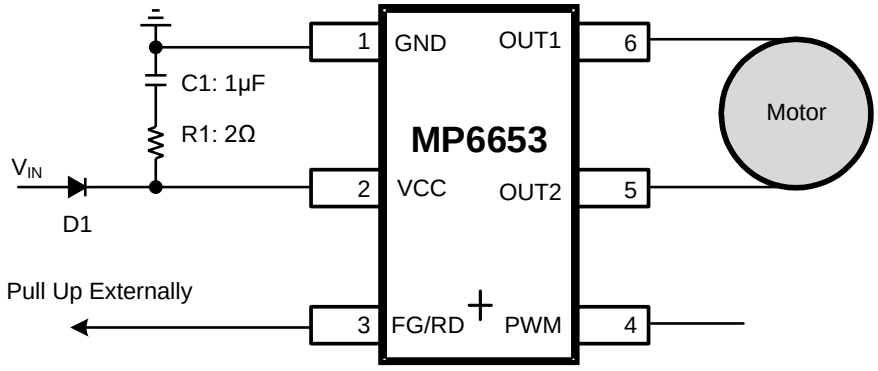
FEATURES

- 5.5V to 32V Operating Input Voltage (V_{IN}) Range
- On-Chip Hall Sensor
- Integrated MOSFETs: HS-FET + LS-FET = 960mΩ
- Soft Commutation
- Starting Duty Set with Hysteresis
- Selectable Open-Loop or Closed-Loop Speed Control
- Configurable Soft-Start Time
- Configurable Hall Lead/Lag Angle
- Supports 50Hz to 100kHz Pulse-Width Modulation (PWM) Input Frequency or DC Input
- Automatic Reverse Current Blocking
- 24kHz PWM Output Frequency
- Configurable Current Limit (I_{LIMIT})
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Standby Mode
- Selectable FG and RD Outputs
- Available in TSOT23-6-SL and TSOT23-6-L Packages

APPLICATIONS

- Cooling Fans
- General Fans
- Industrial Cooling Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6653GJS-xxxx**	TSOT23-6-SL	*See Below*	1
MP6653GJL-xxxx**	TSOT23-6-L		

* For Tape & Reel, add suffix -Z (e.g. MP6653GJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING (MP6653GJS)

BVVY

LLL

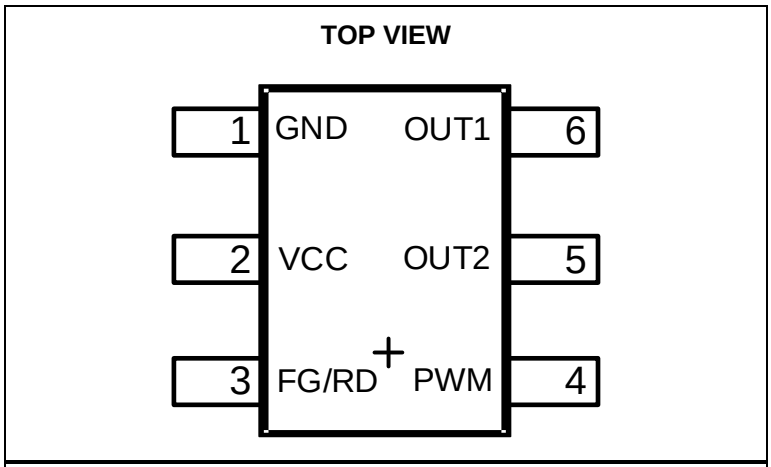
BVV: Product code of MP6653GJS
Y: Year code
LLL: Lot number

TOP MARKING (MP6653GJL)

| BVVY

BVV: Product code of MP6653GJL
Y: Year code

PACKAGE REFERENCE



TSOT23-6-SL and TSOT23-6-L

PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input power supply.** Bypass the VCC pin locally.
3	FG/RD	**Speed indicator (FG), locked-rotor indicator (RD) output.** The FG/RD is an open-drain output that should be pulled up externally.
4	PWM	**Speed control pulse-width modulation input.** The PWM pin supports a 50Hz to 100kHz pulse-width modulation (PWM) input frequency or a 0V to 3V DC input. PWM is pulled up internally via a 100kΩ resistor.
5	OUT2	**Motor driver output 2.** The OUT2 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.
6	OUT1	**Motor driver output 1.** The OUT1 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC} .....-0.3V to +40V
All other pins .....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (2) 1.25W
Input voltage (V_{IN}) .....5.5V to 32V
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged-device model (CDM)..... ±2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....5.5V to 32V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ……..……..100……55…°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

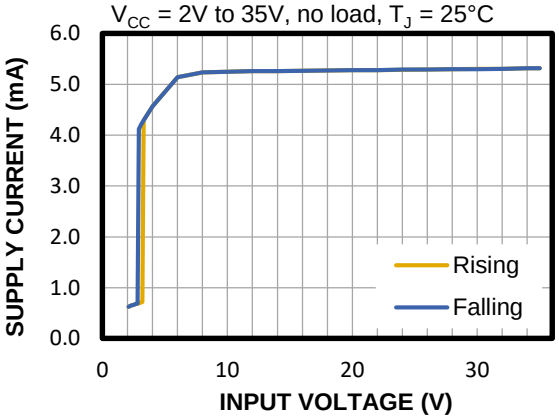
Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	$V_{CC\_UVLO\_RISING}$			3.1		V
V_{CC} UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			0.4		V
Operating supply current	I_{CC}	PWM is high		5	7	mA
Standby current	I_{STD}	PWM is low		75		µA
Pulse-width modulation (PWM) input high threshold	V_{PWM_HIGH}		2.2			V
PWM input low threshold	V_{PWM_LOW}				0.8	V
DC input high threshold	V_{DC_HIGH}			3		V
DC input low threshold	V_{DC_LOW}			100		mV
PWM internal pull-up resistance	R_{PWM}			100		kΩ
FG/RD output low level	V_{FG/RD_LOW}	$I_{FG/RD}$ = 3mA			0.43	V
Switching frequency	f_{SW}	T_J = 25°C		24		kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 100mA		480		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 100mA		480		mΩ
Cycle-by-cycle current limit	I_{LIMIT}	CL = 1		1.2		A
Peak I_{LIMIT}	I_{LIMIT_PEAK}			1.8		A
Zero-current detection (ZCD) threshold	I_{ZCD}			0		mA
Soft-on commutate angle	θ_{SON}	SON = 0x10		46.4		deg
Soft-off commutate angle	θ_{SOFF}	SOFF = 0x10		46.4		deg
Hall lead/lag angle	θ_{HALL}	HAL_ANG = 0xF		21.8		deg
Locked-rotor detection time	t_{RD}			0.6		sec
Locked-rotor retry time	t_{RE}	LOCK_SEL = 0		3.6		sec
Over-voltage protection (OVP) threshold	V_{OVP_H}	OVP_DIS = 0, OVP_H = 1		31	34	V
	V_{OVP_L}	OVP_DIS = 1, OVP_H = 0		19	21	V
OVP hysteresis	V_{OVP_HYS}			2	3	V
Operating point	B_{OP}			1	2	mT
Release point	B_{RP}		-2	-1		mT
Thermal shutdown threshold	T_{SD}			165		°C
Thermal shutdown hysteresis	T_{SD_HYS}			20		°C

TYPICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

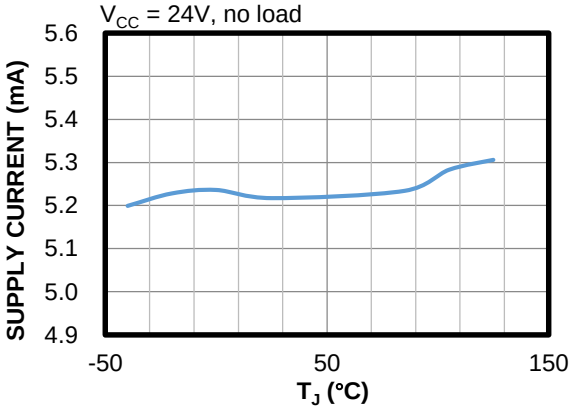
Supply Current vs. Input Voltage

V_{CC} = 2V to 35V, no load, T_J = 25°C

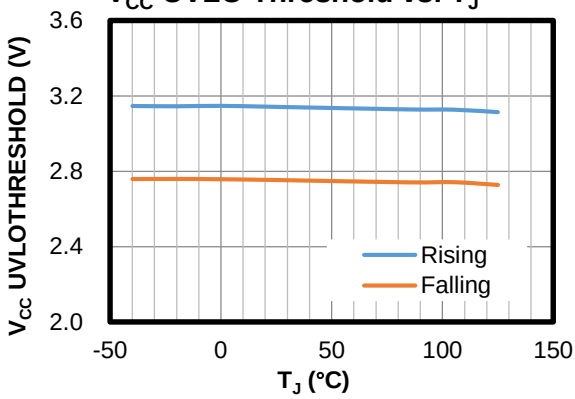


Supply Current vs. T_J

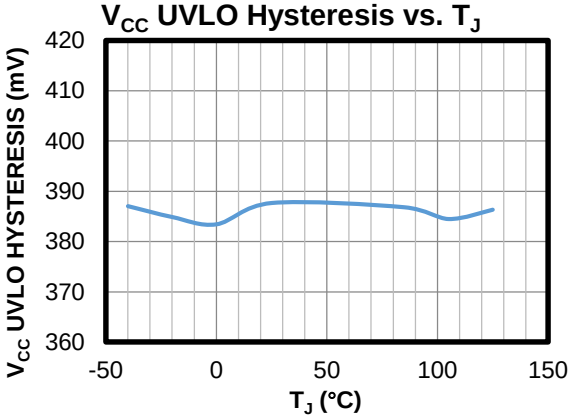
V_{CC} = 24V, no load



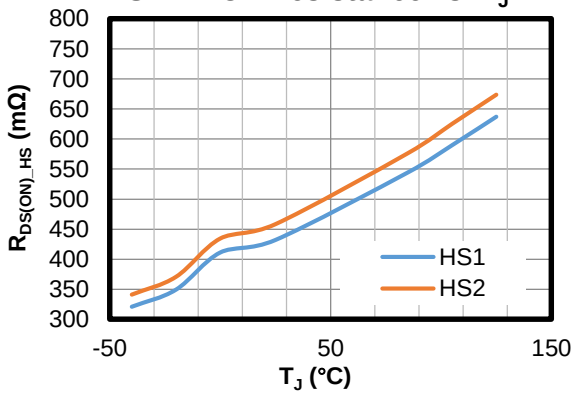
V_{CC} UVLO Threshold vs. T_J



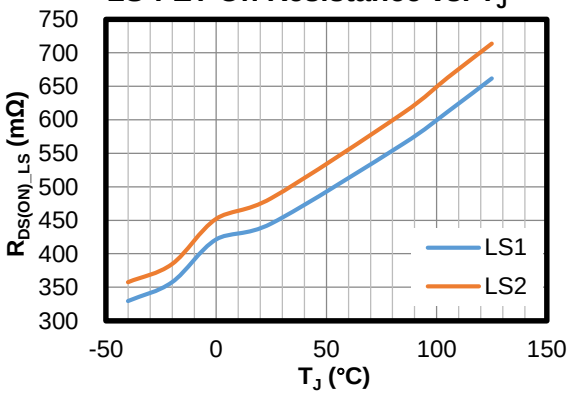
V_{CC} UVLO Hysteresis vs. T_J



HS-FET On Resistance vs. T_J



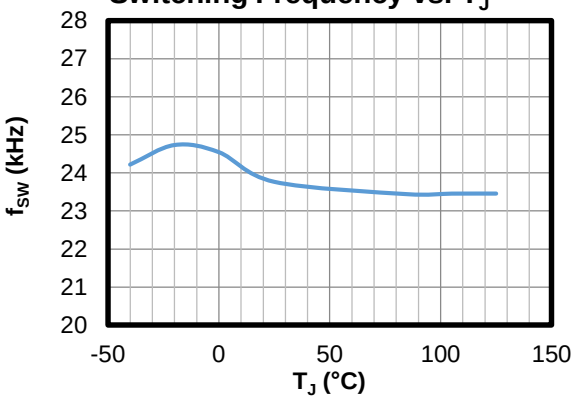
LS-FET On Resistance vs. T_J



TYPICAL CHARACTERISTICS *(continued)*

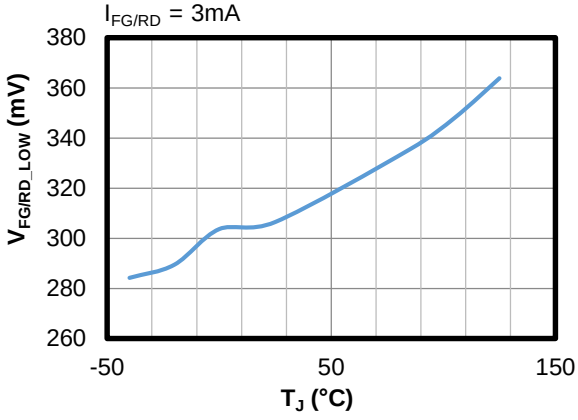
V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

Switching Frequency vs. T_J

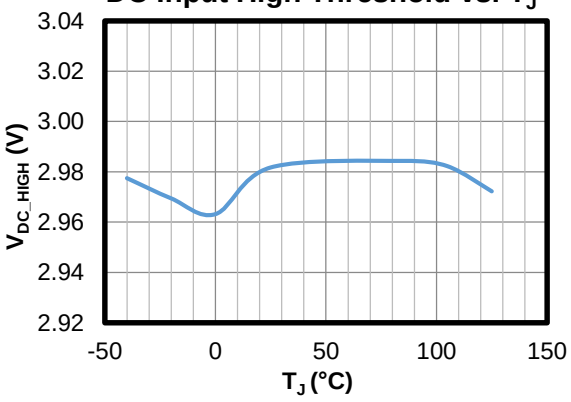


V_{FG/RD_LOW} vs. T_J

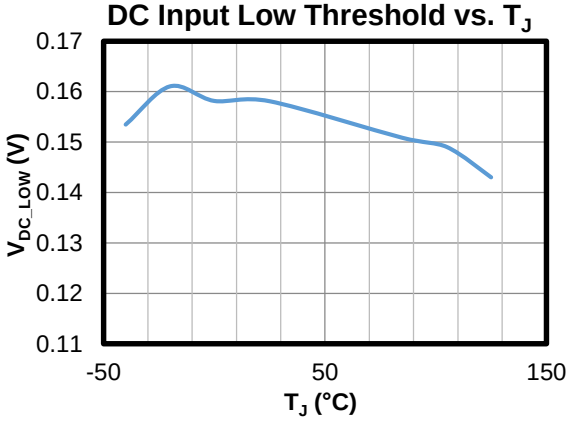
$I_{FG/RD}$ = 3mA



DC Input High Threshold vs. T_J

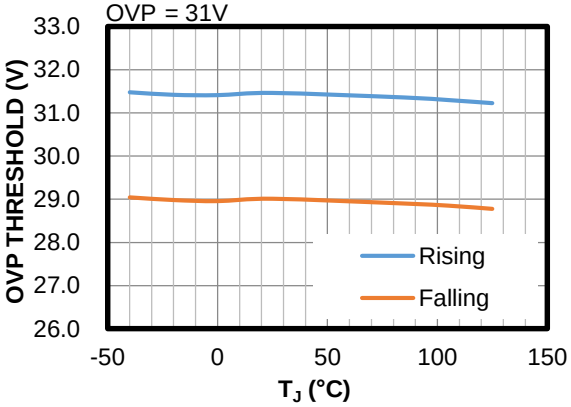


DC Input Low Threshold vs. T_J



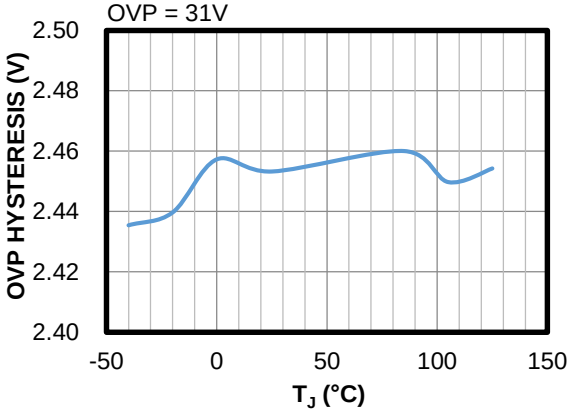
OVP Threshold vs. T_J

OVP = 31V



OVP Hysteresis vs. T_J

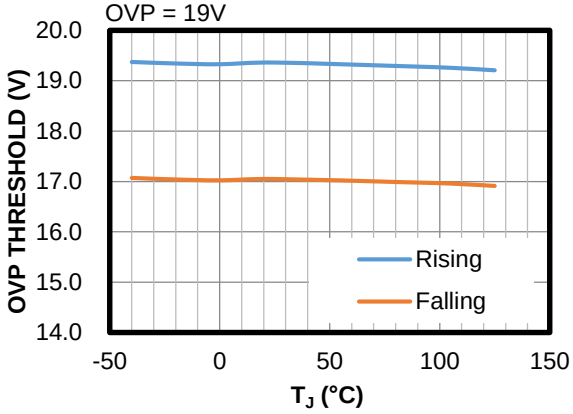
OVP = 31V



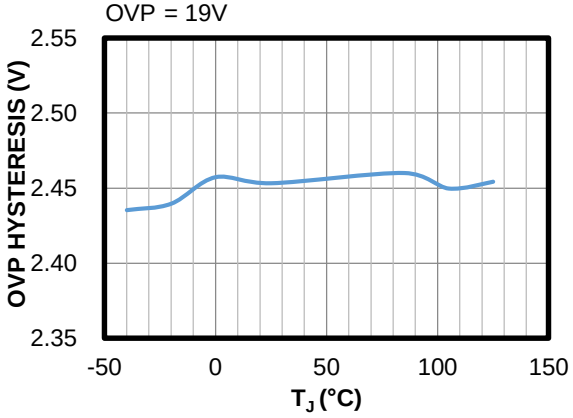
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

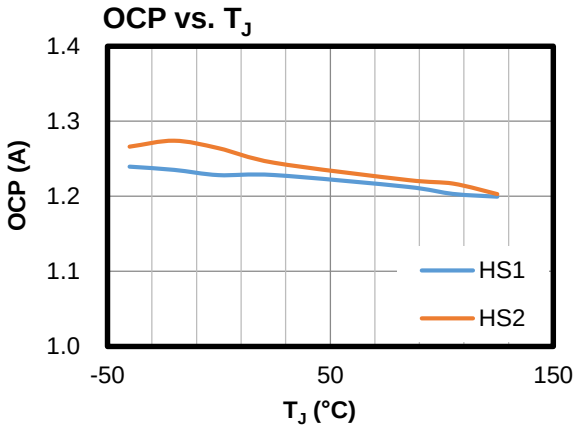
OVP Threshold vs. T_J



OVP Hysteresis vs. T_J



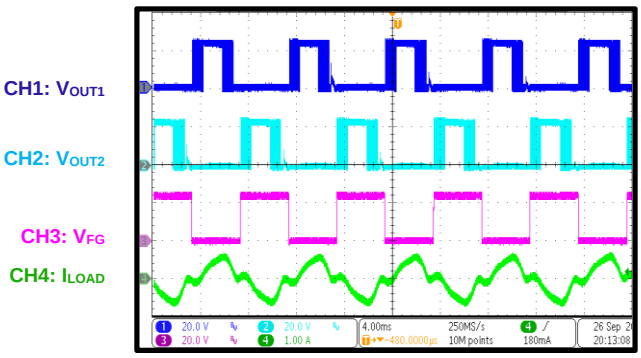
OCP vs. T_J



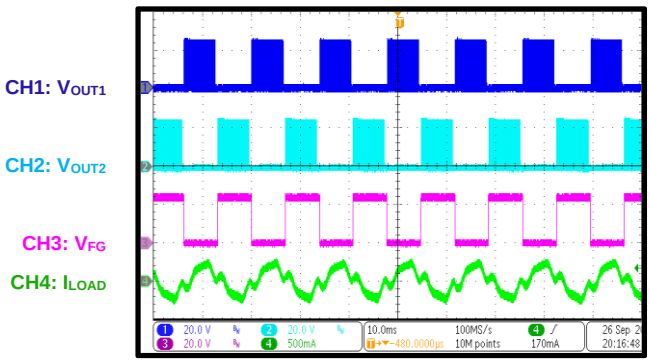
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

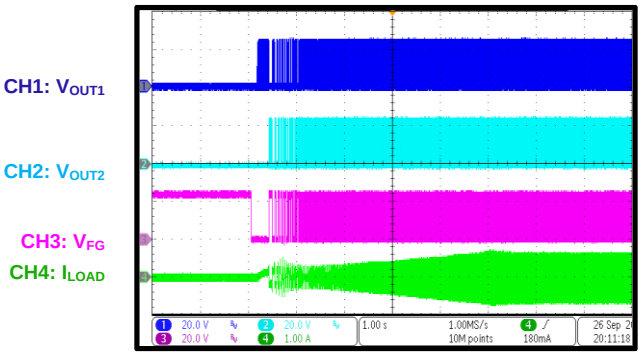
Steady State
PWM = 100%



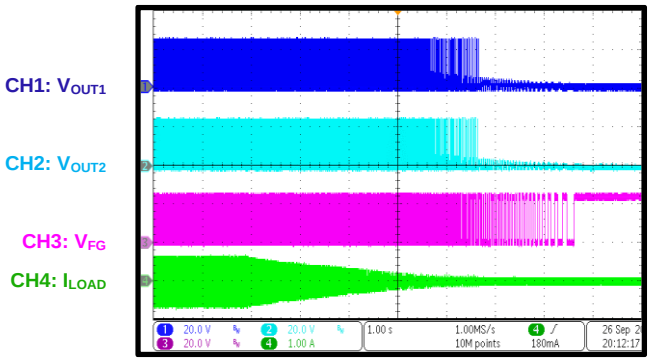
Steady State
PWM = 50%



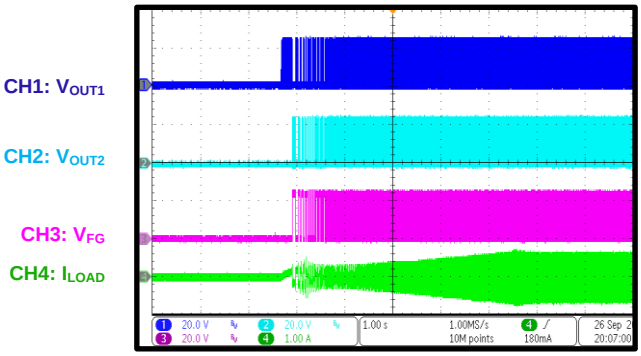
PWM On
PWM duty = 0% to 100%



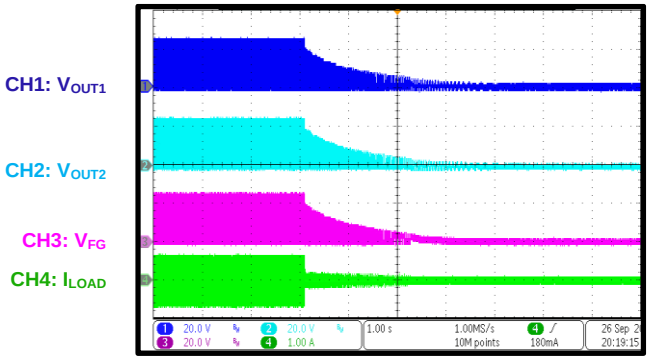
PWM Off
PWM duty = 100% to 0%



Start-Up through VC
VCC power is plugged in



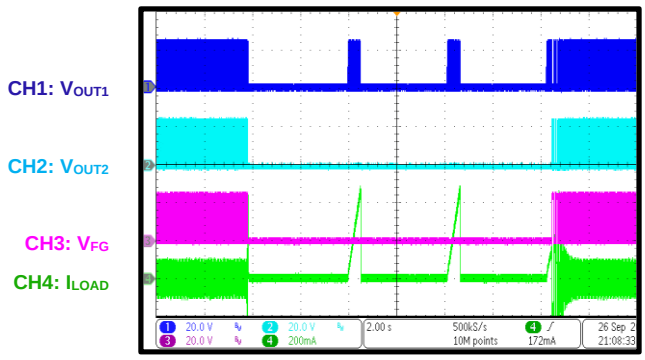
Shutdown through VCC
VCC power is not plugged in



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

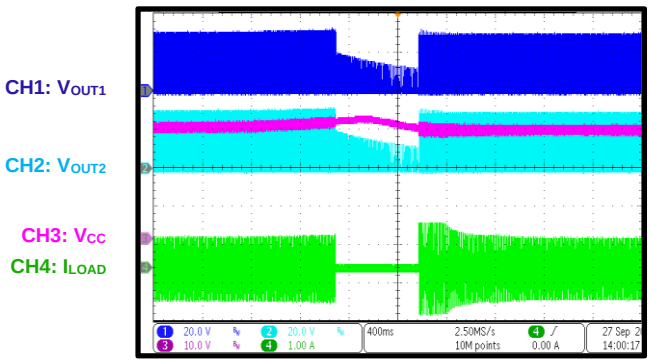
V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

Locked-Rotor Protection



Over-Voltage Protection

V_{CC} ramps up, then ramps down



FUNCTIONAL BLOCK DIAGRAM

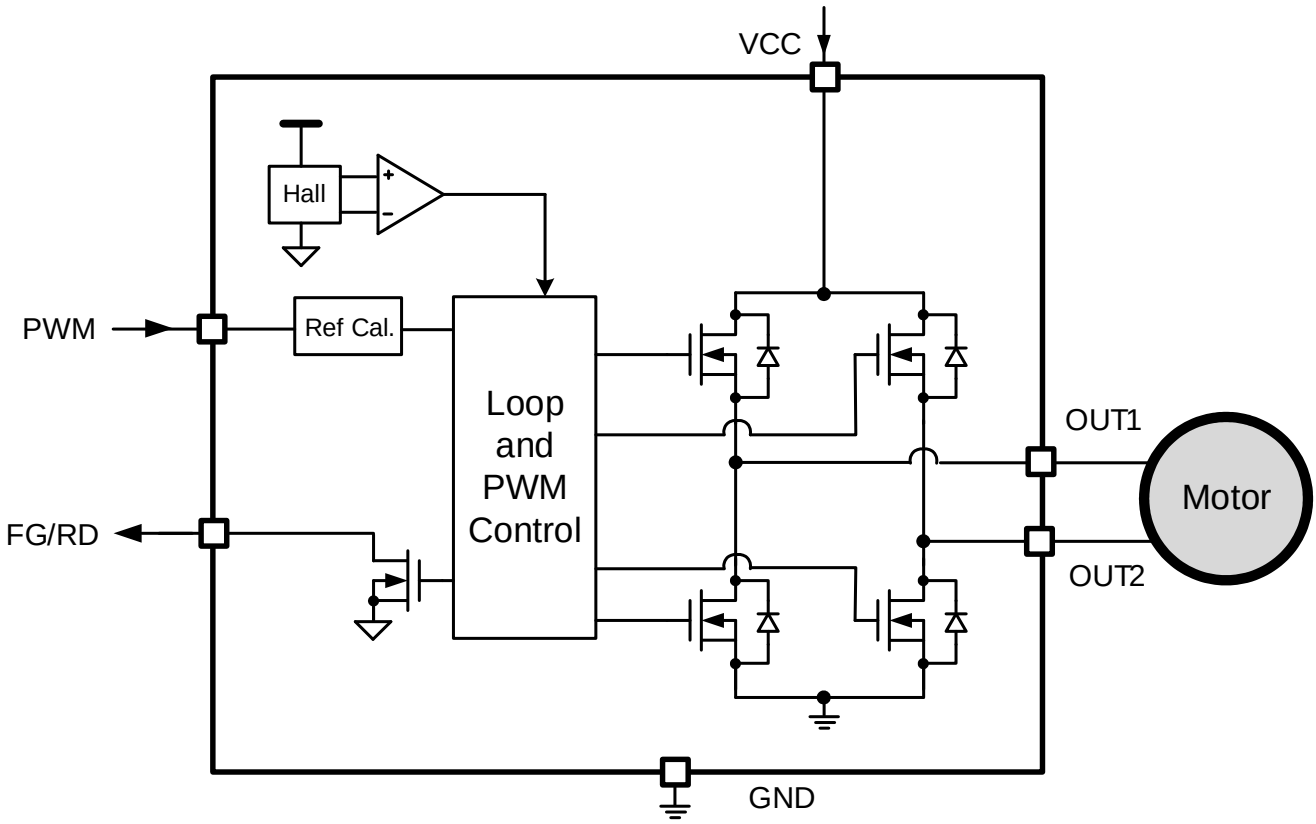


Figure 1: Functional Block Diagram

OPERATION

The MP6653 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall effect sensor. The MP6653 controls the motor speed through the pulse-width modulation (PWM) signal on the PWM pin. The device features configurable soft on/off commutation. The Hall offset angle can be flexibly configured to optimize performance.

The MP6653 also has the rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

Speed Control

The PWM signal or DC voltage applied on the PWM pin controls the motor rotating speed. A wide 50Hz to 100kHz PWM frequency range is available, depending on the register setting.

When LOW_F = 0, the PWM frequency range is 1kHz to 100kHz, and the PWM signal resolution is 163ns. When LOW_F = 1, the PWM frequency range is 50Hz to 2kHz, and the PWM signal resolution is 2.6μs.

If PWM input mode is selected, the PWM input duty cycle is detected, and the motor rotating speed is controlled by the PWM input duty cycle.

In DC input mode, the DC input voltage is detected and converted to a PWM duty cycle, controlling the rotating speed. The tolerance must be taken into consideration when DC input mode is selected.

The MP6653 supports either open-loop speed control or closed-loop speed control, depending on the register setting.

In open-loop speed control, the OUT1 and OUT2 output duty cycle is adjusted based on the PWM input duty cycle or DC input voltage on the PWM pin.

In closed-loop speed control, the PWM input duty cycle or DC input voltage is detected and converted to a reference speed. The motor's rotating speed is feedback to the control loop. The output duty cycle is adjusted by the control loop to make the rotating speed equal to the reference speed.

Starting Duty

The register bits D0 set the starting duty cycle when the input duty cycle is below the starting duty. The IC is not switching and the motor stops (see Figure 2).

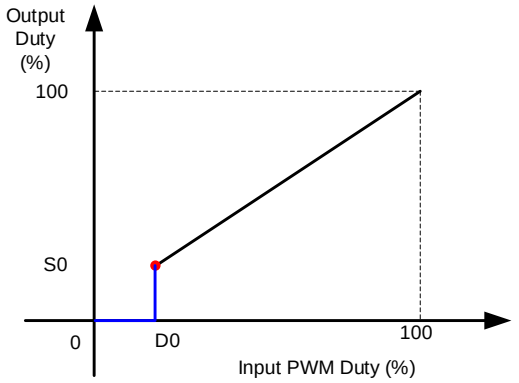


Figure 2: Minimum Speed

Stop Duty

The MP6653 supports fan stops when the PWM input duty cycle is above the stop duty cycle (see Figure 3).

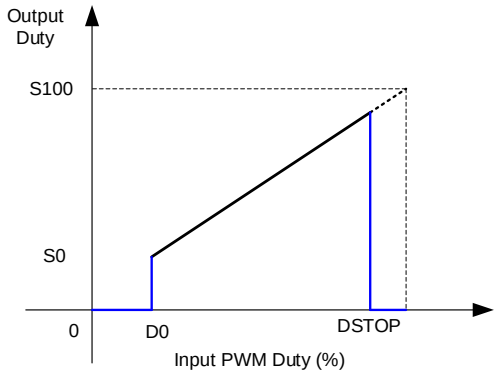


Figure 3: Stop at High Duty Cycle

The register bits configure the stop duty cycle, described below:

- If DSTOP = 00, there are no stops.
- If DSTOP=01, the stop duty cycle is 100%.
- If DSTOP=10, the stop duty cycle is 95%.

- If DSTOP=11, the stop duty cycle is 90%.

OUTx Normal Operation

Operation is based on the internal Hall sensor's output, the operating sequence is introduced in Figure 4 shows the operating sequence.

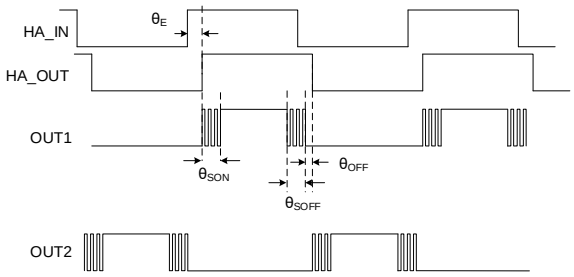


Figure 4: Operation with Hall Offset Angle

H_{A_IN} is the original Hall signal from the embedded Hall sensor. H_{A_OUT} is generated according to H_{A_IN} with a phase shift. The shifted phase (θ_E in Figure 4) is configured by the Hall offset angle register.

When the H_{A_OUT} signal is high, OUT2 remains at a constant low while OUT1 is the switching phase.

When the H_{A_OUT} signal is low, OUT1 remains at a constant low while OUT2 is the switching phase.

The Hall offset angle is dependent on HAL_ANG. The Hall offset angle lead/lag direction is set by the HAL_FLAG bit. When HAL_ANG = 0000, the Hall offset angle is 0°.

Soft-On Commutation

During soft-on commutation (θ_{SON} in Figure 4), the output duty cycle of the switching phase gradually increases from 0 to the target setting duty cycle, and the other phase keeps the low-side MOSFETs (LS-FETs) on.

The register bits SON[4:0] set the soft-on commutation angle. The soft-on commutation angle should be between 0° to 90°. A larger soft-on commutation angle leads to a lower rotating speed under the same conditions.

Soft-Off Commutation

During soft-off commutation (θ_{SOFF} in Figure 4), the switching phase's output duty cycle gradually decreases from the target setting duty cycle to 0, and the other phase keeps the LS-FETs on.

The register bits SOFF[4:0] set the soft-off commutation angle. The soft-off commutation angle should be between 0° to 90°. A larger soft-off commutation angle helps eliminate the reverse current; however, it also leads to a lower rotating speed under the same conditions.

Soft-On and Soft-Off Commutation Angle Linear Interpolation

The soft-on/off commutation angle can be set to linearly change when the output varies. The SON and SOFF bits set the soft-on and soft-off commutation angles, respectively, when the output duty is 100%. The commutation angle linearly increases to 90° when the output duty cycle decreases to 0° (see Figure 5).

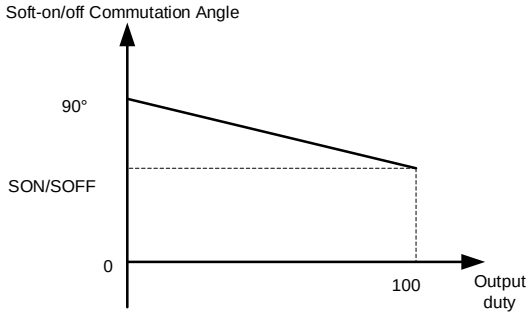


Figure 5: Soft-On/Off Commutation Angle Linear Interpolation

Curve Configuration

The MP6653 provides a curve configuration function. Either the output duty cycle (in open-loop control)/speed (in closed-loop control) or the PWM input duty cycle is configurable (see Figure 6.)

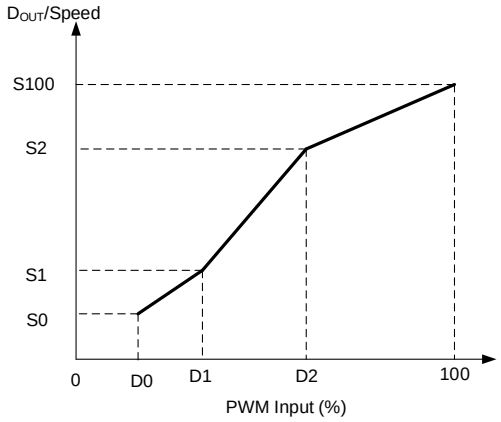


Figure 6: Curve Programming

The register bits S0[7:0], S1[7:0], S2[7:0], and S100[11:0] set the output duty cycle or speed when the input duty cycle is set via the D0[6:0], D1[7:0], D2[7:0] bits or is 100%, respectively.

The input duty cycle is set by Dx, which can be calculated with Equation (1):

$$\text{Input Duty Cycle} = Dx / 255 \quad (1)$$

Where x = 0, 1, and 2.

In open-loop speed control, the corresponding output duty is set by Sx, which can be calculated with Equation (2):

$$\text{Output Duty Cycle} = Sx / 255 \quad (2)$$

Where x = 0, 1, 2, and 100.

In closed-loop speed control, S100 sets the maximum speed when the input duty cycle is 100%. The other point speed can be calculated with Equation (3):

$$\text{Speed} = S100 \times Sx / 255 \quad (3)$$

Where x = 0, 1, and 2.

Standby Mode

If the VCC voltage (V_{CC}) exceeds the UVLO rising threshold and the PWM pin remains low, the IC is in standby mode. The IC exits standby mode when the PWM input signal is detected or the power is recycled.

Pre Start-Up

When V_{CC} exceeds the UVLO threshold or the PWM input duty exceeds the starting duty set by D0[7:0], the MP6653 enters into the pre start-up stage. The output duty increases with a set slope by ignoring the final steady state output duty cycle. After several Hall cycles, the MP6653 exits the pre start-up stage, and soft start (SS) begins.

With different pre start-up timer configurations, the MP6653 can provide enough torque to spin up the motor for different applications.

Soft Dynamic

After the pre start-up stage, SS is employed. The output duty cycle ramps up/down gradually according to TIME_SS.

To reduce the input inrush current during start-up, several configurations are available to meet different applications.

The duty cycle dropping can be configured as 1x or 2x of TIME_SS.

Rotor Speed Indicator (FG) or Locked-Rotor Indicator (RD)

The speed indicator or locked-rotor indicator can be output on the FG/RD pin with different configurations. The FGRD bits set the FG/RD pin's output.

If FGRD = 000, then the FG/RD pin outputs 1 pulse every electrical cycle (1x). If FGRD = 001, then the FG/RD pin outputs 1 pulse every 2 electrical cycles (1/2x). If FGRD = 010, then the FG/RD pin outputs 2 pulses every electrical cycle (2x).

If FGRD = 011, the FG/RD pin outputs 1 pulse every electrical cycle during normal operation, and outputs an RD signal in locked-rotor protection. The RD signal output polarity is set by the RD_H_L bit.

If FGRD = 100, the FG/RD pin is set as the locked-rotor indicator. The RD signal output polarity is set by the RD_H_L bit. If FGRD = 101, the FG/RD pin is set as the fault indicator, and outputs a signal when a fault is detected.

If FGRD = 110, the FG/RD pin is set as the external Hall signal input. The external Hall sensor replaces the internal Hall sensor during operation.

Protection Circuits

The MP6653 is fully protected against over-voltage, under-voltage, over-current, and over-temperature events.

Cycle-By-Cycle Current Limit (OCP)

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set by the CL bits after a blanking time, the HS-FET turns off immediately. The HS-FET resumes switching in the next switching cycle. The current-limit threshold can be set to 0.6A or 1.2A via the register.

Peak Current Limit (SCP)

If the current is not limited by the cycle-by-cycle limit, there is also a peak current limit. If the peak current limit threshold (typical 1.8A) is rescued, all MOSFETs turn off, then resume operation after a locked retry time.

Thermal Shutdown (TSD)

Thermal monitoring is integrated into the MP6653. If the die temperature exceeds 165°C, the MOSFETs of the switching half-bridge turn off. Operation automatically resumes once the die temperature falls to a safe level.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below the UVLO threshold at any time, all circuitry in the device is disabled and the internal logic is reset. Operation resumes when V_{CC} rises above the UVLO threshold.

Locked-Rotor Protection (RD)

The internal Hall signal is detected to judge whether locked-rotor protection is triggered. If no Hall signal edge is detected during the 0.6s detection time, the locked-rotor protection is triggered, and both LS-FETs of the H-bridge turn on. After a locked retry time set by the LOCK_SEL register, the IC automatically tries start-up. The locked retry time can be configured to 3.6s or 8.4s.

The MP6653 also supports options to retry several times; depending on the number of retry times, the locked retry time can become longer with the register configuration (see Figure 7).

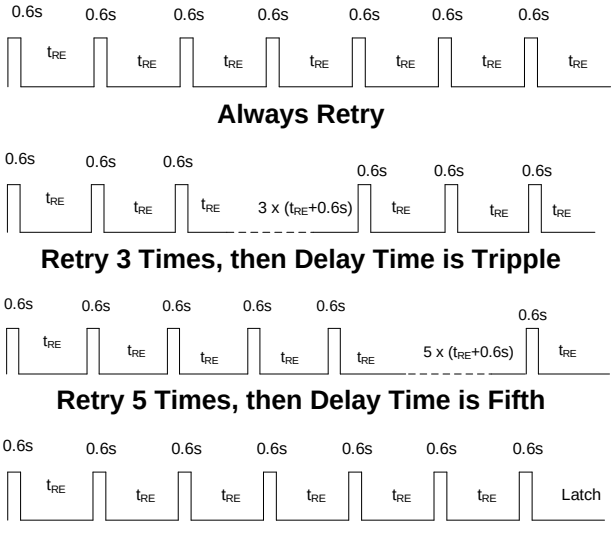


Figure 7: Lock Protection and Retry Time

The FG/RD pin releases only after 3 Hall signal edges are detected after the locked-rotor condition is released.

Over-Voltage Protection (OVP)

The MP6653 employs two over-voltage (OV) thresholds for different applications.

If V_{CC} exceeds the OV threshold (19V/31V), the output drive is disabled, one phase is kept floating, and the other phase's LS-FETs are on.

OVP can be configured to disable the outputs of OUT1/2 when OVP is triggered.

The MP6653 resumes normal operation when V_{CC} drops below the OVP falling threshold, and the Hall edge is detected during the OVP interval.

Fault Diagnosis

The OCP, SCP, TSD, OVP, RD has a relative fault bit to indicating the fault. The fault bit can be reset after the fault bit is read.

Test Mode and Factory Mode

To configure the internal register, the MP6653 has a test mode. In this test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM).

REGISTER MAP

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	S0[7:0]							
01h (OTP/REG)	S1[7:0]							
02h (OTP/REG)	S2[7:0]							
03h (OTP/REG)	S100[11:4]							
04h (OTP/REG)	D1[7:0]							
05h (OTP/REG)	D2[7:0]							
06h (OTP/REG)	RD_H_L	D0[6:0]						
07h (OTP/REG)	OVP_H	FAST_DN	PWM_POL	SON[4:0]				
08h (OTP/REG)	SINE	SPD_SEL[1:0]		SOFF[4:0]				
09h (OTP/REG)	WAIT_DIS	T_PRE[1:0]		HAL_FLAG	HAL_ANG[3:0]			
0Ah (OTP/REG)	RESERVED	INT_EN	RESERVED	LOCK_SEL	CL	RESERVED	PWM_WAIT	TADV_EN
0Bh (OTP/REG)	OVP_DIS	TADV[1:0]		TIME_SS[1:0]		FGRD[2:0]		
0Ch (OTP/REG)	PWM_DC	CLOSE	LOW_F	LOCK_BHV[1:0]		RESERVED	COA_SLOW	DN_SCAEL
0Dh (OTP/REG)	KI[6:0]							ZCD_POS
0Eh (OTP/REG)	RESERVED	FIX_ST	DSTOP[1:0]		S100[3:0]			
14h (REG)	OCP	SCP	OVP	TSD	RD	RESERVED		
15h (REG)	RESERVED	LOCK_DIS	RESERVED					
16h (REG)	RESERVED	OTP_PAGE[1:0]	RESERVED					

SPEED_CURVE_1 (00h)

The SPEED_CURVE_1 command configures output duty or speed when input PWM duty cycle = D0.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0[7:0]	0x20	Sets the output duty or speed when the input PWM duty =D0. For open-loop control, set the output duty when the input PWM duty = D0. Output duty = S0[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = D0. Speed = S0[7:0] / 256 x S100[11:0].

SPEED_CURVE_2 (01h)

The SPEED_CURVE_2 command configures output duty or speed when input PWM duty cycle =D1.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1[7:0]	0x60	Sets the output duty or speed when the input PWM duty =D1. For open-loop control, set the output duty when the input PWM duty = D1. Output duty = S1[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = D1. Speed = S1[7:0] / 256 x S100[11:0].

SPEED_CURVE_3 (02h)

The SPEED_CURVE_3 command configures output duty or speed when input PWM duty cycle =D2.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2[7:0]	0xC0	Sets the output duty or speed when the input PWM duty =D2. For open-loop control, set the output duty when the input PWM duty = D2. Output duty = S2[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = D2. Speed = S2[7:0] / 256 x S100[11:0].

SPEED_CURVE_4 (03h)

The SPEED_CURVE_4 command configures output duty or speed when input PWM duty cycle = 100%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S100[11:4]	0xFF	Sets the output duty or 8-bit most significant bit(MSB) of speed when the input PWM duty =100%. For open-loop control, set the output duty when the input PWM duty = 100%. Output duty = S100[11:4] / 256. For closed-loop control, set the maximum speed reference when the input PWM duty = 100%. Combined with S100[3:0] to set the maximum speed (electrical speed). The MAX speed = 16rpm / LSB.

SPEED_CURVE_5 (04h)

The SPEED_CURVE_5 command configures input duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D1[7:0]	0x60	Sets the input duty for curve programming. The input PWM duty = D1[7:0] / 256.

SPEED_CURVE_6 (05h)

The SPEED_CURVE_6 command configures input duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2[7:0]	0xC0	Sets the input duty for curve programming. The input PWM duty = D2[7:0] / 256.

CFR_1 (06h)

The control function register 1 (CFR_1) command sets RD/FT output polarity and starting corner duty.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_H_L	0	Selects RD/FT output polarity. 0: output low when protection is triggered (default) 1: output high when protection is triggered
6:0	R/W	D0[6:0]	0x20	Sets the starting corner duty for curve programming. The starting corner PWM duty = D0[6:0] / 256.

CFR_2 (07h)

The CFR_2 command sets OVP threshold, fast off, input PWM polarity and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_H	1	Selects the OVP threshold. 0:19V 1:31V (default)
6	R/W	FAST_DN	0	Fast-off enable bit. 0: Disable fast off (default) 1: Enable fast-off in PWM off. The IC quickly stops switching when the input duty cycle falls below the starting duty cycle
5	R/W	PWM_POL	0	Selects input PWM polarity. 0: Positive duty cycle (default) 1: Negative duty cycle.
4:0	R/W	SON[4:0]	0x10	Sets the soft-on commutation angle. 00000: 2.9° 00001: 5.8° …. 11111: 90° Soft-on angle = (SON[4:0]+1) x 2.9°. 2.9° per step.

CFR_3 (08h)

The CFR_3 command sets soft on/off mode, digital clock and soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	SINE	0	Selects soft on/off mode. 0: Linear (default) 1: Sine
6:5	R/W	SPD_SEL[1:0]	00	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds. 00: 200rpm (default electrical speed) 01: 800rpm 10: 1600rpm 11: 3200rpm

4:0	R/W	SOFF[4:0]	0x10	Sets the soft-off commutation angle. 00000: 2.9° 00001: 5.8° …. 11111: 90° The soft-off angle can be calculated with the following equation: Soft-Off Angle = (SOFF[4:0] + 1) x 2.9° 2.9° per step.

CFR_4 (09h)

The CFR_4 command sets waiting function, pre start-up timer and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	R/W	WAIT_DIS	0	The waiting function at start-up disable bit. 0: Enabled (default) 1: Disabled
6:5	R/W	T_PRE[1:0]	01	Selects the pre start-up timer. 00: 21.33ms/step 01: 10.67ms/step (default) 10: 5.36ms/step 11: 2.73ms/step
4	R/W	HAL_FLAG	0	Selects the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	R/W	HAL_ANG[3:0]	0000	Sets the Hall offset angle. 0000: 0° (default) 0001: 1.4° … 1111: 21° The Hall offset angle can be calculated with the following equation: Hall Offset Angle = HAL_ANG[3:0] x 1.4° 1.4° per step.

CFR_5 (0Ah)

The CFR_5 command sets soft on/off angle, lock retry time, current limit , waiting function and the advanced off function.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	INT_EN	0	Soft on/off commutation angle linear interpolation enable bit. 0: Disables soft-on/off commutation angle linear increase to 90° when duty drops. (default) 1: Enables soft-on/off commutation angle linear increase to 90° when duty drops.
5	R	RESERVED	1	Reserved.
4	R/W	LOCK_SEL	0	Selects the lock protection retry time. 0: 3.6s (default) 1: 8.4s

3	R/W	CL	1	Selects the current limit threshold. 0: 0.6A 1: 1.2A (default)
2	R	RESERVED	0	Reserved.
1	R/W	PWM_WAIT	0	The waiting function at PWM on start-up enable bit. 0: Disable (default) 1: Enable
0	R/W	TADV_EN	1	The advanced off enable bit. 0: disable the advanced off 1: enable the advanced off (default)

CFR_6 (0Bh)

The CFR_6 command sets OVP function, the advanced soft off angle, the soft start time and FG/RD pin.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_DIS	0	OVP disable bit. 0: Enables OVP (default) 1: Disables OVP
6:5	R/W	TADV[1:0]	00	Selects the advanced off angle. 00: Auto (default) 01: 5.6° 10: 11.2° 11: 22.5°
4:3	R/W	TIME_SS[1:0]	01	Selects the soft-start time. This is the time that it takes for the output duty to transition from 0 to 100%. 00: 2.73s 01: 5.46s (default) 10: 8.19s 11: 10.92s
2:0	R/W	FGRD[2:0]	000	Selects FG/RD pin. 000: 1xFG (default) 001: 0.5xFG 010: 2xFG 011: FG+RD. FG signal is output during normal operation. RD signal is output when lock protection is detected. 100: RD. The RD signal polarity is set by RD_H_L register. 101: FT. Fault signal is output when fault is detected. The FT polarity is set by RD_H_L register. 110: Hall_IN; the FG/RD pin is set as external Hall input pin

CFR_7 (0Ch)

The CFR_7 command sets PWM/DC input, open/close loop speed control, PWM frequency, lock protection mode, coasting down threshold and output duty ramp-down scale.

Bits	Access	Bit Name	Default	Description
7	R/W	PWM_DC	0	Selects DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
6	R/W	CLOSE	0	Closed-loop speed control enable bit. 0: Open-loop speed control (default) 1: Closed-loop speed control

5	R/W	LOW_F	0	Low frequency PWM input selection bit. 0: High frequency is selected, 1kHz to 100kHz (default) 1: Low frequency is selected, 50Hz to 2kHz
4:3	R/W	LOCK_BHV[1:0]	00	Selects lock behavior mode. 00: always retry (default) 01: retry for 3 times, then the lock retry time is 3x 10: retry for 5 times, then the lock retry time is 5x 11: retry for 7 times, then latch up
2	R	RESERVED	1	Reserved.
1	R/W	COA_SLOW	0	Selects the coasting down speed threshold (electrical speed) at which the fan speed drops below its speed, then the IC initiates a PWM cycle immediately after start-up. 0: 1400rpm (default) 1: 700rpm
0	R/W	DN_SCALE	0	Selects the PWM output duty ramp-down scale as the output duty cycle drops from 100% to 0%. 0: 1 x TIME_SS (default) 1: 2 x TIME_SS

CFR_8 (0Dh)

The CFR_8 command sets integral parameter for close-loop control and ZCD position.

Bits	Access	Bit Name	Default	Description
7:1	R/W	KI[6:0]	0x10	Integral parameter for closed-loop speed control.
0	R/W	ZCD_POS	0	Selects the angle position zero-current detection (ZCD). 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°.

CFR_9 (0Eh)

The CFR_9 command sets the initial output duty, stop input duty and maximum speed reference.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	FIX_ST	0	Selects the initial output duty at start-up. 0: Initial output duty is 0% (default) 1: Initial output duty is 12.5%
5:4	R/W	DSTOP[1:0]	00	Selects stop input duty. IC stops switching when the input PWM duty is equal or higher than setting. 00: No stop (default) 01: 100% 10: 95% 11: 90%
3:0	R/W	S100[3:0]	0000	Sets the maximum speed reference when the input PWM duty = 100% for closed-loop control, Combined with S100[11:4] to set the maximum speed (electrical speed). The MAX speed = 16rpm / LSB.

CFR_10(14h)

The CFR_10 command indicates faults including the cycle-by-cycle current limit (I_{OCP}), peak current limit (I_{LIMIT_PEAK}), input over-voltage (OV) conditions, thermal shutdown, and locked rotor.

Bits	Access	Bit Name	Default	Description
7	R	OCP	0	Indicates whether an I_{OCP} fault has occurred. 0: No I_{OCP} fault has occurred 1: An I_{OCP} fault has occurred
6	R	SCP	0	Indicates whether an I_{LIMIT_PEAK} fault has occurred. 0: No I_{LIMIT_PEAK} fault has occurred 1: An I_{LIMIT_PEAK} fault has occurred
5	R	OVP	0	Indicates whether an input over-voltage (OV) fault has occurred. 0: No input OVP has occurred 1: Input OVP has occurred
4	R	TSD	0	Indicates whether a thermal shutdown fault has occurred. 0: No thermal shutdown fault has occurred 1: A thermal shutdown fault has occurred
3	R	RD	0	Indicates whether a locked-rotor fault has occurred. 0: No locked-rotor fault has occurred 1: A locked-rotor fault has occurred
2:0	R	RESERVED	000	Reserved.

CFR_11 (15h)

The CFR_11 command disables locked-rotor protection.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	LOCK_DIS	0	Disables locked-rotor protection. 0: Enabled 1: Disabled
5:0	R	RESERVED	0x00	Reserved.

CFR_12 (16h)

The CFR_12 command indicates OTP memory.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6:5	R	OTP_PAGE[1:0]	00	Sets the OTP page indicator (read-only). 00: No OTP page is configured 01: First OTP page is configured 10: Second OTP page is configured
4:0	R	RESERVED	0x00	Reserved.

APPLICATION INFORMATION

Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{IN}) and reduce noise at the input. C_{IN} must have a low impedance at f_{SW}.

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

In some applications, an additional large, electrolytic capacitor may be required to absorb the motor's energy.

Input Snubber

An RC snubber is needed to dampen the peak voltage and current during hot plug-in. The RC snubber circuit also helps to depress the ringing during phase commutation.

Typically, a 2Ω resistor placed series with the input capacitor is sufficient for most applications. To improve the high-frequency noise (EMI consideration), a small size capacitor is recommended (see Figure 8).

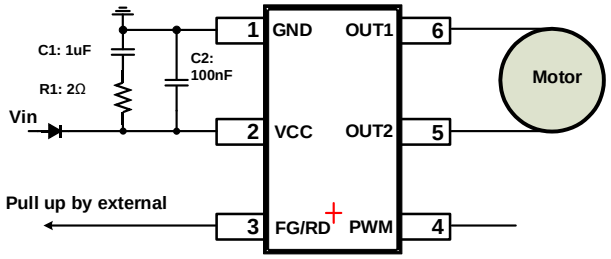
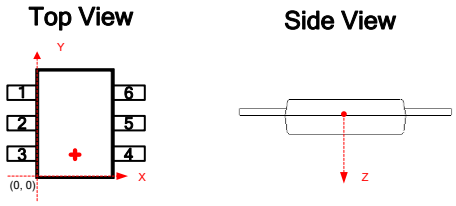


Figure 8: RC Snubber

Hall Position

Figure 9 shows the embedded Hall sensor cell location.



(X, Y, Z) = (800µm, 481µm, 80µm)

Figure 9: Hall Sensor Position

System-Level ESD Enhancement

Some fan products must pass system-level ESD testing. Compared to the HBM ESD ratings, system-level ESD follows the IEC61000-4-2 standard. There are two different modes for the IEC61000-4-2 ESD test: air discharge and contact discharge. Contact discharge mode is the first choice for testing.

Figure 10 shows the equivalent circuit of a HBM ESD circuit.

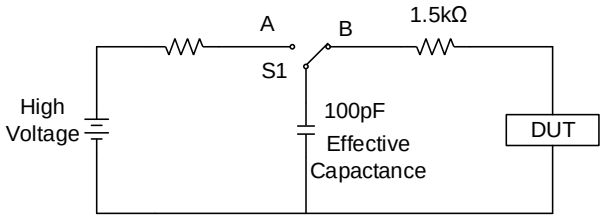


Figure 10: HBM ESD Circuit Equivalent Circuit

Figure 11 shows that the IEC61000-4-2 sets the equivalent circuit.

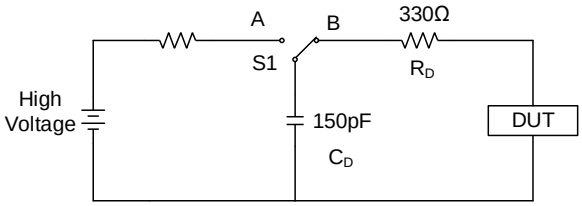


Figure 11: System-Level ESD Equivalent Circuit

Compared to the HBM ESD rating, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistor of the IEC level ESD is much smaller than the HBM. The surge current is much higher in the system-level ESD. An external Zener diode or ESD diode is required to enhance the system-level ESD rating (see Figure 12 on page 23).

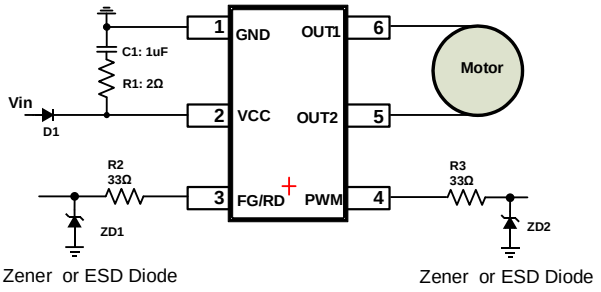


Figure 12: External ESD-Enhanced Circuit with a Zener Diode or ESD Diode

Selecting an Input Clamping Circuit

A voltage-clamping circuit may be required to prevent VCC being charged by the energy stored in the motor. Typically, a 28V SOD-123 Zener diode or TVS diode is sufficient for most 24V applications. A higher clamping voltage can be used if a higher input voltage range is applied.

Selecting the Reverse Blocking Diode

To avoid damage if the fan experiences a reverse plug-in, or reverse voltage applied on input terminal, a reverse blocking diode is required. The reverse blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's reverse voltage rating must be higher than maximum operating voltage under all conditions.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 13 and follow the guidelines below:

1. To improve EMI performance, a 0402 capacitor (C2) is required. Place the capacitor as close to VCC and GND pins as possible.
2. Place the RC snubber (C1 and R1) close the VCC and GND pins.

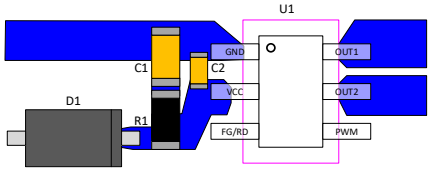


Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

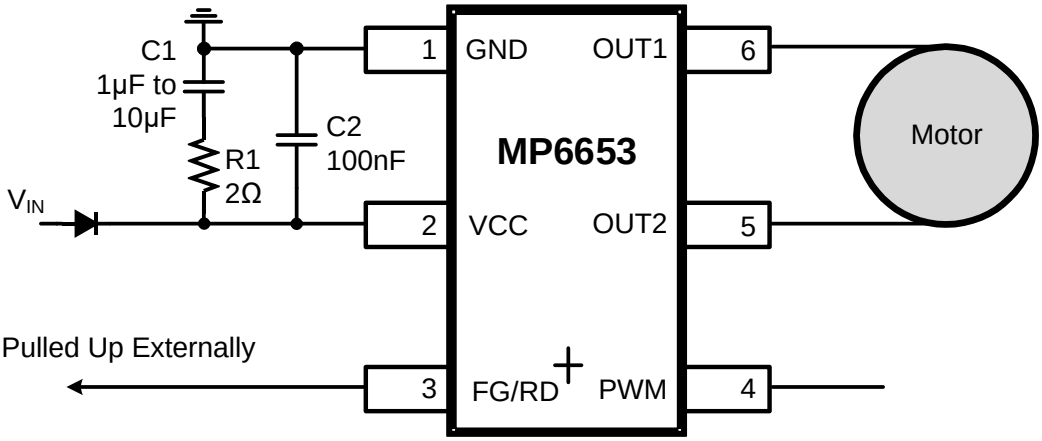


Figure 14: Typical Application Circuit

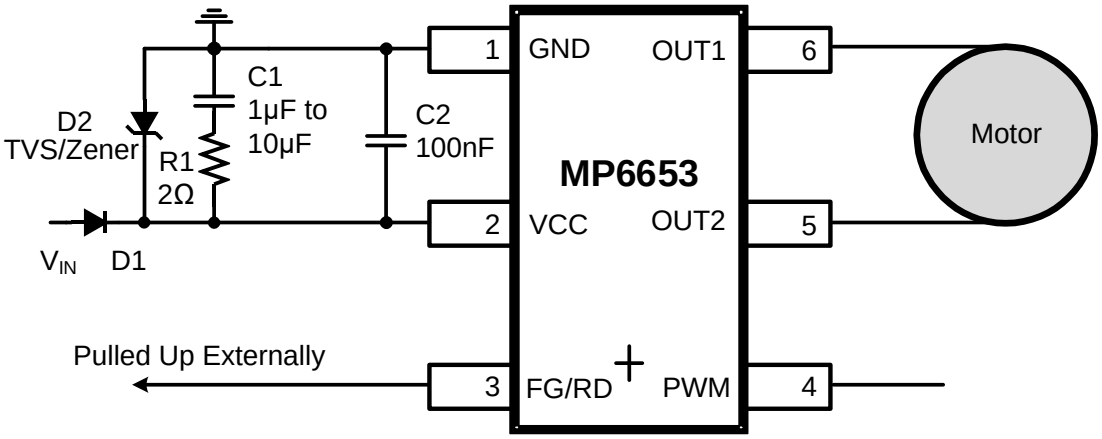


Figure 15: Typical Application Circuit with Voltage Clamping

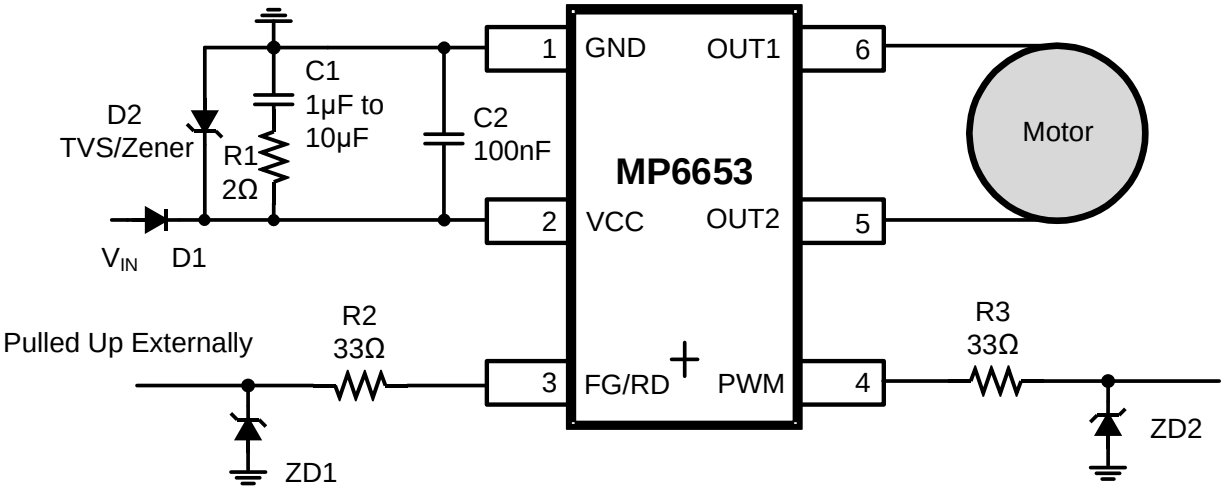
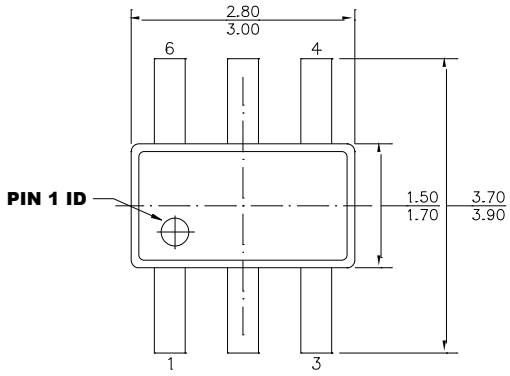


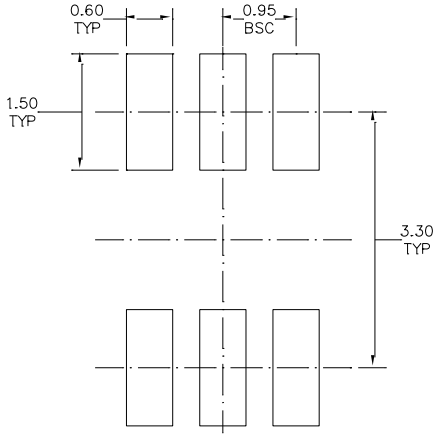
Figure 16: Typical Application Circuit with Voltage Clamping and ESD Enhancement

PACKAGE INFORMATION

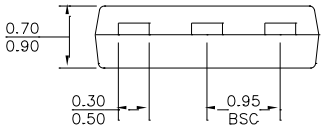
TSOT23-6-SL



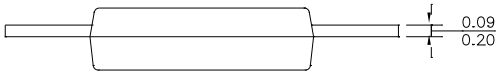
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



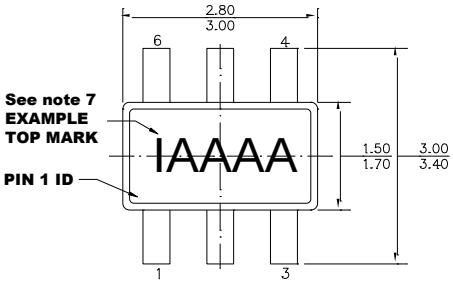
SIDE VIEW

NOTE:

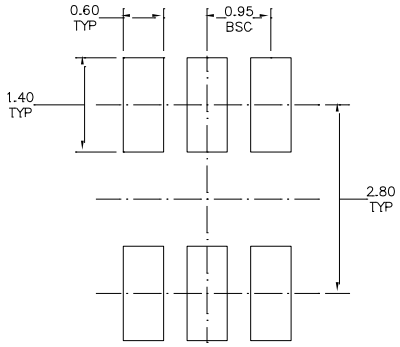
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

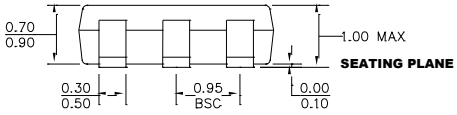
TSOT23-6-L



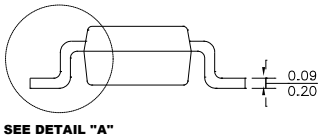
TOP VIEW



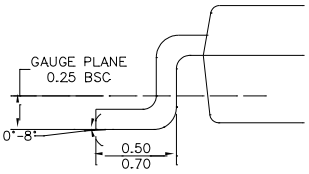
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

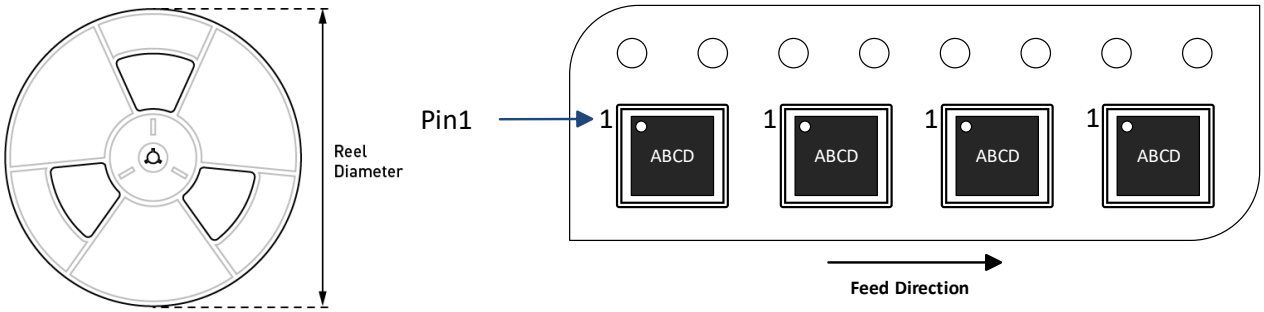


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6653GJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MP6653GJL-xxxx-Z	TSOT23-6-L	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/6/2024	Initial Release	-