



Micro Power Systems

T-51-10-12 **MP674**

Complete 12-Bit, 12  $\mu$ s  
Analog-to-Digital Converter  
with Microprocessor Interface

## FEATURES

- Complete 12-Bit A/D Converter with Reference Clock and Three-State Outputs
- Digital Error Correction
- Full 8, 12 or 16-Bit Microprocessor Bus Interface
- 100 ns Bus Access Time
- No Missing Codes over Temperature
- Minimal Setup Time for Control Signals
- 12  $\mu$ s typ. Conversion Time over Temperature
- Precision Reference for Long Term Stability and Low Gain Tempco
- Monolithic BiCMOS Construction
- Byte Enable/Short Cycle (A0 Input)
- ESD Protection: 1500 V Minimum

- Faster Version of the MP574A
- Low Power: 240 mW typ.
- Same Pin Out as MP574A
- Guaranteed Performance at  $\pm 12$  V and  $\pm 15$  V
- PDIP, SOIC & PLCC Packages Available

## APPLICATIONS

- Industrial Data Acquisition Systems
- High-Speed Electronics Test and Scientific Instrumentation
- Process Control Systems
- Digital Signal Processing

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## GENERAL DESCRIPTION

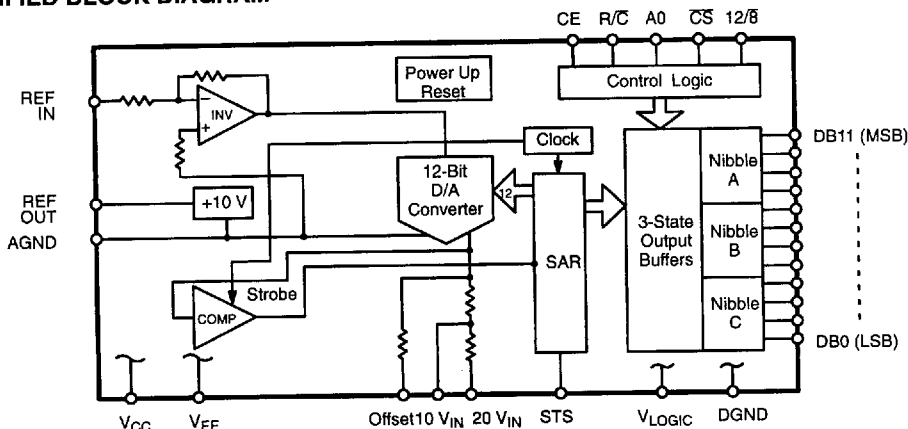
The MP674 is a complete 12-bit Successive Approximation Analog-to-Digital Converter with 3-state output buffers for direct interfacing to 8- and 16-bit microprocessor busses. The MP674 is implemented in advanced BiCMOS, the converter includes a digital error correction circuit. Micro Power Systems utilizes a proprietary decoding technique to improve drift performance and to guarantee no missing codes for all grades. Also, precision low temperature coefficient resistors are used to set critical performance parameters.

Designed for full scale range of  $\pm 20$  V,  $\pm 5$  V, +10 V, or +20 V,

the MP674 will operate with any supply voltage between  $\pm 12$  V and  $\pm 15$  V without special selection. Offset, linearity, and full-scale errors are minimized by laser trimming. To improve digital noise immunity and ease the digital interface, all digital inputs and outputs have been designed for true TTL compatibility.

Specified for operation over the commercial (0 to +70°C) temperature range, the MP674 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC) and Plastic Leaded Chip Carrier (PLCC) packages.

## SIMPLIFIED BLOCK DIAGRAM



# MP674

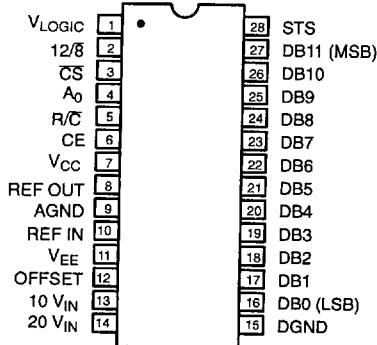


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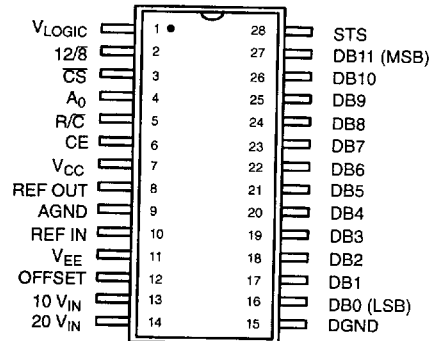
## ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	0 to 70°C	MP674JN	±1	±1	0.3
Plastic Dip	0 to 70°C	MP674KN	±1/2	±1	0.3
SOIC	0 to 70°C	MP674JS	±1	±1	0.3
SOIC	0 to 70°C	MP674KS	±1/2	±1	0.3
PLCC	0 to 70°C	MP674JP	±1	±1	0.3
PLCC	0 to 70°C	MP674KP	±1/2	±1	0.3

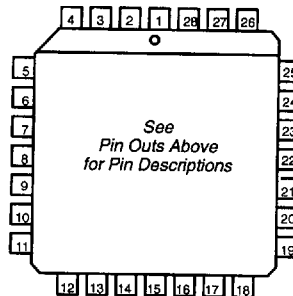
## PIN CONFIGURATIONS



28 Pin PDIP, (0.600")  
N28



28 Pin SOIC, (Jedec, 0.300")  
S28



28 Pin PLCC  
P28



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## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V <sub>LOGIC</sub>	+5 V Logic Supply
2	12/8	Select Format of Output Bits (8 or 12) (TTL Compatible)
3	$\overline{CS}$	Chip Select. Enables Conversions on Falling Clock Edge
4	A0	Access High 8 Bits or Low 4 Bits Plus 4 Zeroes (Read Mode)
5	R/ $\overline{C}$	Read/Convert: Main Control for Stand-Alone Operation
6	CE	Chip Enable. Enables Conversion on Rising Clock Edge
7	V <sub>CC</sub>	+12 V to +15 V
8	REF OUT	Output from Internal +10 V Reference

PIN NO.	NAME	DESCRIPTION
9	AGND	Analog Ground
10	REF IN	Input for Voltage Reference
11	V <sub>EE</sub>	-12 V to -15 V
12	OFFSET	Voltage Input for Bipolar Operations, or Zero Adjust
13*	10 V <sub>IN</sub>	Input for 0 to +10 V or -5 V to +5 V Operation
14	20 V <sub>IN</sub>	Input for 0 to +20 V or -10 V to +10 V
15	DGND	Digital Ground
16-27	Output Data Bits	DB0 (LSB) to DB11 (MSB)
28	STS	Status Flag

\* When not in use, NC to avoid noise pick-up.

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## DEFINING THE CONTROL FUNCTIONS

FUNCTION	DEFINITION	FUNCTION
CE	Chip Enable	<ol style="list-style-type: none"> <li>Typically used as clock synchronization with <math>\mu</math>p.</li> <li>Must be high (1) for a conversion to start.</li> <li>Must be high (1) to read data on the output.</li> <li><math>\uparrow</math> Transition may be used to initiate conversion.</li> </ol>
$\overline{CS}$	Chip Select	<ol style="list-style-type: none"> <li>Typically the address pin when used with a microprocessor.</li> <li>Must be low (0) for a conversion to start.</li> <li><math>\downarrow</math> Transition may be used to initiate conversion.</li> </ol>
R/ $\overline{C}$	Read/Convert	<ol style="list-style-type: none"> <li><math>\downarrow</math> Initiate conversion.</li> <li><math>\uparrow</math> Initiate read.</li> </ol>
A0	Address	<ol style="list-style-type: none"> <li>Selects conversion mode 12 Bits if low (0) 8 Bits if high (1).</li> <li>In read mode A0 selects the output format. If low (0) then 8 MSB's (high and middle byte) are enabled. If high (1) then the 4 LSB's are enabled.</li> </ol>
12/8	Output Format	<ol style="list-style-type: none"> <li>Usually hard-wired.</li> <li>Normal 12-Bit format if high (1).</li> <li>8-Bit format as set by A0 if low (0).</li> </ol>

\* When not in use, NC to avoid noise pick-up.

## MP674



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## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $V_{CC} = +15\text{ V}$ ,  $V_{\text{LOGIC}} = +5\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>KEY FEATURES</b>								
Resolution		12			12		Bits	FSR = Full Scale Range
<b>ACCURACY (K Grade)</b>								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1/2		±1/2	LSB	
Unipolar Offset	UOZT			±2		±2	LSB	Adjustable to Zero
Bipolar Offset <sup>1</sup>	BOZT			±4		±4	LSB	Adjustable to Zero
Full Scale Calibration Error (with fixed 50Ω resistor from REF OUT to REF IN)	FSE			±0.3		±0.3	% FSR	Adjustable to Zero
Tempco <sup>2</sup>								
Unipolar Offset	TCUOZT					±1 (5)	LSB	(ppm/°C)
Bipolar Offset	TCBOZT					±1 (5)	LSB	(ppm/°C)
Full Scale Calibration	TCFSE					±5 (27)	LSB	(ppm/°C)
<b>ACCURACY (J Grade)</b>								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Unipolar Offset	UOZT			±2		±2	LSB	Adjustable to Zero
Bipolar Offset <sup>1</sup>	BOZT			±4		±4	LSB	Adjustable to Zero
Full Scale Calibration Error (with fixed 50Ω resistor from REF OUT to REF IN)	FSE			±0.3		±0.3	% FSR	Adjustable to Zero
Tempco <sup>2</sup>								
Unipolar Offset	TCUOZT					±2 (10)	LSB	(ppm/°C)
Bipolar Offset	TCBOZT					±1 (10)	LSB	(ppm/°C)
Full Scale Calibration	TCFSE					±5 (50)	LSB	(ppm/°C)
<b>POWER SUPPLY REJECTION</b>								
Max Change in FS Calibration $V_{CC} = 15\text{ V} \pm 1.5\text{ V}$ or $12\text{ V} \pm 0.6\text{ V}$ J Grade K Grade $V_{\text{LOGIC}} = 5\text{ V} \pm 0.5\text{ V}$				±2 ±1 ±1/2		±2 ±1 ±1/2	LSB LSB LSB	
<b>ANALOG INPUT</b>								
Input Ranges	$A_{\text{IN}}$							
Bipolar 10 $V_{\text{IN}}$		-5		5	-5	5	V	
20 $V_{\text{IN}}$		-10		10	-10	10	V	
Unipolar 10 $V_{\text{IN}}$		0		10	0	10	V	
20 $V_{\text{IN}}$		0		20	0	20	V	
Input Impedance	$R_{\text{IN}}$							
10 $V_{\text{IN}}$		3	5	7	3	7	kΩ	
20 $V_{\text{IN}}$		6	10	14	6	14	kΩ	
<b>DIGITAL INPUTS<sup>3</sup></b>								
Logical "1" Voltage	$V_{\text{IH}}$	2.0			2.0		V	Inputs CE, CS, R/C, A0, 12/8
Logical "0" Voltage	$V_{\text{IL}}$			0.8		0.8	V	
Current	$I_{\text{IN}}$	-5	0.1	5	-5	5	μA	
Capacitance <sup>4</sup>	$C_{\text{IN}}$		5				pF	



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## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C			Tmin to Tmax		Units	Conditions
		Min	Typ	Max	Min	Max		
<b>DIGITAL OUTPUTS</b>								
Logical "1" Voltage	V <sub>OH</sub>	2.4			2.4		V	DB11-DB0, STS I <sub>SOURCE</sub> = ≤ 500μA I <sub>SINK</sub> = ≤ 1.6mA DB11-DB0, Hi-Z State
Logical "0" Voltage	V <sub>OL</sub>			0.4		0.4	V	
Output Leakage	I <sub>OL</sub>	-5		5	-5	5	μA	
Capacitance <sup>4</sup>	C <sub>O</sub>		5				pF	
<b>POWER SUPPLIES</b> (Tmin to Tmax)								
Operating Range								
V <sub>LOGIC</sub>	V <sub>LL</sub>	4.5		5.5	4.5	5.5	V	
V <sub>CC</sub>	V <sub>CC</sub>	11.4		16.5	11.4	16.5	V	
V <sub>EE</sub>	V <sub>EE</sub>	-11.4		-16.5	-11.4	-16.5	V	
Operating Current								
I <sub>LOGIC</sub>			3	6		8	mA	
I <sub>CC</sub>			7	10		12	mA	
I <sub>EE</sub>			8	12		14	mA	
<b>POWER DISSIPATION</b>								
V <sub>LOGIC</sub> = +5 V, V <sub>CC</sub> = +15 V, V <sub>EE</sub> = -15 V	P <sub>D</sub>		240	360		430	mW	
V <sub>LOGIC</sub> = +5 V, V <sub>CC</sub> = +12 V, V <sub>EE</sub> = -12 V			200	300		360	mW	
<b>INTERNAL REFERENCE</b>								
Reference Voltage	V <sub>REF</sub>	9.95	10.00	10.05	9.95	10.05		External load should not change during conversion
Output Current (External Load)	I <sub>REF</sub>	1.5	5		1.5		mA	

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## NOTES

- (1) Bipolar offset zero transition.
- (2) ppm/°C information for reference only.
- (3) Detailed timing specifications appear in the timing section.
- (4) Guaranteed, but not production tested.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V <sub>CC</sub> to DGND	0 to +16.5 V	20 V <sub>IN</sub> to AGND	±24 V
V <sub>EE</sub> to DGND	0 to -16.5 V	REF OUT	Indefinite short to DGND, Momentary short to V <sub>CC</sub>
V <sub>LOGIC</sub> to DGND	0 to +7 V	Package Power Dissipation Rating to 75°C	
AGND to DGND	±1 V	PDIP, SOIC, PLCC	1000mW
Control Inputs (CE, CS, AO, 12/8, R/C) to DGND	-0.5 V to V <sub>LOGIC</sub> + 0.5 V	Derates above 75°C	14mW/°C
Analog Inputs (REF IN, OFFSET, 10 V <sub>IN</sub> ) to AGND	±16.5 V	Lead Temperature, Soldering	+300°C, 10 Sec
		Storage Temperature	-65°C to +150°C

## NOTES:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

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## APPLICATION DATA

The MP674 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor which can control both conversion and formatting of output.

Successful application of the MP674 requires careful attention to four main areas:

- 1) Physical layout.
- 2) Connection/Trimming according to mode of operation.
- 3) Conditioning of input signals.
- 4) Controlling and timing considerations.

### Physical Layout

The 12-bit accuracy of the MP674 represents a dynamic range of 72dB. In order that this be preserved, thorough precautions must be taken to avoid any interfering signals, whether conducted or radiated. It is therefore recommended that one:

- Avoid placing the device and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1  $\mu$ F ceramic cap and a 10-47  $\mu$ F tantalum type, in parallel.
- Use well-regulated and filtered power supplies.

### Connection/Trimming

There are two modes of operation, each with two submodes, Unipolar, 0 to +10 V or 0 to +20 V; and Bipolar, -5 V to +5 V or -10

V to +10 V. If the accuracy of the MP674 as supplied is sufficient for the application, connect the device as shown in *Figures 1 & 2*.

If greater accuracy is required, the part may be trimmed. The procedure is as follows:

**Unipolar Mode:** Connect MP674 as shown in *Figure 3*. R1 is used to adjust the converter offset so that an input voltage equivalent to 1/2 LSB will produce the first change in the output codes (0000 0000 0000 to 0000 0000 0001). This input is 1.22 mV for the 10 V scale (pin 13) or 2.44 mV for the 20 V scale (pin 14). Using one of these inputs, R1 should be adjusted until the output flickers between the above code values.

Having trimmed zero scale (adjusted the offset), the all "-1"s level can be set using R2 (gain adjust). Apply an input of 9.9963V to pin 13 (or 19.9927V to pin 14). This is 1.5 or 1 1/2 LSB less than 10 V (20 V). Adjust R2 until the output flickers between codes 1111 1111 1110 and 1111 1111 1111.

**Bipolar Mode:** In the bipolar mode the user can either adjust the  $\pm$  Fullscale limits, or adjust the zero transition and gain ( $\pm$  Fullscale), as is best suited to the end application.

1. To set  $\pm$  Fullscale: Connect MP674 as shown in *Figure 4*. Apply -4.9988 V to pin 13 (or -9.9976 V to pin 14) and adjust R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1110 and 1111 1111 1111.
2. To set Zero Transition and Gain: Connect MP674 as shown in *Figure 4*. Apply 0.0000V to pin 13 (for +5 V fullscale applications) or pin 14 (for +10 V fullscale systems) and adjust R1 until the output code flickers between 0111 1111 1111 and 1000 0000 0000. Then apply +4.9963 V to pin 13 (or +9.9927 V to pin 14) and adjust R2 for flicker between output codes 1111 1111 1111 and 1111 1111 1110.

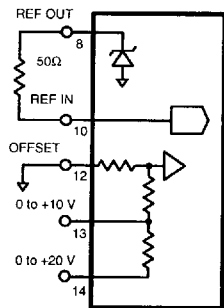


Figure 1. Unipolar Operation

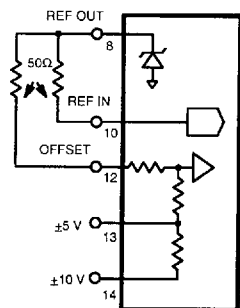


Figure 2. Bipolar Operation

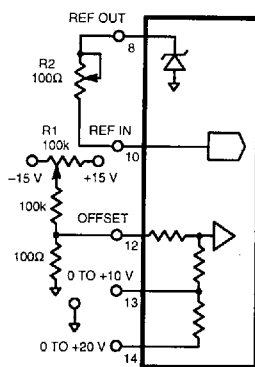


Figure 3. Unipolar Operation with Trim Adjustments

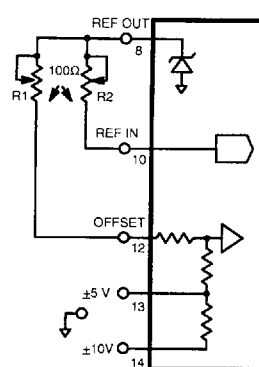


Figure 4. Bipolar Operation with Trim Adjustments



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## Control and Timing Considerations

The MP674 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 5 control lines: CE,  $\overline{CS}$ , R/C, A0 and 12/8 with their functions described in the box "Defining the Control Functions". The role each line plays in control is shown in the MP674 Truth Table.

### TRUTH TABLE

Control Inputs					MP674 Operation
CE	$\overline{CS}$	R/C	12/8	A0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	↓	X	0	Initiates 12-Bit Conversion
1	0	↓	X	1	Initiates 8-Bit Conversion
↑	0	0	X	0	Initiates 12-Bit Conversion
↑	0	0	X	1	Initiates 8-Bit Conversion
1	↓	0	X	0	Initiates 12-Bit Conversion
1	↓	0	X	1	Initiates 8-Bit Conversion
1	0	↑	1	X	Enables 12-Bit Parallel Output
1	0	↑	0	0	Enables 8 MSBs
1	0	↑	0	1	Enables 4 LSBs and 4 Trailing Zeros

### TIMING

The MP674 is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the MP674 control signals will provide the system designer with useful insight into the operation of the device.

Figure 5. shows a complete timing diagram for the MP674 convert start operation. R/C should be low before both CE and

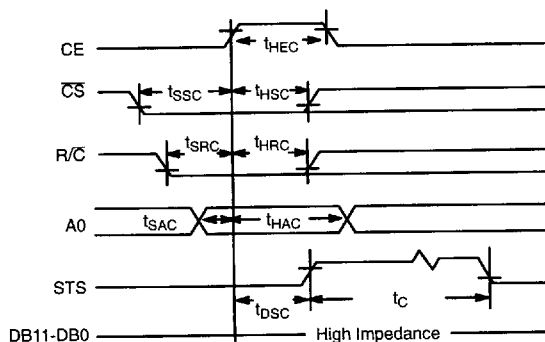


Figure 5. Convert Start Timing

$\overline{CS}$  are asserted; if R/C is high, a read operation will momentarily occur, possibly resulting in system bus contention.

Either CE or  $\overline{CS}$  may be used to initiate a conversion. We recommend using CE, however, as it includes one less propagation delay than  $\overline{CS}$ . As shown in Figure 5., CE is used. If  $\overline{CS}$  is used to trigger the conversion the specified set-up times will be longer.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The output data buffers cannot be enabled during conversion. However, all inputs and outputs which change during conversion can introduce noise.

### CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
$t_{DSC}$	STS Delay from CE	-	80	200	ns
$t_{HEC}$	CE Pulse Width	50	40	-	ns
$t_{SSC}$	$\overline{CS}$ to CE Setup	50	20	-	ns
$t_{HSC}$	$\overline{CS}$ Low During CE High	50	25	-	ns
$t_{SRC}$	R/C to CE Setup	50	0	-	ns
$t_{HRC}$	R/C Low During CE High	50	25	-	ns
$t_{SAC}$	A0 CE Setup	0	0	-	ns
$t_{HAC}$	A0 Valid During CE High	50	30	-	ns
$t_c$	Conversion Time				
	8-Bit Cycle	3	5	10	$\mu$ s
	12-Bit Cycle	6	12	15	$\mu$ s

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Figure 6. shows the timing for data read operations. The MP674 features fast access times and short data latency times. This simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/C both are high (assuming  $\overline{CS}$  is already low).

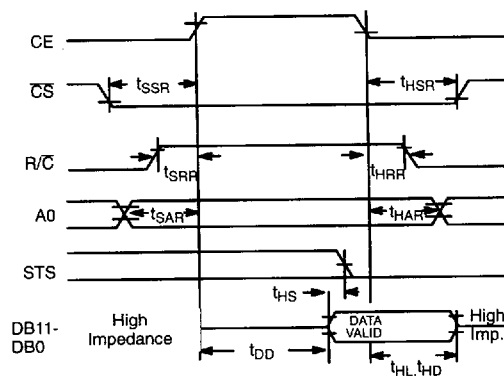


Figure 6. Read Cycle Timing

# MP674

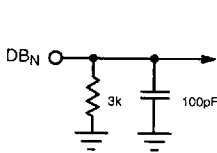


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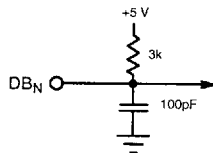
## READ TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
$t_{DD1}$	Access Time (from CE)	–	80	150	ns
$t_{HD}$	Data Valid after CE Low	25	35	–	ns
$t_{HL2}$	Output Float Delay	–	60	150	ns
$t_{SSR}$	$\overline{CS}$ to CE Setup	50	0	–	ns
$t_{SRR}$	R/ $\overline{C}$ to CE Setup	0	0	–	ns
$t_{SAR}$	A0 to CE Setup	50	25	–	ns
$t_{HSR}$	$\overline{CS}$ Valid After CE Low	0	0	–	ns
$t_{HRR}$	R/ $\overline{C}$ High After CE Low	0	0	–	ns
$t_{HAR}$	A0 Valid After CE Low	50	25	–	ns

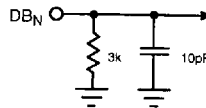
- $t_{DD}$  is measured with the load circuit of Figure 7, and defined as the time required for an output to cross 0.4 V or 2.4 V.
- $t_{HL}$  is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 8.



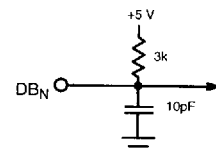
a. High-Z to Logic 1



b. High-Z to Logic 0



a. Logic 1 to High-Z

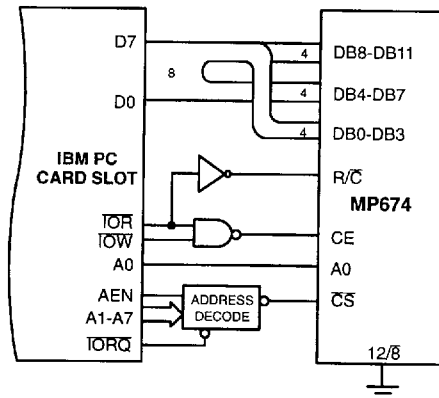


b. Logic 0 to High-Z

Figure 7. Load Circuit for Access Time Test

Figure 8. Load Circuit for Output Float Delay Test

## IBM PC - MP674 INTERFACE







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### “STAND-ALONE” OPERATION

The MP674 can be used in a “stand-alone” mode, which is useful in systems not requiring full computer bus interface capability.

In this mode, CE and 12/8 are wired high,  $\overline{CS}$  and A0 are wired low, and conversion is controlled by R/C. The three-state buffers are enabled when R/C is high and a conversion starts when R/C goes low. This gives rise to two possible control signals – a high pulse or a low pulse. Operation with a low pulse is shown in Figure 9. In this case, the outputs are forced into the high impedance state in response to the falling edge of R/C and return to valid logic levels after the conversion cycle is completed. The STS line goes high 50 ns after R/C goes low and returns low 100 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 10., the data lines are enabled during the time when R/C is high. The falling edge of R/C starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/C.

### CONDITIONING OF INPUT SIGNALS

It is important that the signal being applied to the MP674 input not change during a conversion cycle (it should be stable to within 1/2 LSB). Since that input is being subjected to the DAC test signals (12 comparisons in  $12\mu\text{s} = 1\text{ MHz}$ ), the driving buffer should have a low impedance at 1 MHz.

### STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
$t_{HRL}$	Low R/C Pulse Width	50	30	–	ns
$t_{DS}$	STS Delay from R/C	–	60	200	ns
$t_{HDR}$	Data Valid After R/C Low	20	25	–	ns
$t_{HL}$	Output Float Delay	–	100	150	ns
$t_{HS}$	STS Delay After Data Valid	25	–	850	ns
$t_{HRH}$	High R/C Pulse Width	150	50	–	ns
$t_{DDR}$	Data Access Time	–	90	150	ns

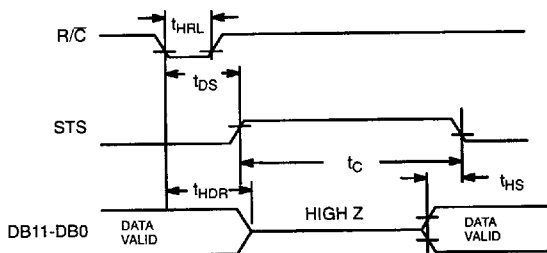


Figure 9. Low Pulse for R/C.  
Outputs Enabled After Conversion

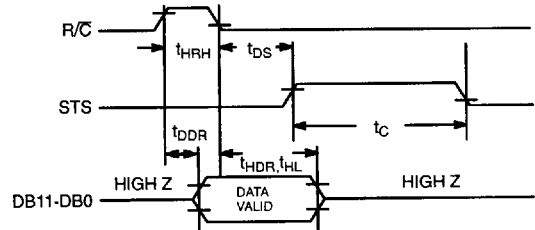


Figure 10. High Pulse for R/C.  
Outputs Enabled While R/C High, Otherwise High-Z