



The Future of Analog IC Technology®

MP8049S

24V, 5.5A

Quad Channel Power Half-Bridge

DESCRIPTION

The MP8049S is a configurable dual channel full-bridge or quad channel half-bridge that can be configured as the output stage of a Class-D audio amplifier. Each full-bridge can be driven independently as stereo single ended audio amplifiers or driven complementary in a bridge tied load (BTL) audio amplifier configuration.

The MP8049S features a low current shutdown mode, standby mode, input under voltage protection, current limit, thermal shutdown and fault flag signal output. All channels of drivers interface with standard logic signals.

The MP8049S is available in a 40 lead QFN 5X5 package.

FEATURES

- 5V to 26V VDD
- ±5.5A Peak Current Output
- Up to 1MHz Switching Frequency
- Protected Integrated Power 0.14Ω Switches
- 10ns Switch Dead Time
- All Switches Current Limited
- Internal Under Voltage Protection
- Internal Thermal Protection
- Short-circuit Protection
- Fault Output Flag
- Bridge Tied Load Output Power: 37W/Channel at 24V, 8Ω

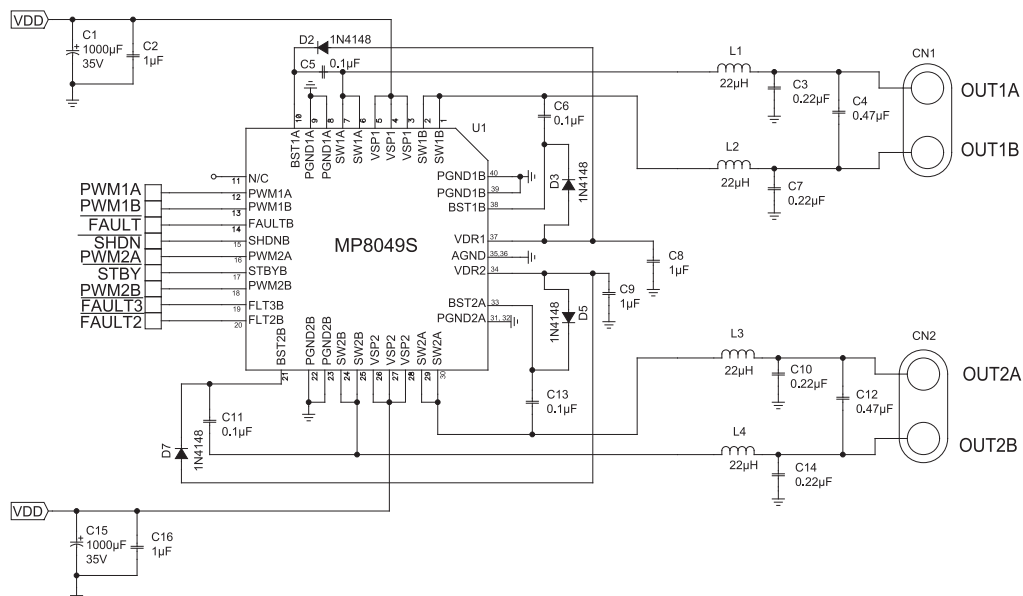
APPLICATIONS

- Flat TV
- Home Theaters
- DVD Receivers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION

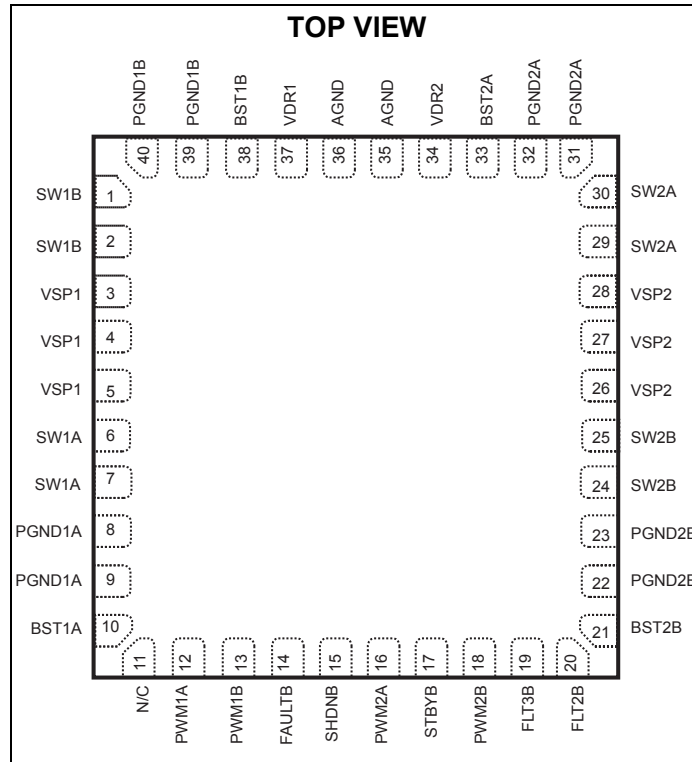


ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|--------------|---------------|-------------|
| MP8049SDU | QFN40 (5x5mm) | MP8049S |

* For Tape & Reel, add suffix -Z (e.g. MP8049SDU-Z).
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP8049SDU-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|--------------------------|
| VSP Supply Voltage | 28V |
| SW1/2 Pin Voltage..... | -0.3V to $V_{DD} + 0.3V$ |
| SW1/2 to BST1/2 | -0.3V to +6V |
| Voltage at All Other Pins..... | -0.3V to +6V |
| Continuous Power Dissipation.. ($T_A = +25^\circ C$) ⁽²⁾ | 4.2W |
| Storage Temperature..... | -55°C to +150°C |
| Junction Temperature..... | 150°C |
| Lead Temperature | 260°C |

Recommended Operating Conditions ⁽³⁾

| | |
|--|-----------------|
| VSP Supply Voltage | 5V to 26V |
| Operating Junction Temp. (T_J) | -40°C to +125°C |

| | | |
|--|---------------------------------|---------------------------------|
| Thermal Resistance ⁽⁴⁾ | θ_{JA} | θ_{JC} |
| QFN40 (5 x 5mm) | 36 | 8 |
| | °C/W | |

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{SP} = 12V$, $V_{SHDNB} = 5V$, $T_A = +25^{\circ}C$, unless otherwise specified.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|--|--------|--|-----|------|-----|-------------|
| VSP Operating Current | | $I_{LOAD} = 0A$, $PWM_{1,2}=0$ | | 2.2 | 3.5 | mA |
| VSP Shutdown Current | | $V_{SHDN} = 0V$ | | 24 | 30 | μA |
| Operating VSP Threshold Low | | | 3.7 | 4 | | V |
| Operating VSP Threshold High | | | | 4.4 | 4.8 | V |
| STBYB Threshold Low | | | 0.8 | 1.0 | | V |
| STBYB Threshold High | | | | 1.6 | 1.8 | V |
| PWM Input Bias Current | | | | 0.1 | 1.0 | μA |
| SHDNB Threshold Low | | | 0.8 | 1.0 | | V |
| SHDNB Threshold High | | | | 1.6 | 1.8 | V |
| PWM _{1,2} Threshold Low | | | 0.8 | 1 | | V |
| PWM _{1,2} Threshold High | | | | 1.6 | 1.8 | V |
| SW _{1/2} On Resistance ⁽⁵⁾ | | $V_{SP} = 7V$, High-Side and Low-Side | | 0.14 | | Ω |
| SW _{1/2} Current Limit ⁽⁵⁾ | | $V_{PWM} = 0V$, Sinking | | 5.5 | | A |
| | | $V_{PWM} = 5V$, Sourcing | | 5.5 | | A |
| SW _{1/2} Switching Frequency | | $V_{PWM} = 0$ to 5V, 50% Duty Cycle | | | 1 | MHz |
| BST Voltage UVLO | | falling value | | 2.2 | | V |
| BST Current | | High-Side MOSFET on, $V_{BST}-V_{SW}=5.5V$ | | 30 | | μA |
| SW _{1/2} Rise/Fall Time ⁽⁵⁾ | | $V_{PWM} = 0V$ to 5V | | 5 | | ns |
| Minimum PWM Pulse Width | | $V_{PWM} = 0V$ to 5V, High or Low Pulse | | 30 | | ns |
| Dead Time ⁽⁵⁾ | | $I_{OUT} = \pm 100mA$ | | 10 | | ns |
| PWM _{1,2} to SW _{1,2} Delay Time Rising | | $V_{PWM} = 0V$ to 5V | | 30 | | ns |
| PWM _{1,2} to SW _{1,2} Delay Time Falling | | $V_{PWM} = 5V$ to 0V | | 30 | | ns |
| Thermal Shutdown Temperature ⁽⁵⁾ | | T_J Rising | | 160 | | $^{\circ}C$ |
| Thermal Shutdown Hysteresis | | | | 35 | | $^{\circ}C$ |

Notes:

5) Not production tested.

OPERATING SPECIFICATIONS ⁽⁶⁾

$V_{SP} = 18V$, $V_{SHDNB} = 5V$, $V_{STBYB} = 5V$, Bridge-tied-load output configuration, $T_A = +25^{\circ}C$, unless otherwise specified.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|------------------------|--------|---|--------------|-----|-----|---------|
| Power Output | P_O | $V_{SP}=18V$, $f = 1kHz$, $THD+N < 1\%$, $R_L = 6\Omega$ | | 20 | | W |
| | | $V_{SP}=24V$, $f = 1kHz$, $THD+N < 1\%$, $R_L = 8\Omega$ | | 30 | | W |
| THD+ Noise | | $V_{SP}=18V/24V$, $f = 1kHz$, $P_O = 1W$, $R_L = 8\Omega/6\Omega$ | | 0.1 | | % |
| Efficiency | | $V_{SP}=24V$, $f = 1kHz$, $P_O = 35W$, 8Ω Load | | 92 | | % |
| SNR | | $P_O=15W$, $R_L = 8\Omega/6\Omega$, A-Weighted | | 100 | | dB |
| Noise Floor | | A-Weighted | | 100 | | μV |
| Cross Talk | | | | -80 | | dB |
| Power Supply Rejection | | $V_{RIPPLE}=200mV_{PP}$ $C_{SP}=1\mu F$ | $f = 1k Hz$ | | -70 | dB |
| | | | $f = 217 Hz$ | | -70 | dB |

Note:

6) Operating Specifications are for the IC in Typical Application circuit.

PIN FUNCTIONS

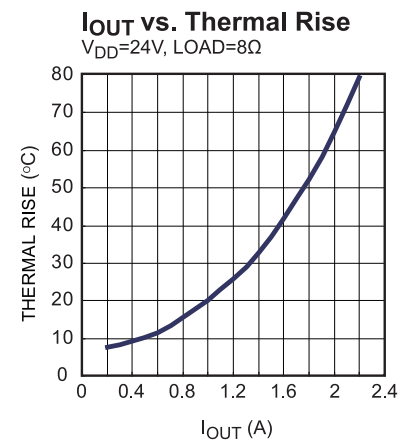
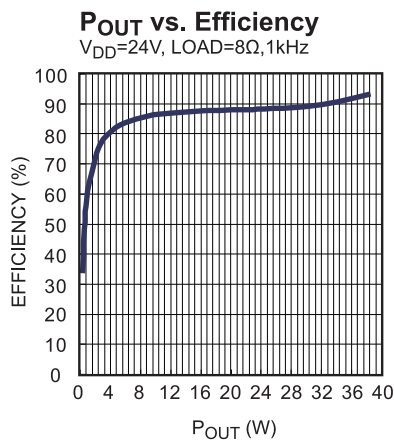
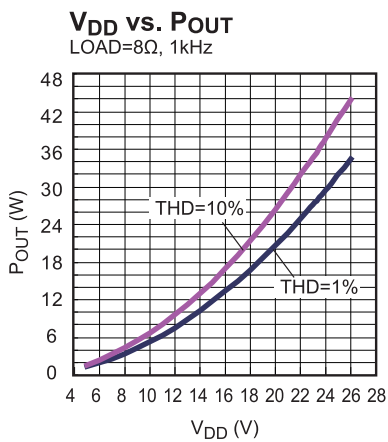
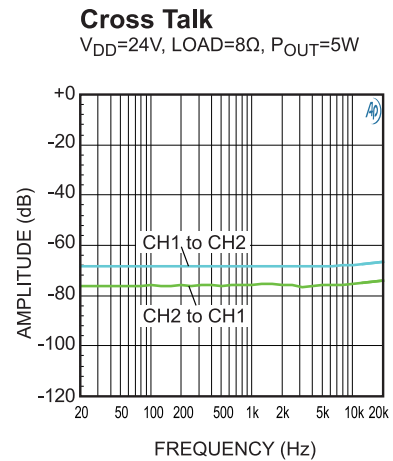
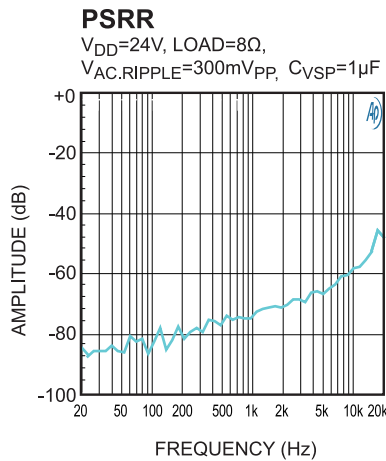
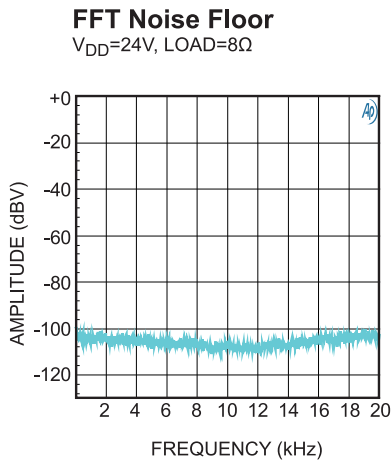
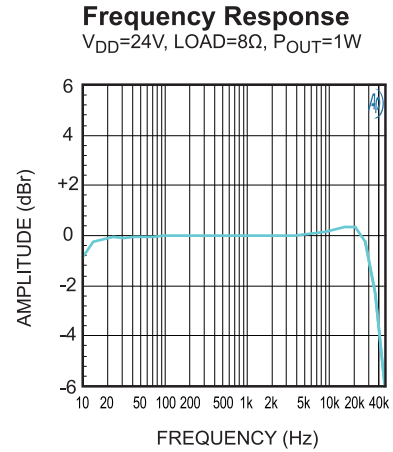
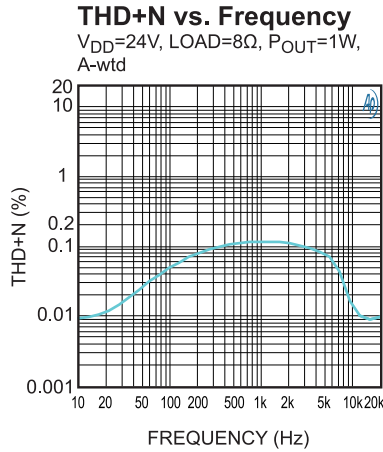
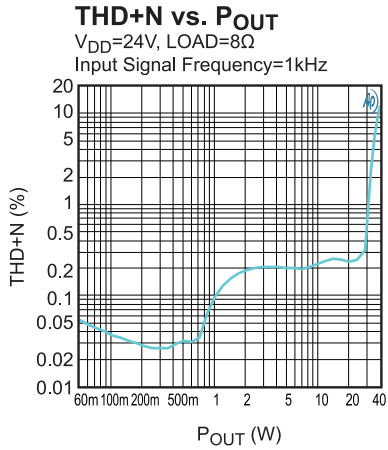
| Pin # | Name | Description |
|-----------|--------|--|
| 1,2 | SW1B | Switched Output 1B. Connect the output LC filter to SW1B. SW1B is valid approximately 100µs after VSP goes high. |
| 3,4,5 | VSP1 | Power Supply Input. Connect VSP1 to the positive side of the input power supply. Bypass VSP1 to PGND as close to the IC as possible. |
| 6,7 | SW1A | Switched Output 1A. Connect the output LC filter to SW1A. SW1A is valid approximately 100µs after VSP goes high. |
| 8,9 | PGND1A | Power Ground of channel 1A. Connect the exposed pad on bottom side to the ground plane. |
| 10 | BST1A | Bootstrap Supply. BST1A powers the high-side gate of the SW1A stage. Connect a 0.1µF or greater capacitor between BST1A and SW1A. |
| 11 | N/C | No connect. |
| 12 | PWM1A | Driver Logic Input 1A. Drive PWM1 with the signal that controls the MP8049S SW1A. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch. |
| 13 | PWM1B | Driver Logic Input 1B. Drive PWM1 with the signal that controls the MP8049S SW1B. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch. |
| 14 | FAULTB | Fault Output. A low output at $\overline{\text{FAULT}}$ indicates that the MP8049S has detected an over temperature or over current or under voltage condition. This output is open drain. |
| 15 | SHDNB | Shutdown Input. When low, the IC will be shut off. |
| 16 | PWM2A | Driver Logic Input 2A. Drive PWM2 with the signal that controls the MP8049S SW2A. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch. |
| 17 | STBYB | Standby Input. Default low (internal pull-down). If driven high, the output of the drivers is determined by the PWM1A/1B/2A/2B. If driven low, the output of both drivers is high impedance. |
| 18 | PWM2B | Driver Logic Input 2B. Drive PWM2 with the signal that controls the MP8049S SW2B. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch. |
| 19 | FLT3B | Fault monitor pin. Detailed please see the Fault Output section. This output is open drain. |
| 20 | FLT2B | Fault monitor pin. Detailed please see the Fault Output section. This output is open drain. |
| 21 | BST2B | Bootstrap Supply. BST2B powers the high-side gate of the SW2B stage. Connect a 0.1µF or greater capacitor between BST2B and SW2B. |
| 22, 23 | PGND2B | Power Ground of Channel 2B. Connect the exposed pad on the bottom side to the ground plane. |
| 24, 25 | SW2B | Switched Output 2B. Connect the output LC filter to SW2B. SW2B is valid approximately 100µs after VSP goes high. |
| 26,27, 28 | VSP2 | Power Supply Input. Connect VSP2 to the positive side of the input power supply. Bypass VSP2 to PGND as close to the IC as possible. |
| 29, 30 | SW2A | Switched Output 2A. Connect the output LC filter to SW2A. SW2A is valid approximately 100µs after VSP goes high. |

PIN FUNCTIONS *(continued)*

| Pin # | Name | Description |
|--------|--------|---|
| 31, 32 | PGND2A | Power Ground of channel 2A. Connect the exposed pad on bottom side to the ground plane. |
| 33 | BST2A | Bootstrap Supply. BST2A powers the high-side gate of the SW2A stage. Connect a 0.1 μ F or greater capacitor between BST2A and SW2A. |
| 34 | VDR2 | Gate Drive Supply Bypass. The voltage at VDR2 is supplied from an internal regulator from its respective VSP. VDR2 powers the internal circuitry and internal MOSFET gate drive for its respective SW2 stage. Bypass VDR2 to PGND with a 0.1 μ F to 10 μ F capacitor. |
| 35, 36 | AGND | Analog Ground. |
| 37 | VDR1 | Gate Drive Supply Bypass. The voltage at VDR1 is supplied from an internal regulator from its respective VSP. VDR1 powers the internal circuitry and internal MOSFET gate drive for its respective SW1 stage. Bypass VDR1 to PGND with a 0.1 μ F to 10 μ F capacitor. |
| 38 | BST1B | Bootstrap Supply. BST1B powers the high-side gate of the SW1B stage. Connect a 0.1 μ F or greater capacitor between BST1B and SW1B. |
| 39,40 | PGND1B | Power Ground of Channel 1B. Connect the exposed pad on bottom side to the ground plane. |

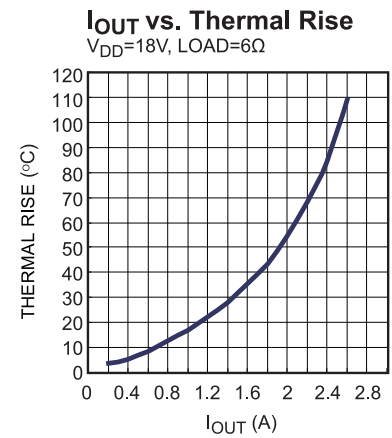
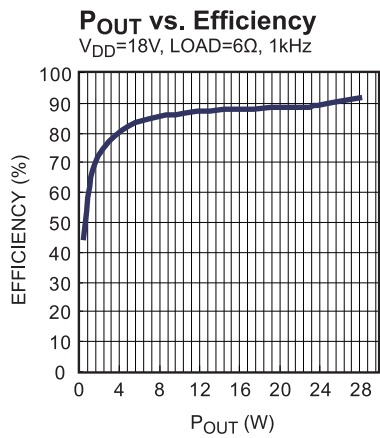
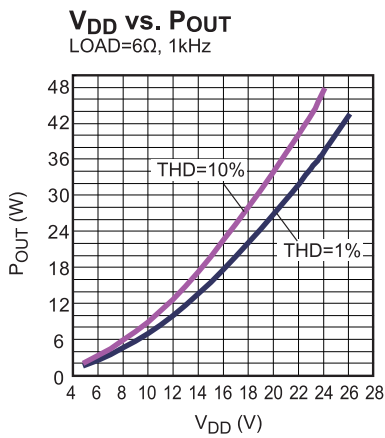
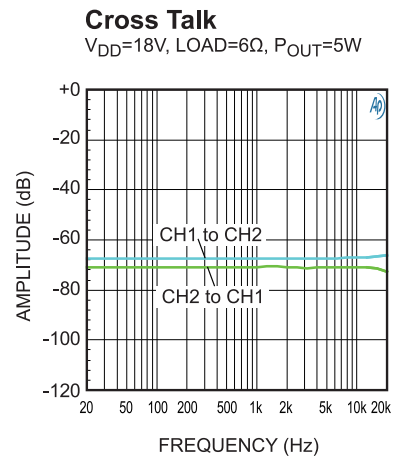
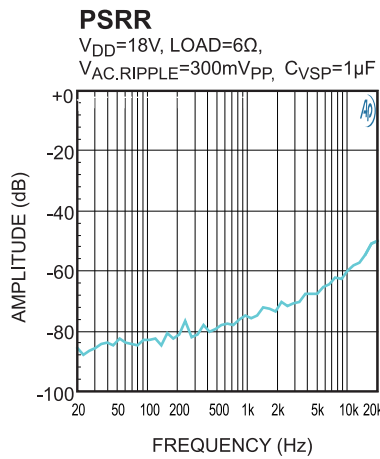
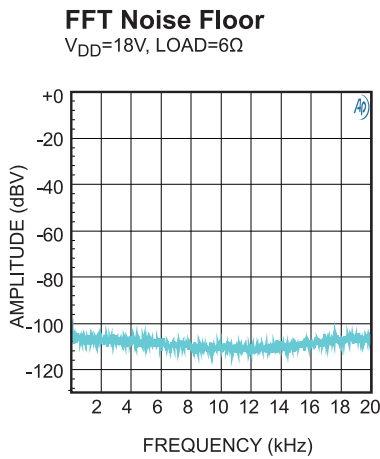
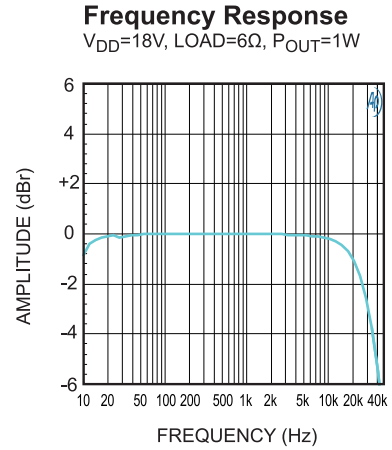
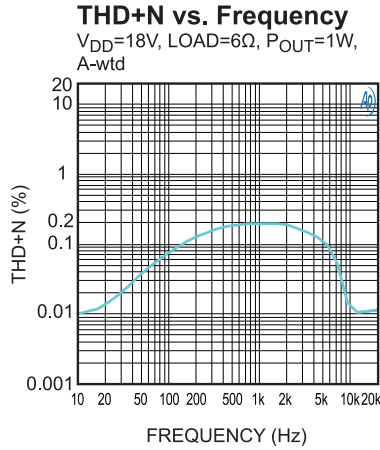
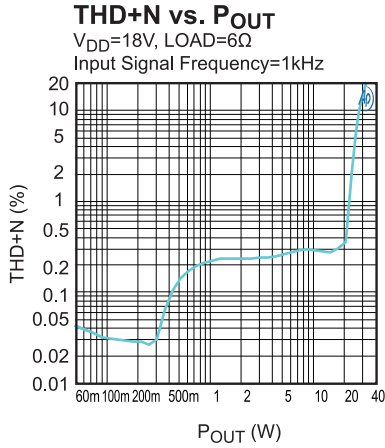
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SP} = 24V$, $V_{SHDNB} = 5V$, $R_{LOAD} = 8\Omega$, Bridge-tied-load output configuration, $T_A = +25^\circ C$, unless otherwise noted.



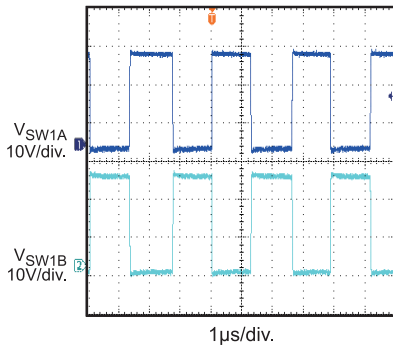
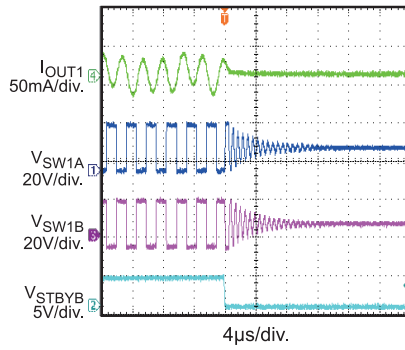
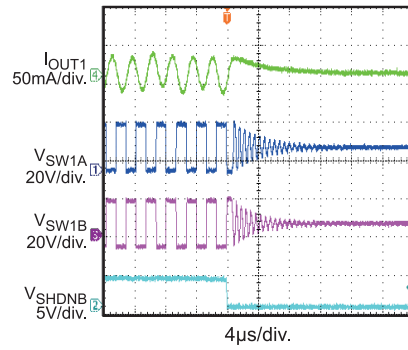
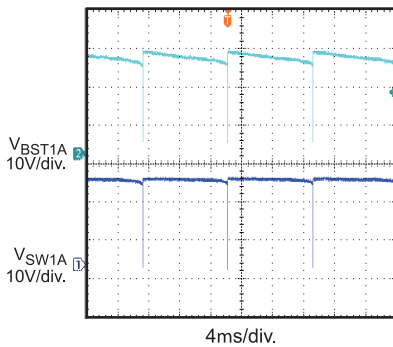
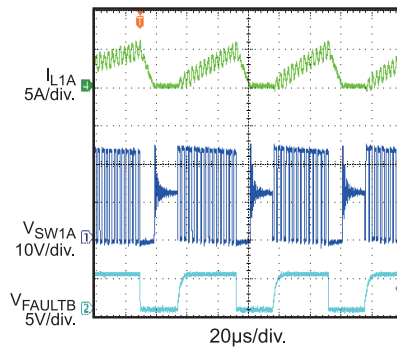
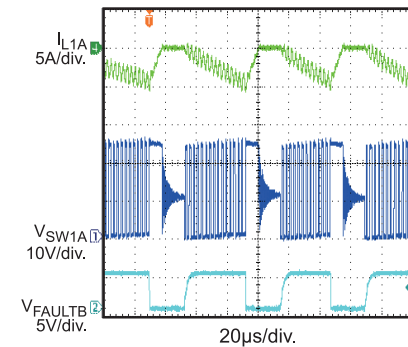
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{SP} = 18V$, $V_{SHDNB} = 5V$, $R_{LOAD} = 6\Omega$, Bridge-tied-load output configuration, $T_A = +25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{SP} = 24V$, $V_{SHDNB} = 5V$, $R_{LOAD} = 8\Omega$, Bridge-tied-load output configuration, $T_A = +25^\circ C$, unless otherwise noted.

Normal Switch Waveform

Standby

Shutdown

BS Recharge Cycling

Short Circuit Positive Current

Short Circuit Negative Current


OPERATION

The MP8049S is a quad channel power half-bridge driver that can be configured as the output of a Class D amplifier. The output is in phase with the input and the dead time is optimized for symmetrical performance, regardless of load conditions.

When the shutdown (SHDN) pin is low, all channels will be off. When the standby (STBYB) is pulled low, it causes the outputs of all channels to go into high impedance. However, when the voltage across the BST1A/1B/2A/2B and SW1A/1B/2A/2B pins drops sufficiently low, the bottom MOSFET will be turned on to refresh the external bootstrap capacitor. Suggest connect a 0.1µF or greater capacitor between BST and SW pins as the bootstrap capacitor.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One of them is to ensure that the supply for the bottom gate drive circuit is sufficiently high and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, an internal current limit of 5.5A is set for all MOSFETs. When this limit is reached, all four MOSFETs of the over current full bridge channel will go into high impedance for a fixed duration of approximately 30µs before resuming normal operation.

Thermal monitoring is also integrated into the MP8049S. If the die temperature rises above 160°C, all switches are turned off. The temperature must fall below 125°C before normal operation resumes.

To enhance the robustness of the device under short circuit condition, a capacitor can be connected to the FaultB pin, as shown in figure 1. The time constant of the RC is selected to be greater than 50ms for the FaultB node to reach 2V. Under short circuit condition, the FaultB node will be reset to zero and the part will be place in standby mode until the voltage at the STBYB pin is above 2V.

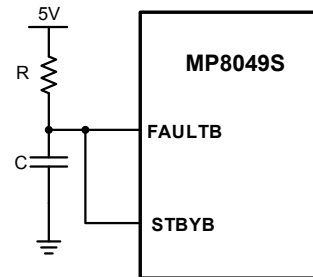


Figure 1—Fault Protection Enhancement Circuit

Fault Output

The MP8049S includes an open drain, active low fault indicator output (FAULTB). A fault will be indicated if one of the following conditions is detected: the current limit is tripped, or the thermal shutdown is tripped.

A fault on any channel will cause the FAULTB pin to be pulled low. When the fault goes away, the MP8049S will resume normal operation.

Do not apply more than 6V to the FAULTB pin.

Error Reporting

The MP8049S also have two fault monitor pins (FLT3B and FLT2B), which are active low and open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system control device, as shown in the below table.

| OCP | OTP | UVP | FLT2B | FLT3B |
|-----|-----|-----|-------|-------|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |

Table 1- Fault Boolean

BLOCK DIAGRAM

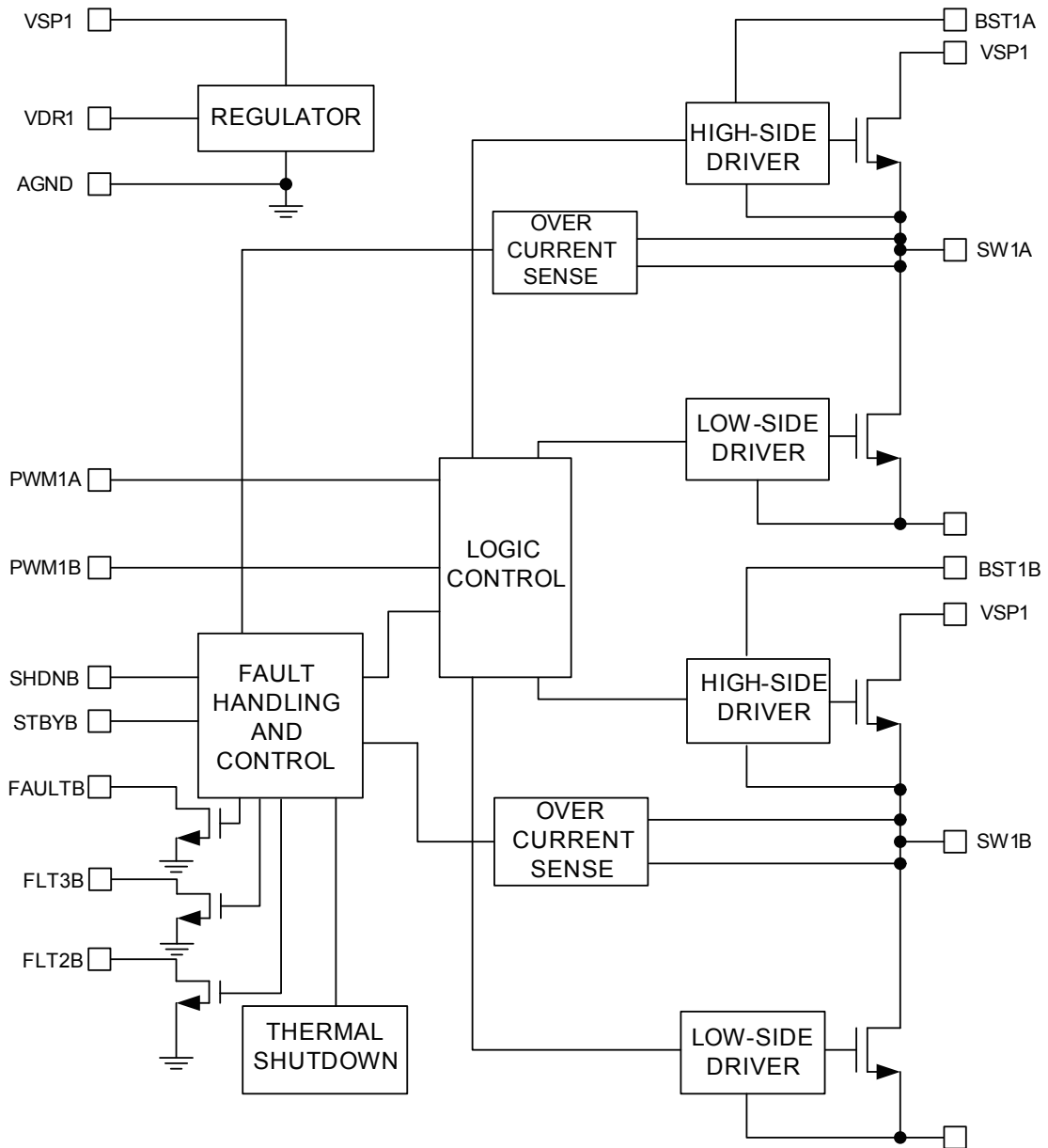
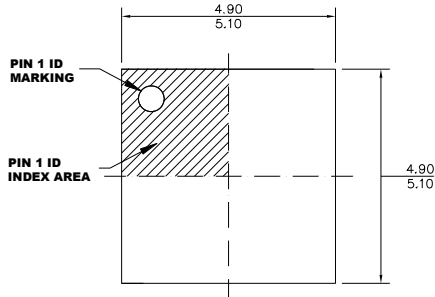


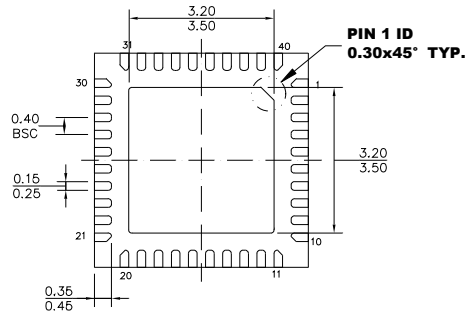
Figure 2—Function Block Diagram (1 full bridge channel only)

PACKAGE INFORMATION

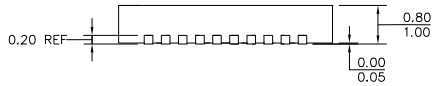
QFN 40 (5x5mm)



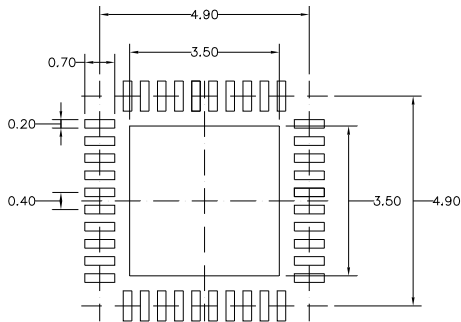
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1
- 5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.